

ULTRA HIGH SPEED MULTIPROTOCOL TRANSCEIVER**ABSOLUTE MAXIMUM RATINGS**

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage (Vcc).....+ 7.0V
 Logic-Interface Voltage (V_L)..... V_L ≤ Vcc
 Input voltage at TTL input pins ... - 0.3V to V_L+0.5V
 Receiver Input voltage..... ±15.5V
 Driver output (from Ground)..... -7.5V to +12.5V
 Short Circuit Duration, TxOUT to GND, Continuous

Continuous Power Dissipation at Ta = +70° C

100-Pin QFP.....1520 mW

(derate 19.0 mW / °C above 70° C)

θJA 52.7 °C/W, θJC 6.5 °C/W

Storage Temperature.....-65°C to +150°C

Lead Temperature (soldering, 10s)..... 300° C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (Vcc)... 4.75V to 5.25V

Logic-Interface Supply Voltage (V_L).....1.65V to 5.25V

Operating Temperature Range.....-40° C to +85° C

TABLE 1: DC ELECTRICAL CHARACTERISTICS

| DC ELECTRICAL CHARACTERISTICS | | | | | | |
|---|-------------------|--|----------------------|-------|----------------------|------|
| V _{CC} = +4.75V to +5.25V, C1-C4 = 1μF. T _{AMB} = T _{MIN} to T _{MAX} , unless otherwise noted. Typical values are at T _{AMB} = +25°C | | | | | | |
| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
| V _{CC} Supply Voltage | V _{CC} | | 4.75 | | 5.25 | V |
| Logic Interface Voltage | V _L | V _{CC} ≥ V _L | 1.65 | | 5.25 | V |
| I _{CC} Shutdown | I _{CCSD} | | | 200 | | μA |
| I _{CC} Supply Current | I _{CC} | | | | 300 | mA |
| DRIVER INPUT AND LOGIC INPUT PINS | | | | | | |
| Logic Input High | V _{IH} | | 2.0 | | | V |
| Logic Input Low | V _{IL} | | | | 0.4 | V |
| RECEIVER OUTPUTS | | | | | | |
| Receiver Logic Output Low | V _{OL} | I _{OUT} = -3.2 mA | | | 0.4 | V |
| Receiver Logic Output High | V _{OH} | I _{OUT} = 1 mA | V _L - 0.3 | | V _L + 0.3 | V |
| Receiver Output Short-Circuit Current | I _{OSS} | 0V < V _O < V _{CC} | | ±20 | ±60 | mA |
| Receiver Output Leakage Current | I _{OZ} | Receivers disabled. 0.4V < V _O < 5.25V | | ±0.05 | ±1 | μA |
| V.28 / RS-232 DRIVERS | | | | | | |
| Output Voltage Swing | V _T | Output load = 3kΩ to GND Fig. 3 | ±5.0 | ±6.0 | ±15.0 | V |
| | V _{OC} | Output load = Open Circuit Fig.2 | | | ±15.0 | V |
| Short Circuit Current | I _{SC} | V _{OUT} = 0V, Fig 5 | | | ±100 | mA |
| Power-Off Impedance | | Fig. 6 | 300 | | | Ω |
| V.28 / RS-232 RECEIVERS | | | | | | |
| Input Voltage Range | | | -15 | | 15 | V |
| Input Threshold Low | | | 0.8 | 1.2 | | V |
| Input Threshold High | | | | 1.7 | 3.0 | V |
| Input Hysteresis | | | | 500 | | mV |
| Input Resistance | | Fig. 8 | 3 | 5 | 7 | kΩ |
| Open Circuit Bias | V _{OC} | Fig. 9 | | | ±2.0 | V |

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +4.75V$ to $+5.25V$, $C1-C4 = 1\mu F$. $T_{AMB} = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_{AMB} = +25^{\circ}C$

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
|--|----------------------------|--|--------------|-----|--------------|------------|
| V.10 / RS-423 DRIVERS | | | | | | |
| Open Circuit Voltage | V_{OC} | Fig.10 | ± 4.0 | | ± 6.0 | V |
| Test Terminated Voltage | V_T | Fig. 11 | $0.9 V_{OC}$ | | | V |
| Short Circuit Current | I_{SC} | Fig. 12 | | | ± 150 | mA |
| Power-Off Current | | Fig. 13 | | | ± 100 | μA |
| V.10 / RS-423 RECEIVERS | | | | | | |
| Input Current | I_{IA} | Fig. 15 and 16 | -3.25 | | +3.25 | mA |
| Input Impedance | | | 4 | 15 | | k Ω |
| Sensitivity | | | | | ± 0.2 | V |
| V.11 / RS-422 DRIVERS | | | | | | |
| Open Circuit Voltage | V_{OC}, V_{OCA}, V_{OCB} | Fig. 17 | | | ± 6.0 | V |
| Test Terminated Voltage | V_T | Fig. 18 | ± 2.0 | | | V |
| Balance | ΔV_T | Fig. 18 | | | ± 0.4 | V |
| Driver DC Offset | V_{OS} | Fig. 18 | | | +3.0 | V |
| Offset Balance | ΔV_{OS} | Fig. 18 | | | ± 0.4 | V |
| Short Circuit Output Current | I_{SA}, I_{SB} | Fig. 19 | | | ± 150 | mA |
| Power-Off Current | | Fig. 20 | | | ± 100 | μA |
| V.11 / RS-422 RECEIVERS | | | | | | |
| Receiver Input Range | V_{CM} | | -7 | | +7 | V |
| Input Current | I_{IA}, I_{IB} | Fig. 21 and 23 | | | ± 3.25 | mV |
| Input Current with Termination | I_{IA}, I_{IB} | Fig. 24 and 25 | | | ± 60.75 | mA |
| Receiver Input Impedance | R_{IN} | $-10V \leq V_{CM} \leq +10V$ | 4 | 15 | | k Ω |
| Receiver Sensitivity | V_{TH} | | | | ± 200 | mV |
| Receiver Input Hysteresis | ΔV_{TH} | $V_{CM} = 0 V$ | | 15 | | mV |
| V.35 DRIVERS (ALL VALUES MEASURE WITH TERM_OFF = '0') | | | | | | |
| Test Terminated Voltage | V_T | Fig. 26 | ± 0.44 | | ± 0.66 | V |
| Offset | V_{OS} | Fig. 26 | | | ± 0.6 | V |
| Output Overshoot | | Fig. 26, $V_{ST} =$ Steady State Voltage | $-0.2V_{ST}$ | | $+0.2V_{ST}$ | V |
| Source Impedance | | Fig. 29, $Z_S = V_2 / V_1 \times 50\Omega$ | 50 | | 150 | Ω |

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75V to +5.25V, C1-C4 = 1μF. T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_{AMB} = +25°C

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
|--|--------|---|------|------|------|------|
| Short Circuit Impedance | | Fig. 28 | 135 | | 165 | Ω |
| V.35 RECEIVERS (ALL VALUES MEASURE WITH TERM_OFF = '0') | | | | | | |
| Sensitivity | | | | ±100 | ±200 | mV |
| Source Impedance | | Fig. 30, Z _S = V ₂ / V ₁ x 50Ω | 90 | | 110 | Ω |
| Short-Circuit Impedance | | Fig. 31 | 135 | | 165 | Ω |
| TRANSCEIVER LEAKAGE CURRENT | | | | | | |
| Driver Output 3-state Current | | Drivers disabled, per Fig. 32 | | 500 | | μA |
| Receiver Output 3-state Current | | Tx and Rx Disabled, 0.4V - V _O - 2.4V | | 1 | 10 | μA |

TABLE 2: AC TIMING CHARACTERISTICS

| TIMING CHARACTERISTICS | | | | | | |
|--|----------------------------|---|------|-----|-----|------------|
| $V_{CC} = +4.75$ to $5.25V$, $C1-C4 = 1\mu F$; $T_{AMB} = T_{MIN}$ to T_{MAX} , unless noted. Typical values are at $T_{AMB} = +25^{\circ}C$. | | | | | | |
| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
| V.28 / RS-232 | | | | | | |
| Maximum Transmission Rate | | Fig. 7 | 250 | | | kbps |
| Driver Propagation Delay | t_{DPLH} , t_{DPLH} | | 0.5 | 1 | 5 | μs |
| Transition Time | | +3V to -3V, -3V to +3V per Fig. 7 | 0.2 | | 1.5 | μs |
| Instantaneous Slew Rate | | +3V to -3V, -3V to +3V per Fig. 4 | 4 | | 30 | V/ μs |
| Driver Skew | | $ t_{DPLH} - t_{DPLH} $ at zero crossing | | 100 | 800 | ns |
| Driver Channel to Channel Skew | | | | 20 | | ns |
| Driver Output Enable Time Tri-state to output Low | t_{ZL} | $C_L = 100$ pF, Fig. 34 and 40, S1 closed | | | 2.0 | μs |
| Driver Output Enable Time Tri-state to output High | t_{ZH} | $C_L = 100$ pF, Fig. 34 and 40, S2 closed | | | 2.0 | μs |
| Driver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 34 and 40, S1 closed | | | 2.0 | μs |
| Driver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 34 and 40, S2 closed | | | 20 | μs |
| Receiver Propagation Delay | t_{PHL} , t_{PLH} | R_IN to R_OUT, $C_L = 15$ pF | 50 | 100 | 500 | ns |
| Receiver Skew | | $ t_{PHL} - t_{PLH} $ at 1.5V | | 50 | | ns |
| Receiver Output Rise / Fall Time | t_R , t_F | $C_L = 15$ pF | | 15 | | ns |
| Receiver Output Enable Time Tri-state to output Low | t_{ZL} | $C_L = 100$ pF, Fig. 35 and 40, S1 closed | | | 2.0 | μs |
| Receiver Output Enable Time Tri-state to output High | t_{ZH} | $C_L = 100$ pF, Fig. 35 and 40, S2 closed | | | 2.0 | μs |
| Receiver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 35 and 40, S1 closed | | | 2.0 | μs |
| Receiver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 35 and 40, S2 closed | | | 2.0 | μs |
| Charge Pump Rise Time | | Shutdown to normal operation | | | 2 | ms |
| V.10 / RS-423 | | | | | | |
| Maximum Transmission Rate | | | 250 | | | kbps |

TIMING CHARACTERISTICS

$V_{CC} = +4.75$ to $5.25V$, $C1-C4 = 1\mu F$; $T_{AMB} = T_{MIN}$ to T_{MAX} , unless noted. Typical values are at $T_{AMB} = +25^{\circ}C$.

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
|--|----------------------|--|------|-----|-----|---------|
| Driver Propagation Delay | t_{PHL}, t_{PLH} | | 30 | 150 | 500 | ns |
| Driver Rise / Fall Time | t_R, t_F | 10% to 90% - Fig. 14 | | | 500 | ns |
| Driver Skew | | $ t_{DPHL} - t_{DPLH} $ at zero crossing | | | 100 | ns |
| Driver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 34 and 40, S1 closed | | | 2 | μs |
| Driver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 34 and 40, S2 closed | | | 2 | μs |
| Driver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 34 and 40, S1 closed | | | 2 | μs |
| Driver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 34 and 40, S2 closed | | | 2 | μs |
| Receiver Propagation Delay | t_{PHL}, t_{PLH} | | | 100 | 500 | ns |
| Receiver Output Enable Time Tri-state to output Low | t_{ZL} | $C_L = 100$ pF, Fig. 35 and 40, S1 closed | | | 2 | μs |
| Receiver Output Enable Time Tri-state to output High | t_{ZH} | $C_L = 100$ pF, Fig. 35 and 40, S2 closed | | | 2 | μs |
| Receiver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 35 and 40, S1 closed | | | 2 | μs |
| Receiver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 35 and 40, S1 closed | | | | |
| Receiver Output Rise / Fall Time | t_R, t_F | $C_L = 15$ pF | | 15 | | ns |
| Receiver Skew | | $ t_{PHL} - t_{PLH} $ at 1.5V | | 5 | | ns |
| HIGH SPEED V.11 / RS-422 (DRIVERS 1, 2 & 3, RECEIVERS 1, 2 & 3) | | | | | | |
| Maximum Bit Rate | | NRZI Encoding | 52 | | | Mbps |
| Driver Rise and Fall Time | t_R, t_F | Fig. 22 and 36, 10-90% | 0.5 | | 6 | ns |
| Propagation Delay Time | t_{DPHL}, t_{DPLH} | Fig. 33 and 36, $C_L = 50$ pF | | 5 | 25 | ns |
| Differential Skew | | $ t_{DPHL} - t_{DPLH} $ | | | 3.8 | ns |
| Driver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 34 and 37, S1 closed | | | 100 | ns |
| Driver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 34 and 37, S2 closed | | | 100 | ns |
| Driver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 34 and 37, S1 closed | | | 100 | ns |

TIMING CHARACTERISTICS

$V_{CC} = +4.75$ to $5.25V$, $C1-C4 = 1\mu F$; $T_{AMB} = T_{MIN}$ to T_{MAX} , unless noted. Typical values are at $T_{AMB} = +25^{\circ}C$.

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
|---|----------------------|--|------|-----|-----|------|
| Driver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 34 and 37, S2 closed | | | 100 | ns |
| Receiver Propagation Delay | t_{PHL}, t_{PLH} | Fig. 33, 36 $C_L = 50$ pF | | 20 | 50 | ns |
| Receiver Skew | | $ t_{PHL} - t_{PLH} $ Fig. 33, 36 $C_L = 50$ pF | | | 3.8 | ns |
| Receiver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 35 and 39, S1 closed | | | 100 | ns |
| Receiver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 35 and 39, S2 closed | | | 100 | ns |
| Receiver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 35 and 39, S1 closed | | | 100 | ns |
| Receiver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 35 and 39, S2 closed | | | 100 | ns |
| Receiver Output Rise / Fall Time | t_R, t_F | $3.0V < V_L < 5.5V$ $1.65V < V_L < 3.0V$ $C_L = 50$ pF | 0.5 | | 6 | ns |
| Channel to channel Skew | | | | 2 | | ns |
| V.11 / RS-422 HANDSHAKE SIGNALS (DRIVERS 4, 5 & 6, RECEIVERS 4, 5 & 6) | | | | | | |
| Maximum Transmission Rate | | Fig. 33 | 10 | | | Mbps |
| Driver Rise and Fall Time | t_R, t_F | Fig. 22 and 36 | | 2 | 10 | ns |
| Propagation Delay Time | t_{DPHL}, t_{DPLH} | Fig. 33 and 36, $C_L = 50$ pF | | 20 | 50 | ns |
| Driver Propagation Delay Skew | | $ t_{DPHL} - t_{DPLH} $ | | | 10 | ns |
| Driver Channel to Channel Skew | | | | 2 | | ns |
| Driver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 34 and 37, S1 closed | | | 100 | ns |
| Driver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 34 and 37, S2 closed | | | 100 | ns |
| Driver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 34 and 37, S1 closed | | | 100 | ns |
| Driver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 34 and 37, S2 closed | | | 100 | ns |
| Receiver Propagation Delay | t_{PHL}, t_{PLH} | Fig. 33, 36 $C_L = 50$ pF | | 20 | 50 | ns |

TIMING CHARACTERISTICS

$V_{CC} = +4.75$ to $5.25V$, $C1-C4 = 1\mu F$; $T_{AMB} = T_{MIN}$ to T_{MAX} , unless noted. Typical values are at $T_{AMB} = +25^{\circ}C$.

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
|--|----------------------|---|------|-----|-----|------|
| Receiver Skew | | $ t_{PHL} - t_{PLH} $ Fig. 33, 36 $C_L = 50$ pF | | | 10 | ns |
| Receiver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 35 and 39, S1 closed | | | 100 | ns |
| Receiver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 35 and 39, S2 closed | | | 100 | ns |
| Receiver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 35 and 39, S1 closed | | | 100 | ns |
| Receiver Output Disable Time Output Low to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 35 and 39, S2 closed | | | 100 | ns |
| Receiver Output Rise / Fall Time | t_R, t_F | | 1 | | 20 | ns |
| Channel to Channel Skew | | | | 2 | | ns |
| V.35 (DRIVERS 1, 2 & 3, RECEIVERS 1, 2 & 3) | | | | | | |
| Maximum Transmission Rate | | Fig. 33, $f_{MAX} = 20$ MHz | 40 | | | Mbps |
| Driver Rise and Fall Time | t_R, t_F | Fig. 29 | | | 10 | ns |
| Propagation Delay Time | t_{DPHL}, t_{DPLH} | Fig. 33 and 36, $C_L = 50$ pF | | 20 | 50 | ns |
| Driver Differential Skew | | $ t_{DPHL} - t_{DPLH} $ Fig. 33 and 36 | | | 5.0 | ns |
| Driver Channel to Channel Skew | | | | 2 | | ns |
| Driver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 34 and 37, S1 closed | | | 200 | ns |
| Driver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 34 and 37, S2 closed | | | 200 | ns |
| Driver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 34 and 37, S1 closed | | | 200 | ns |
| Driver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 34 and 37, S2 closed | | | 200 | ns |
| Receiver Propagation Delay | t_{PHL}, t_{PLH} | Fig. 33, 38 $C_L = 50$ pF | | 18 | 30 | ns |
| Receiver Skew | | $ t_{PHL} - t_{PLH} $ Fig. 33 and 38 $C_L = 50$ pF | | | 5.0 | ns |
| Receiver Output Enable Time Tri-state to Output Low | t_{ZL} | $C_L = 100$ pF, Fig. 35 and 39, S1 closed | | | 200 | ns |

TIMING CHARACTERISTICS

$V_{CC} = +4.75$ to $5.25V$, $C1-C4 = 1\mu F$; $T_{AMB} = T_{MIN}$ to T_{MAX} , unless noted. Typical values are at $T_{AMB} = +25^{\circ}C$.

| PARAMETERS | SYMBOL | TEST CONDITIONS | MIN. | TYP | MAX | UNIT |
|--|----------|--|------|-----|-----|------|
| Receiver Output Enable Time Tri-state to Output High | t_{ZH} | $C_L = 100$ pF, Fig. 35 and 39, S2 closed | | | 200 | ns |
| Receiver Output Disable Time Output Low to Tri-state | t_{LZ} | $C_L = 15$ pF, Fig. 35 and 39, S1 closed | | | 200 | ns |
| Receiver Output Disable Time Output High to Tri-state | t_{HZ} | $C_L = 15$ pF, Fig. 35 and 39, S2 closed | | | 200 | ns |

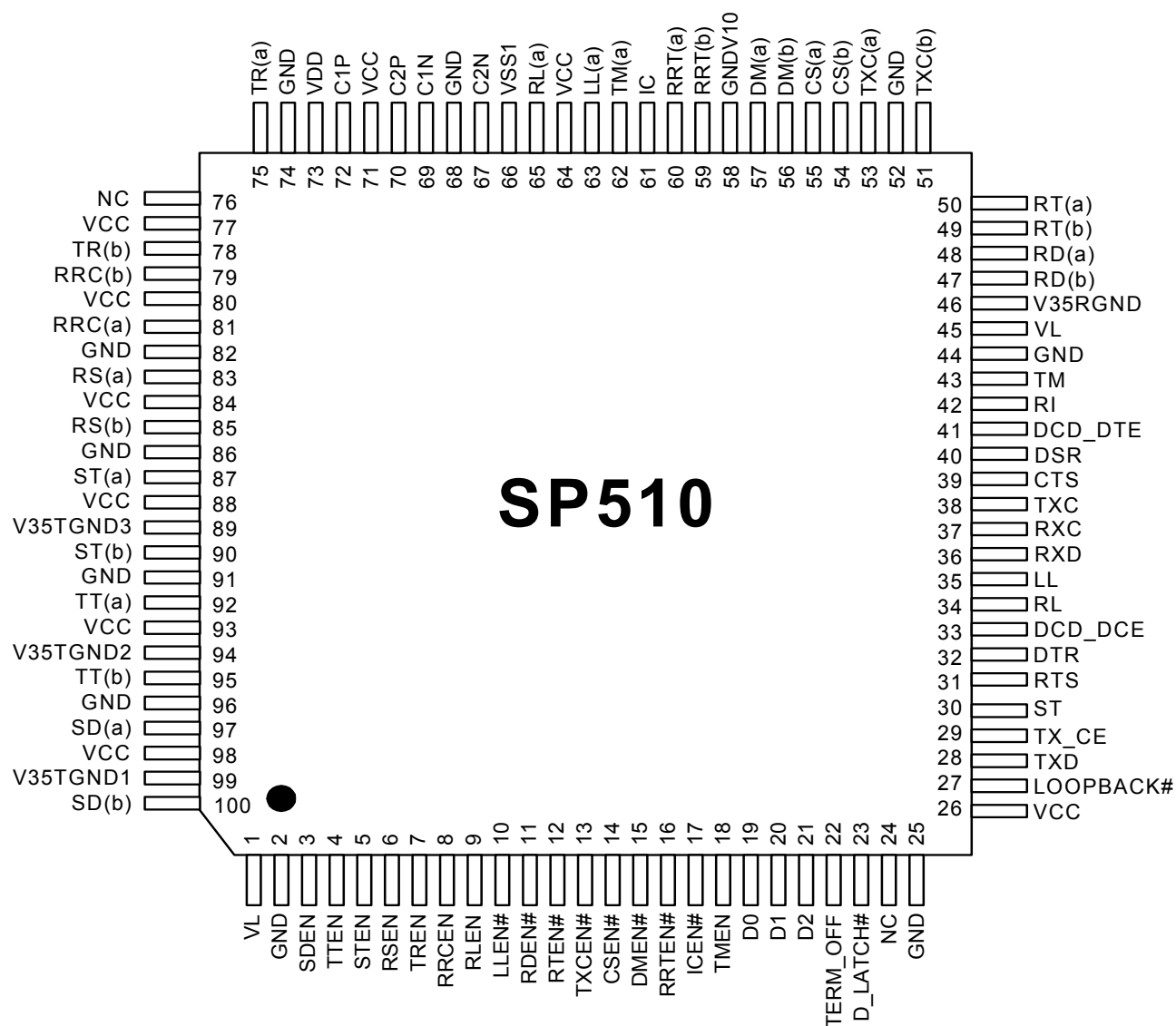
FIGURE 1. PIN OUT DIAGRAM


TABLE 3: PIN DESCRIPTIONS BY FUNCTION

| Pin Name | Pin Number | I/O | | DESCRIPTION |
|-----------------------------|------------|-----|-----|--|
| DIFFERENTIAL DRIVERS | | | | |
| TxD | 28 | I | TTL | TxD Driver Input |
| SD(b) / SD(a) | 100, 97 | O | TTL | Differential Transmit data non-inverting (b) and inverting (a) outputs |
| V35TGND1 | 99 | I | | SD Termination Reference |
| SDEN | 3 | I | TTL | TxD Driver Enable |
| TxCE | 29 | I | TTL | TxCE Driver Input |
| TT(b) / TT(a) | 95, 92 | O | TTL | Differential TxCE non-inverting (b) and inverting (a) outputs |
| V35TGND2 | 94 | I | | TT Termination Reference |
| TTEN | 4 | I | TTL | TxCE Driver Enable |
| ST | 30 | I | TTL | ST Driver Input |
| ST(b) / ST(a) | 90, 87 | O | TTL | Differential ST non-inverting (b) and inverting (a) outputs |
| V35TGND3 | 89 | I | | ST Termination Reference |
| STEN | 5 | I | TTL | ST Driver Enable |
| RTS | 31 | I | TTL | RTS Driver Input |
| RS(b) / RS(a) | 85, 83 | O | TTL | Differential RTS non-inverting (b) and inverting (a) outputs |
| RSEN | 6 | I | TTL | RTS Driver Enable |
| DTR | 32 | I | TTL | DTR Driver Input |
| TR(b) / TR(a) | 78, 75 | O | TTL | Differential DTR non-inverting (b) and inverting (a) outputs |
| TREN | 7 | I | TTL | DTR Driver Enable |
| DCD_DCE | 33 | I | TTL | DCD_DCE Driver Input |
| RRC(b) / RRC(a) | 79, 81 | O | TTL | Differential DCD non-inverting (b) and inverting (a) outputs |
| RRCEN | 8 | I | TTL | DCD Driver Enable |
| SINGLE ENDED DRIVERS | | | | |
| RL | 34 | I | TTL | RL Driver Input |
| RL(a) | 65 | O | TTL | RL Driver Output |
| RLEN | 9 | I | TTL | RL Driver Enable |
| LL | 35 | I | TTL | LL Driver Input |
| LL(a) | 63 | O | TTL | LL Driver Output |
| LLEN# | 10 | I | TTL | LL Driver Enable, active low |

| Pin Name | Pin Number | I/O | | DESCRIPTION |
|--|------------|-----|-----|--|
| DIFFERENTIAL RECEIVERS | | | | |
| RxD | 36 | O | TTL | RxD Receiver Output |
| RD(b) / RD(a) | 47, 48 | I | TTL | Differential RXD non-inverting (b) and inverting (a) inputs |
| RDEN# | 11 | I | TTL | RxD Receiver Enable, active low |
| RxC | 37 | O | TTL | RxC Receiver Output |
| RT(b) / RT(a) | 49, 50 | I | TTL | Differential RXC non-inverting (b) and inverting (a) inputs |
| RTEN# | 12 | I | TTL | RxC Receiver Enable, active low |
| TxC | 38 | O | TTL | TxC Receiver Output |
| TxC(b) / TxC(a) | 51, 53 | I | TTL | Differential TxC non-inverting (b) and inverting (a) inputs |
| TxCEN# | 13 | I | TTL | TxC Receiver Enable, active low |
| CTS | 39 | O | TTL | CTS Receiver Output |
| CS(b) / CS(a) | 54, 55 | I | TTL | Differential CTS non-inverting (b) and inverting (a) inputs |
| CSEN# | 14 | I | TTL | CTS Receiver Enable, active low |
| DSR | 40 | O | TTL | DSR Receiver Output |
| DM(b) / DM(a) | 56, 57 | I | TTL | Differential DSR non-inverting (b) and inverting (a) inputs |
| DMEN# | 15 | I | TTL | DSR Receiver Enable, active low |
| DCD_DTE | 41 | O | TTL | DCD_DTE Receiver Output |
| RRT(b) / RRT(a) | 59, 60 | I | TTL | Differential DCD_DTE non-inverting (b) and inverting (a) inputs |
| RRTEN# | 16 | I | TTL | DCD_DTE Receiver Enable, active low |
| SINGLE ENDED RECEIVERS | | | | |
| IC | 61 | I | TTL | RI Receiver Input |
| RI | 42 | O | TTL | RI Receiver Output |
| ICEN# | 17 | I | TTL | RI Receiver Enable, active low |
| TM(a) | 62 | I | TTL | TM Receiver Input |
| TM | 43 | O | TTL | TM Receiver Output |
| TMEN | 18 | I | TTL | TM Receiver Enable |
| PROTOCOL MODE SELECTION SIGNALS | | | | |
| D2, D1, D0 | 21, 20, 19 | I | TTL | Mode Select - Refer to Table 5 and Table 6 |

| Pin Name | Pin Number | I/O | | DESCRIPTION |
|--------------------------|---------------------------------------|-----|-----|--|
| Charge Pump Signals | | | | |
| C1P, C1N | 72, 69 | I | | Charge Pump Capacitor 1 +/- inputs. Connect a 1 μF capacitor between C1P and C1N pins. |
| C2P, C2N | 70, 67 | I | | Charge Pump Capacitor 2 +/- inputs. Connect a 1 μF capacitor between C2P and C2N pins. |
| VSS1 | 66 | I | | -2xVCC Charge Pump |
| VDD | 73 | I | | 2xVCC Charge Pump |
| GENERAL CONTROL SIGNALS | | | | |
| LOOPBACK# | 27 | I | TTL | Loopback mode enable, active low |
| D_LATCH# | 23 | I | | Decoder Latch, active low |
| TERM_OFF | 22 | I | | Termination disable |
| RESERVED PINS | | | | |
| NC | 24, 76 | | | No Connect |
| POWER AND GROUND SIGNALS | | | | |
| VCC | 26, 64, 71, 77, 80, 84, 88, 98 | I | | 5V supply. |
| VL | 1, 45 | I | | Logic I/O Power Supply Input |
| GND | 2, 25, 44, 52, 68, 74, 82, 86, 91, 96 | I | | Ground. |
| GNDV10 | 58 | I | | V.10 Receiver Ground Reference |
| V35RGND | 46 | O | | Receiver Termination Reference |

NOTE: Pin type: I = Input, O = Output, I/O = Input/output.

TABLE 4: PIN DESCRIPTIONS BY PIN NUMBER

| PIN DESCRIPTIONS BY PIN NUMBER | | | | | |
|--------------------------------|------------|-------------------------------|----|---------|--------------------------------|
| 1 | VL | Logic I/O Power Supply Input | 32 | DTR | DTR Driver TTL Input |
| 2 | GND | Ground | 33 | DCD_DCE | DCD_DCE Driver TTL Input |
| 3 | SDEN | TxD Driver Enable Input | 34 | RL | RL Driver TTL Input |
| 4 | TTEN | TxCE Driver Enable Input | 35 | LL | LL Driver TTL Input |
| 5 | STEN | ST Driver Enable Input | 36 | RxD | RxD Receiver TTL Output |
| 6 | RSEN | RTS Driver Enable Input | 37 | RxC | RxC Receiver TTL Output |
| 7 | TREN | DTR Driver Enable Input | 38 | TxC | TxC Receiver TTL Output |
| 8 | RRCEN | DCD Driver Enable Input | 39 | CTS | CTS Receiver TTL Output |
| 9 | RLEN | RL Driver Enable Input | 40 | DSR | DSR Receiver TTL Output |
| 10 | LLEN# | LL Driver Enable Input | 41 | DCD_DTE | DCD_DTE Receiver TTL Output |
| 11 | RDEN# | RxD Receiver Enable Input | 42 | RI | RI Receiver TTL Output |
| 12 | RTEN# | RxC Receiver Enable Input | 43 | TM | TM Receiver TTL Output |
| 13 | TxCEN# | TxC Receiver Enable Input | 44 | GND | Ground |
| 14 | CSEN# | CTS Receiver Enable Input | 45 | VL | Logic I/O Power Supply Input |
| 15 | DMEN# | DSR Receiver Enable Input | 46 | V35RGND | Receiver Termination Reference |
| 16 | RRTEN# | DCD_DTE Receiver Enable Input | 47 | RD(b) | RXD Non-Inverting Input |
| 17 | ICEN# | RI Receiver Enable Input | 48 | RD(a) | RXD Inverting Input |
| 18 | TMEN | TM Receiver Enable Input | 49 | RT(b) | RxC Non-Inverting Input |
| 19 | D0 | Mode Select Input - Bit 0 | 50 | RT(a) | RxC Inverting Input |
| 20 | D1 | Mode Select Input - Bit 1 | 51 | TxC(b) | TxC Non-Inverting Input |
| 21 | D2 | Mode Select Input - Bit 2 | 52 | GND | Ground |
| 22 | TERM_OFF | Termination Disable Input | 53 | TxC(a) | TxC Inverting Input |
| 23 | D_LATCH# | Decoder Latch Input | 54 | CS(b) | CTS Non-Inverting Input |
| 24 | NC | No Connect | 55 | CS(a) | CTS Inverting Input |
| 25 | GND | Ground | 56 | DM(b) | DSR Non-Inverting Input |
| 26 | Vcc | Power Supply Input | 57 | DM(a) | DSR Inverting Input |
| 27 | LOOP-BACK# | Loopback Mode Enable Input | 58 | GNDV10 | V.10 Rx Ground Reference |
| 28 | TxD | TxD Driver TTL Input | 59 | RRT(b) | DCD_DTE Non-Inverting Input |
| 29 | TxCE | TxCE Driver TTL Input | 60 | RRT(a) | DCD_DTE Inverting Input |
| 30 | ST | ST Driver TTL Input | 61 | IC | RI Receiver Input |
| 31 | RTS | RTS Driver TTL Input | 62 | TM(a) | TM Receiver Input |

| PIN DESCRIPTIONS BY PIN NUMBER | | | | | |
|--------------------------------|--------|--------------------------|-----|----------|---------------------------|
| 63 | LL(a) | LL Driver Output | 82 | GND | Ground |
| 64 | VCC | Power Supply Input | 83 | RS(a) | RTS Inverting Output |
| 65 | RL(a) | RL Driver Output | 84 | VCC | Power Supply Input |
| 66 | VSS1 | -2xVCC Charge Pump | 85 | RS(b) | RTS Non-Inverting Output |
| 67 | C2N | Charge Pump Capacitor | 86 | GND | Ground |
| 68 | GND | Ground | 87 | ST(a) | ST Inverting Output |
| 69 | C1N | Charge Pump Capacitor | 88 | VCC | Power Supply Input |
| 70 | C2P | Charge Pump Capacitor | 89 | V35TGND3 | ST Termination Reference |
| 71 | VCC | Power Supply Input | 90 | ST(b) | ST Non-Inverting Output |
| 72 | C1P | Charge Pump Capacitor | 91 | GND | Ground |
| 73 | VDD | 2xVCC Charge Pump | 92 | TT(a) | TxCE Inverting Output |
| 74 | GND | Ground | 93 | VCC | 5V Power Supply |
| 75 | TR(a) | DTR Inverting Output | 94 | V35TGND2 | TT Termination Reference |
| 76 | NC | No Connect | 95 | TT(b) | TxCE Non-Inverting Output |
| 77 | VCC | Power Supply Input | 96 | GND | Ground |
| 78 | TR(b) | DTR Non-Inverting Output | 97 | SD(a) | TxD Inverting Output |
| 79 | RRC(b) | DCD Non-Inverting Output | 98 | VCC | 5V Power Supply |
| 80 | VCC | Power Supply Input | 99 | V35TGND1 | SD Termination Reference |
| 81 | RRC(a) | DCD Inverting Output | 100 | SD(b) | TxD Non-Inverting Output |

TABLE 5: DRIVER MODE SELECTION

| DRIVER OUTPUT PIN | V.35 MODE | EIA-530 MODE | RS-232 MODE (V.28) | EIA- 530A MODE | RS-449 MODE (V.36) | X.21 MODE (V.11) | SHUT- DOWN | SUGGESTED SIGNAL |
|-----------------------|--------------|-----------------|--------------------------|----------------------|--------------------------|------------------------|---------------|---------------------|
| MODE (D0, D1, D2) | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| T ₁ OUT(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxD(a) |
| T ₁ OUT(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxD(b) |
| T ₂ OUT(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxCE(a) |
| T ₂ OUT(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxCE(b) |
| T ₃ OUT(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxC_DCE(a) |
| T ₃ OUT(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxC_DCE(b) |
| T ₄ OUT(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | RTS(a) |
| T ₄ OUT(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | RTS(b) |
| T ₅ OUT(a) | V.28 | V.11 | V.28 | V.10 | V.11 | V.11 | High-Z | DTR(a) |
| T ₅ OUT(b) | High-Z | V.11 | High-Z | High-Z | V.11 | V.11 | High-Z | DTR(b) |
| T ₆ OUT(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | DCD_DCE(a) |
| T ₆ OUT(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | DCD_DCE(b) |
| T ₇ OUT(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | RL |
| T ₈ OUT(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | LL |

TABLE 6: RECEIVER MODE SELECTION

| RECEIVER INPUT PIN | V.35 MODE | EIA-530 MODE | RS-232 MODE (V.28) | EIA- 530A MODE | RS-449 MODE (V.36) | X.21 MODE (V.11) | SHUT- DOWN | SUGGESTED SIGNAL |
|-----------------------|--------------|-----------------|--------------------------|----------------------|--------------------------|------------------------|---------------|---------------------|
| MODE (D0, D1, D2) | 001 | 010 | 011 | 100 | 101 | 110 | 111 | |
| R ₁ IN(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | RxD(a) |
| R ₁ IN(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | RxD(b) |
| R ₂ IN(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | RxCe(a) |
| R ₂ IN(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | RxCe(b) |
| R ₃ IN(a) | V.35 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | TxC_DTE(a) |
| R ₃ IN(b) | V.35 | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | TxC_DTE(b) |
| R ₄ IN(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | CTS(a) |
| R ₄ IN(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | CTS(b) |
| R ₅ IN(a) | V.28 | V.11 | V.28 | V.10 | V.11 | V.11 | High-Z | DSR(a) |
| R ₅ IN(b) | High-Z | V.11 | High-Z | High-Z | V.11 | V.11 | High-Z | DSR(b) |
| R ₆ IN(a) | V.28 | V.11 | V.28 | V.11 | V.11 | V.11 | High-Z | DCD_DTE(a) |
| R ₆ IN(b) | High-Z | V.11 | High-Z | V.11 | V.11 | V.11 | High-Z | DCD_DTE(b) |
| R ₇ IN(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | RI |
| R ₈ IN(a) | V.28 | V.10 | V.28 | V.10 | V.10 | High-Z | High-Z | TM |

TABLE 7: V.11 & V.35 DRIVERS

| INPUTS | | OUTPUTS | |
|--------|-------|---------|-------|
| Tx_EN# | Tx_IN | Tx(A) | Tx(B) |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |

TABLE 11: V.10 DRIVERS

| INPUTS | | OUTPUTS | |
|--------|-------|---------|---------|
| Tx_EN# | Tx_IN | Tx(A) | Tx(B) |
| 1 | 1 | < -4V | > 30 kΩ |
| 1 | 0 | > +4V | > 30 kΩ |

TABLE 8: V.11 & V.35 RECEIVERS

| INPUTS | OUTPUTS |
|----------------|---------|
| Rx(A) - Rx(B) | RO |
| ≥ 200 mV | 1 |
| ≤ -200 mV | 0 |
| Open / shorted | 1 |

TABLE 12: V.10 RECEIVERS

| INPUTS | OUTPUTS |
|---------------|---------|
| Rx(A) - Rx(B) | RO |
| ≥ +0.3V | 0 |
| ≤ -0.3V | 1 |
| Open / ground | 1 |

TABLE 9: V.28 DRIVERS

| INPUTS | | OUTPUTS | |
|--------|-------|---------|---------|
| Tx_EN# | Tx_IN | Tx(A) | Tx(B) |
| 1 | 1 | < -5V | > 30 kΩ |
| 1 | 0 | > +5V | > 30 kΩ |

TABLE 10: V.28 RECEIVERS

| INPUTS | OUTPUTS |
|---------------|---------|
| Rx(A) - Rx(B) | RO |
| ≥ +3V | 0 |
| ≤ -3V | 1 |
| Open / ground | 1 |

FIGURE 2. V.28 DRIVER OUTPUT OPEN CIRCUIT VOLTAGE

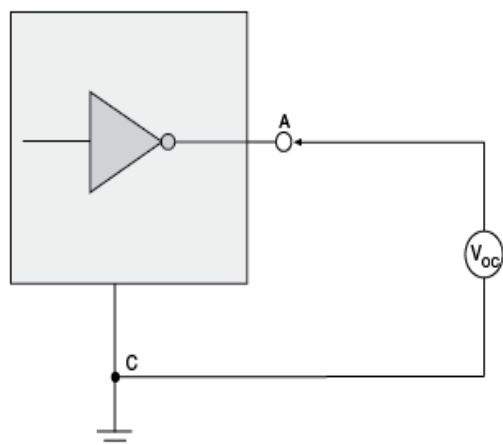


FIGURE 3. V.28 DRIVER OUTPUT LOADED VOLTAGE

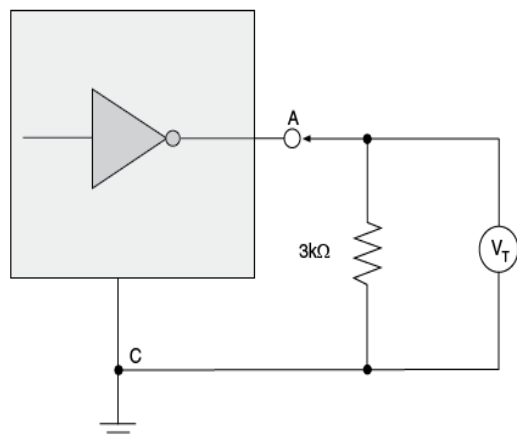


FIGURE 4. V.28 DRIVER OUTPUT SLEW RATE

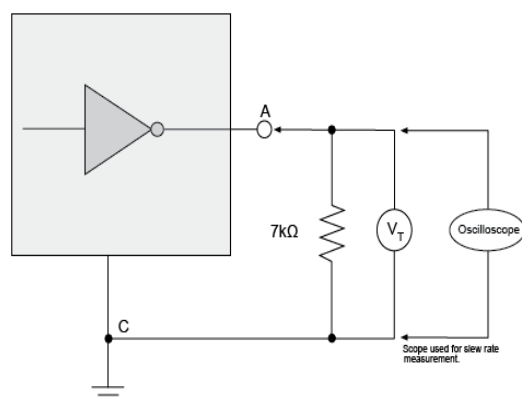


FIGURE 5. V.28 DRIVER OUTPUT SHORT CIRCUIT CURRENT

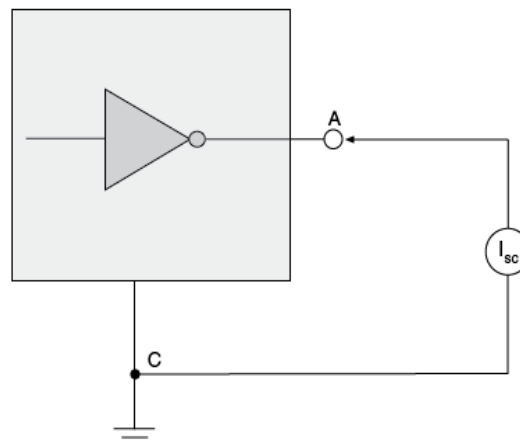


FIGURE 6. V.28 DRIVER OUTPUT POWER-OFF IMPEDANCE

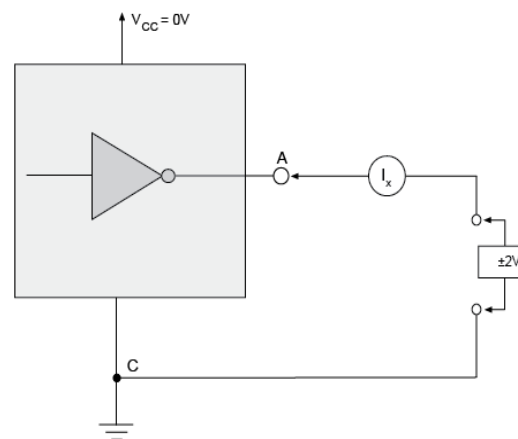


FIGURE 7. V.28 DRIVER OUTPUT RISE/FALL TIME

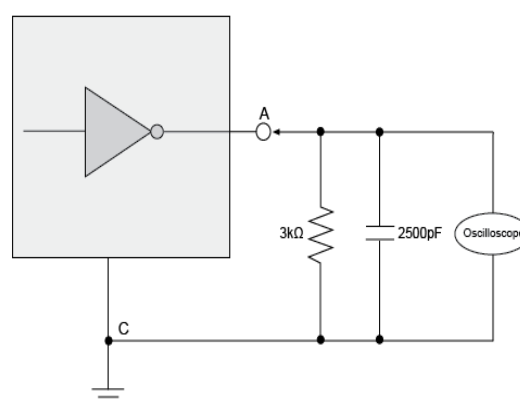


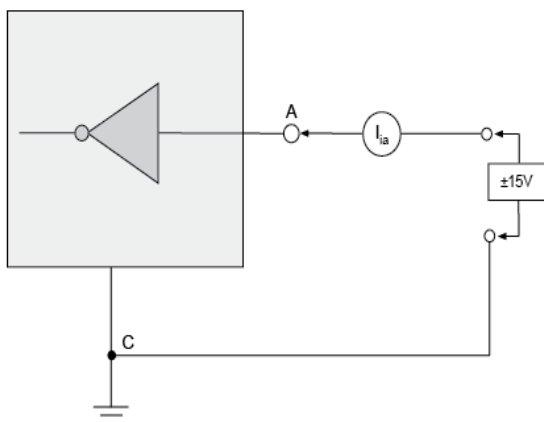
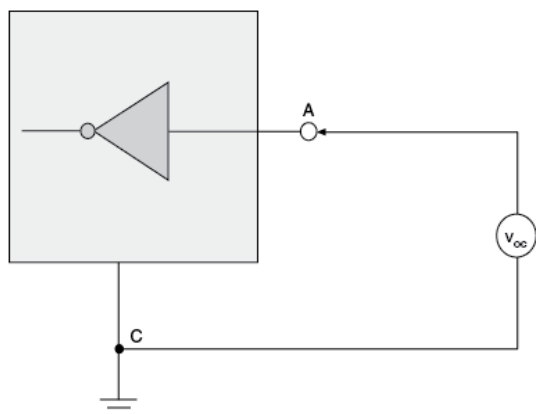
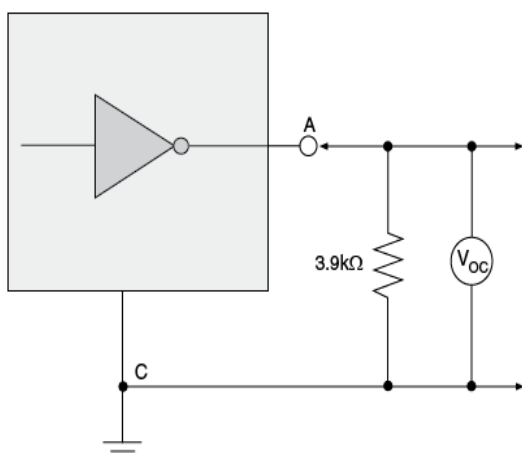
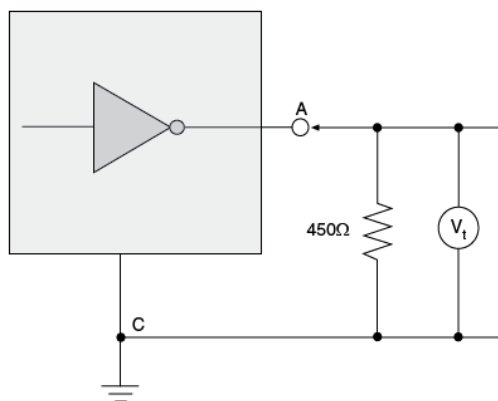
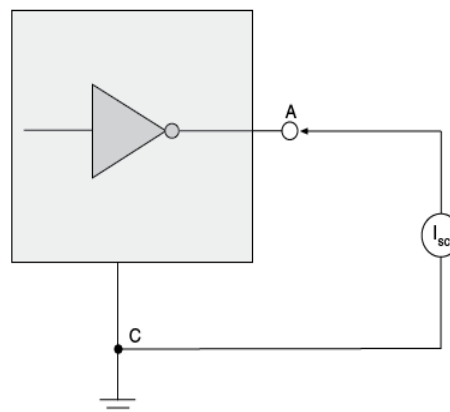
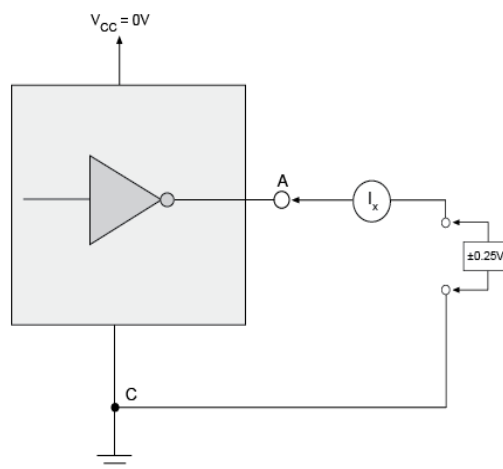
FIGURE 8. V.28 RECEIVER INPUT IMPEDANCE

FIGURE 9. V.28 RECEIVER INPUT OPEN-CIRCUIT BIAS

FIGURE 10. V.10 DRIVER OUTPUT OPEN-CIRCUIT VOLTAGE

FIGURE 11. V.10 DRIVER OUTPUT TEST TERMINATED VOLTAGE

FIGURE 12. V.10 DRIVER OUTPUT SHORT-CIRCUIT CURRENT

FIGURE 13. V.10 DRIVER OUTPUT POWER-OFF IMPEDANCE


FIGURE 14. V.10 DRIVER OUTPUT TRANSITION TIME

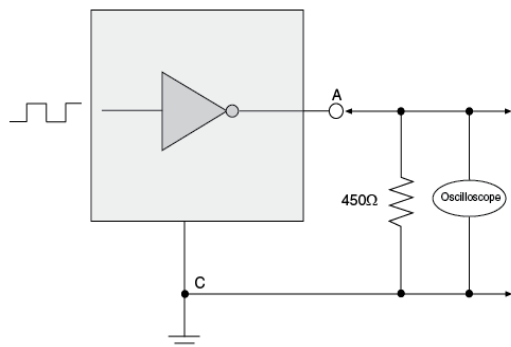


FIGURE 15. V.10 RECEIVER INPUT CURRENT

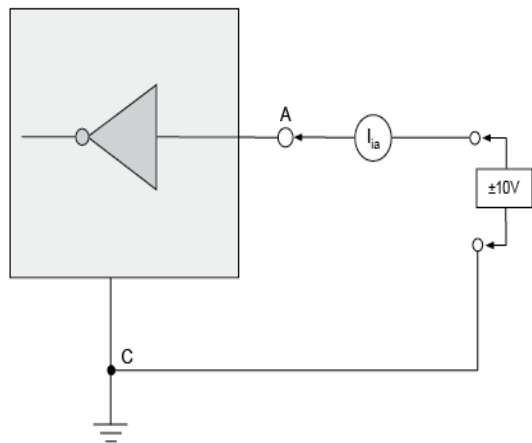


FIGURE 16. V.10 RECEIVER INPUT IV GRAPH

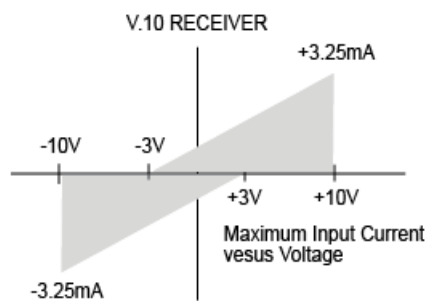


FIGURE 17. V.11 DRIVER OUTPUT TEST TERMINATED VOLTAGE

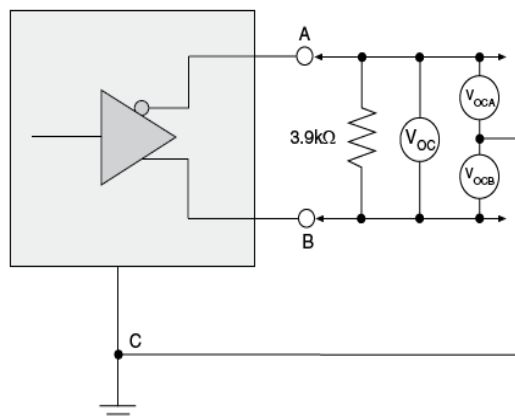


FIGURE 18. V.11 DRIVER OUTPUT TEST TERMINATED VOLTAGE

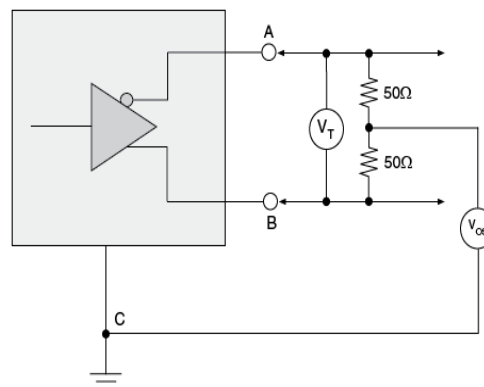


FIGURE 19. V.11 DRIVER OUTPUT SHORT-CIRCUIT CURRENT

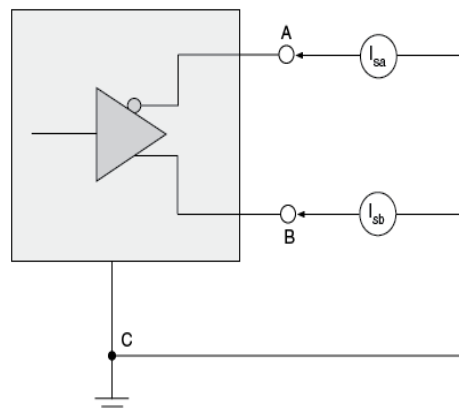


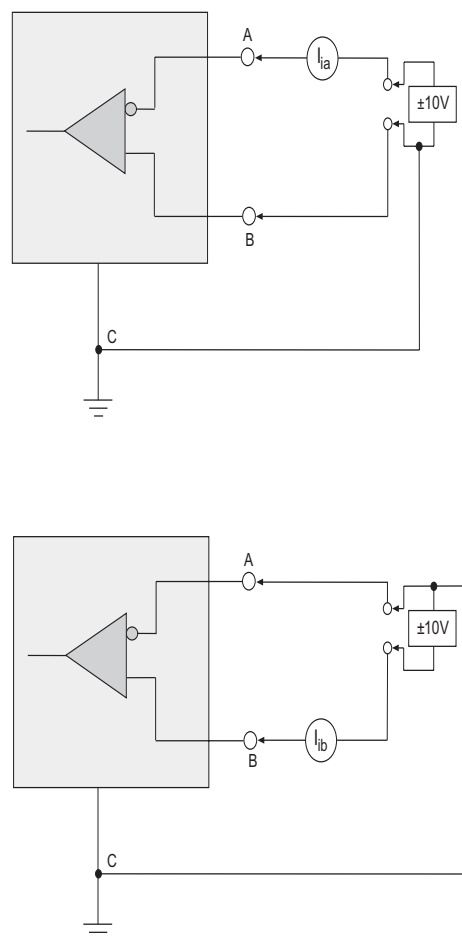
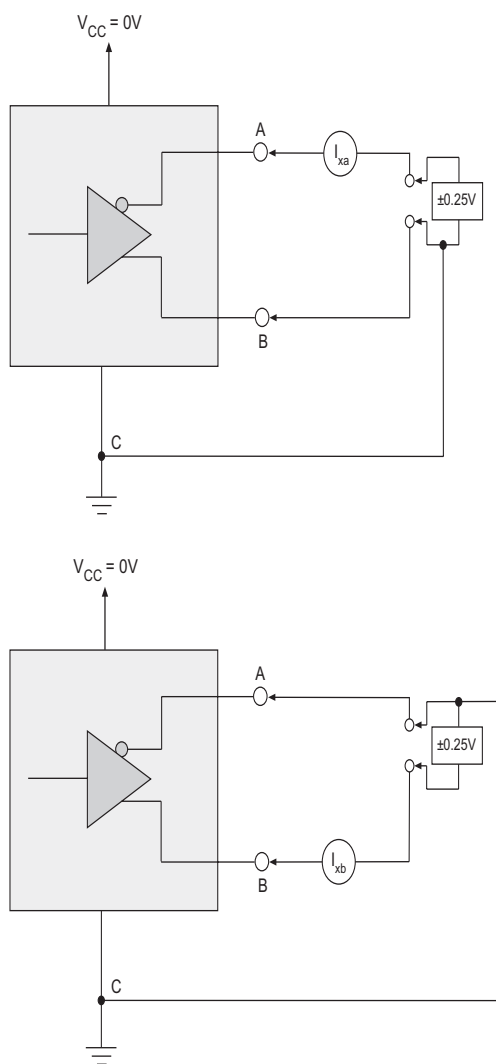
FIGURE 20. V.11 DRIVER OUTPUT POWER-OFF CURRENT
FIGURE 21. V.11 RECEIVER INPUT CURRENT


FIGURE 24. V.11 RECEIVER INPUT CURRENT WITH TERMINATION

FIGURE 22. V.11 DRIVER OUTPUT RISE/FALL TIME

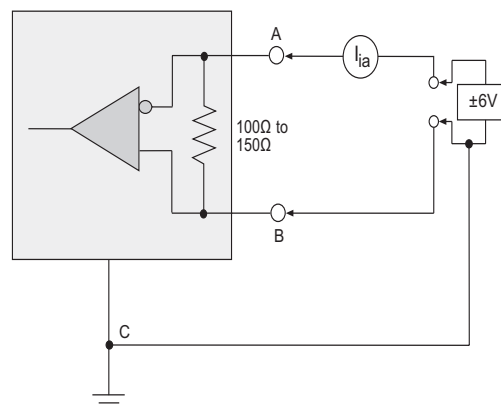
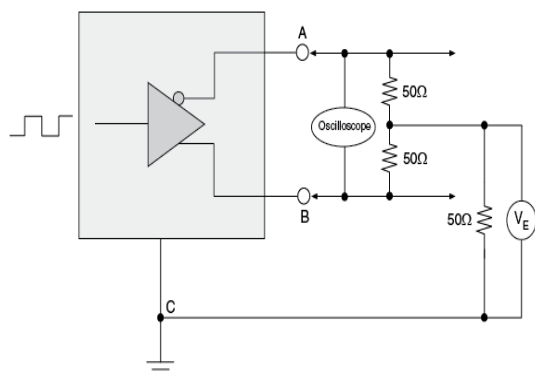


FIGURE 23. V.11 RECEIVER INPUT IV GRAPH

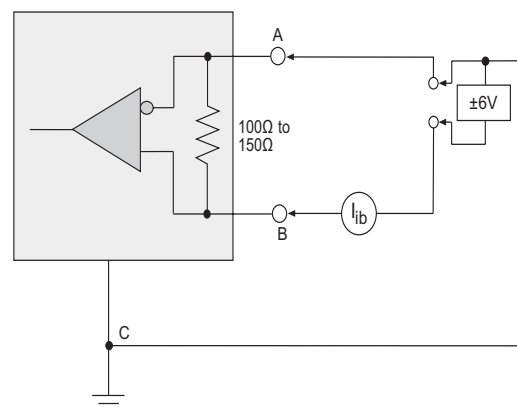
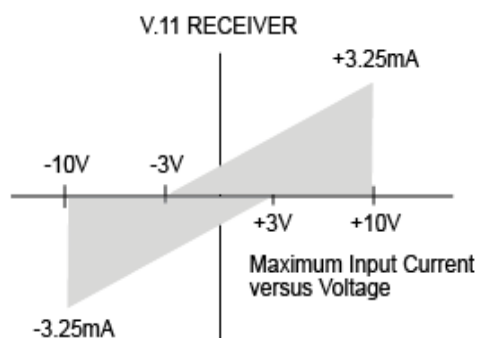


FIGURE 25. V.11 RECEIVER INPUT IV GRAPH WITH TERMINATION

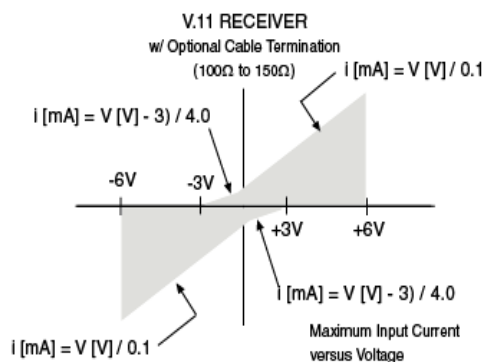


FIGURE 26. V.35 DRIVER OUTPUT TEST TERMINATED VOLTAGE

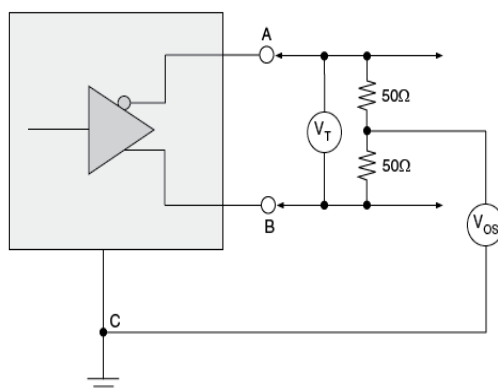


FIGURE 27. V.35 DRIVER OUTPUT SOURCE IMPEDANCE

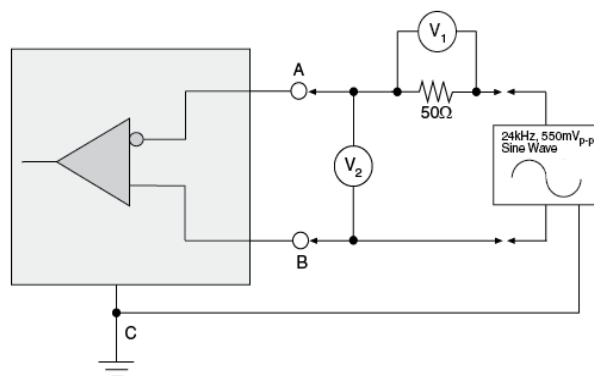


FIGURE 28. V.35 DRIVER OUTPUT SHORT-CIRCUIT IMPEDANCE

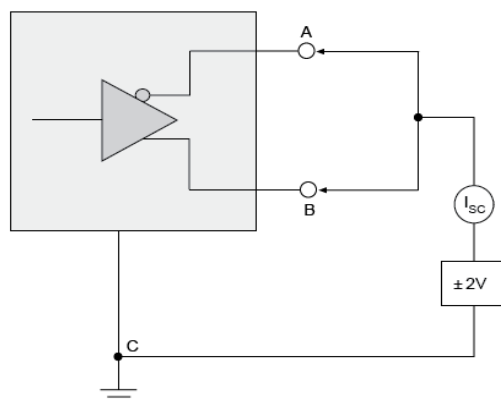


FIGURE 29. V.35 DRIVER OUTPUT RISE/FALL TIME

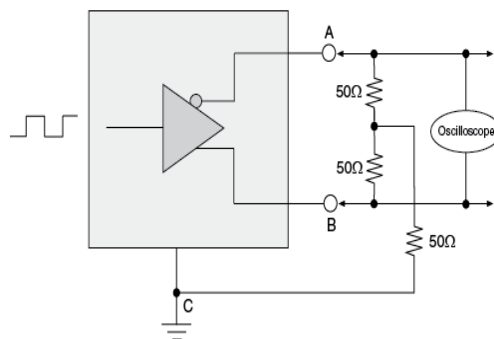


FIGURE 30. V.35 RECEIVER INPUT SOURCE IMPEDANCE

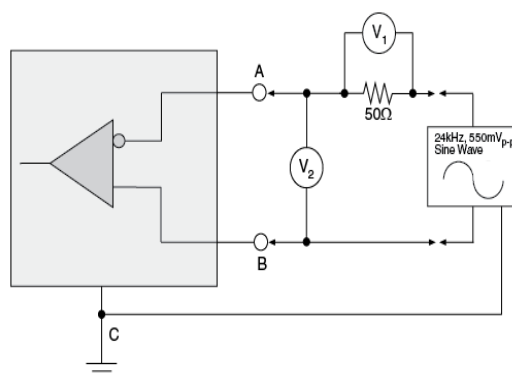


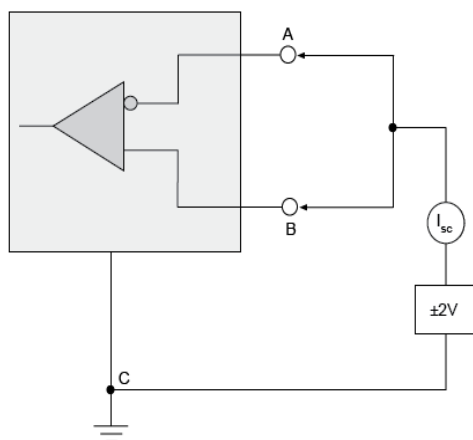
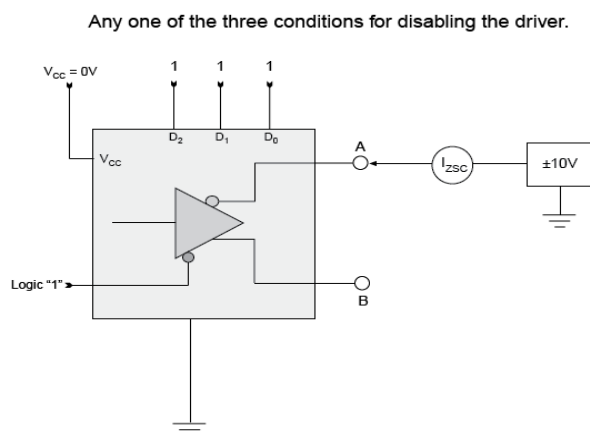
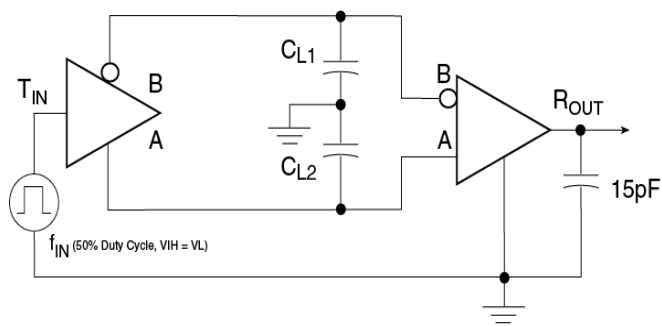
FIGURE 31. V.35 RECEIVER INPUT SHORT-CIRCUIT IMPEDANCE

FIGURE 32. DRIVER OUTPUT CURRENT LEAKAGE TEST

FIGURE 33. DRIVER / RECEIVER TIMING TEST CIRCUIT


FIGURE 34. DRIVER TIMING TEST LOAD CIRCUIT

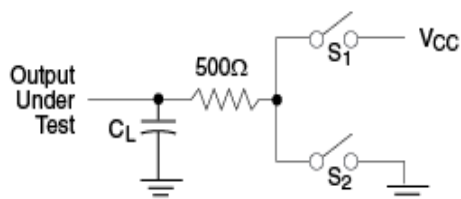


FIGURE 35. RECEIVER TIMING TEST LOAD CIRCUIT

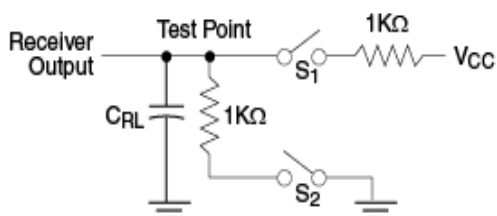


FIGURE 36. DRIVER PROPAGATION DELAYS

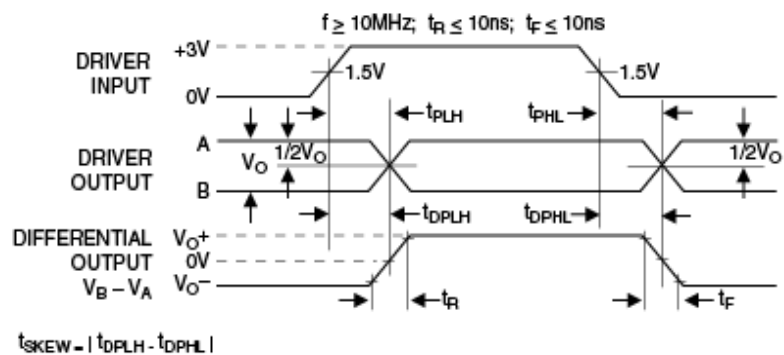


FIGURE 37. DRIVER ENABLE AND DISABLE TIMES

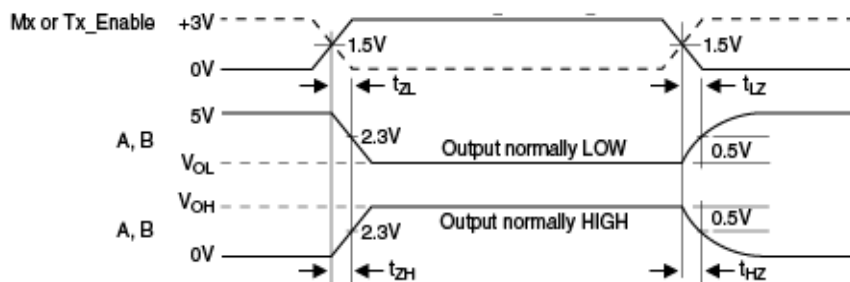


FIGURE 38. RECEIVER PROPAGATION DELAYS

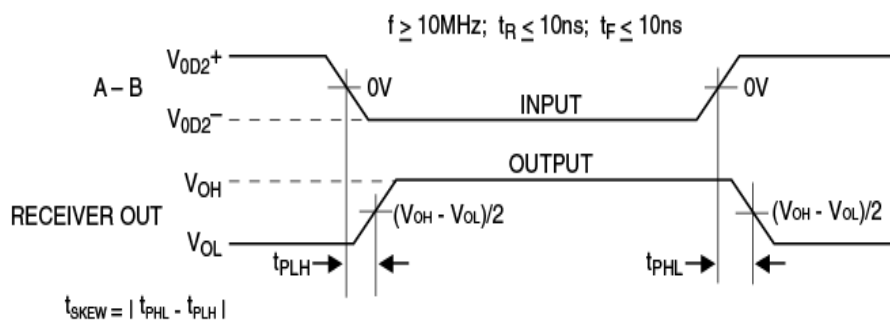


FIGURE 39. RECEIVER ENABLE AND DISABLE TIMES

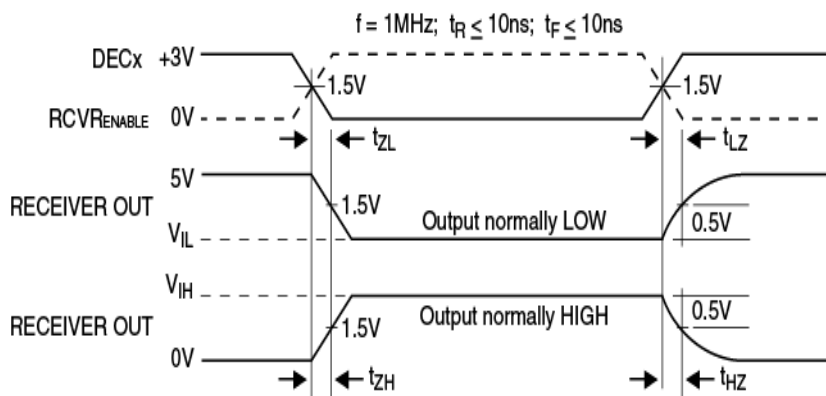


FIGURE 40. V.28 (RS-232) AND V.10 (RS-423) DRIVER ENABLE AND DISABLE TIMES

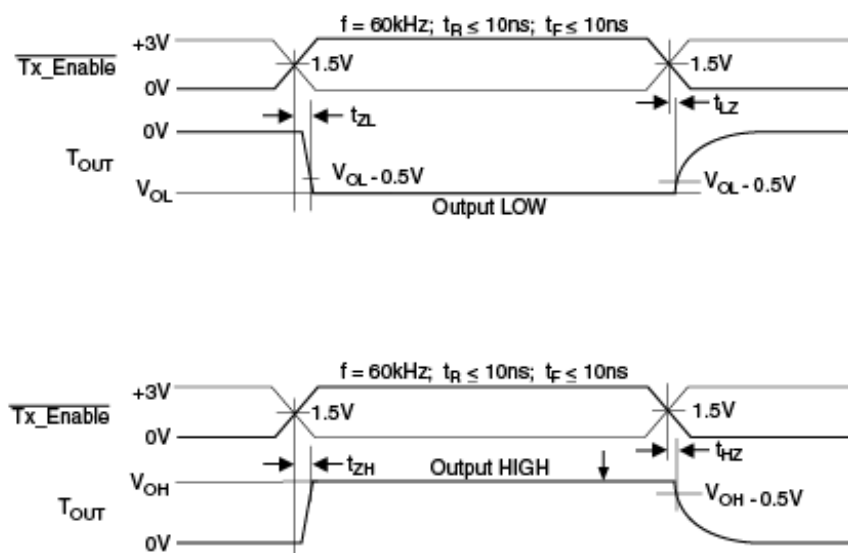


FIGURE 41. TYPICAL V.28 DRIVER OUTPUT WAVEFORM

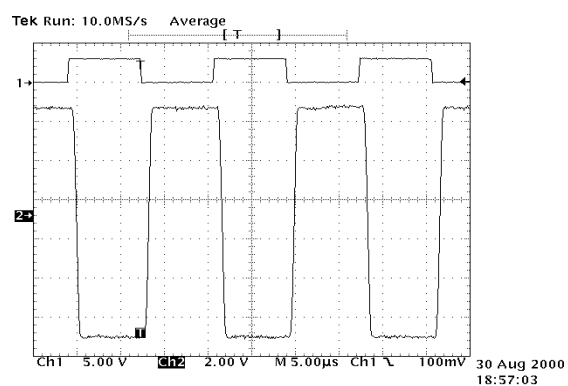


FIGURE 42. TYPICAL V.10 DRIVER OUTPUT WAVEFORM

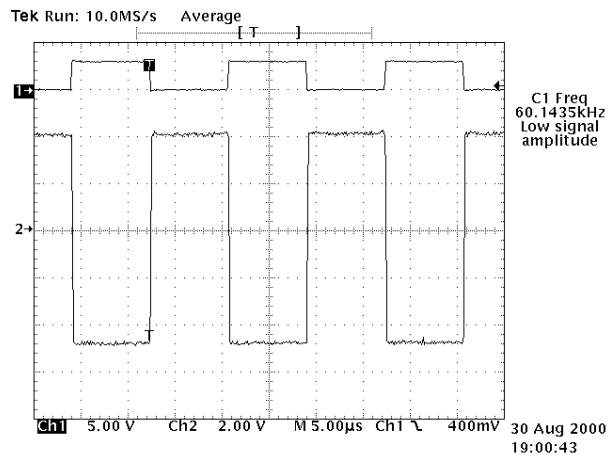


FIGURE 43. TYPICAL V.11 DRIVER OUTPUT WAVEFORM

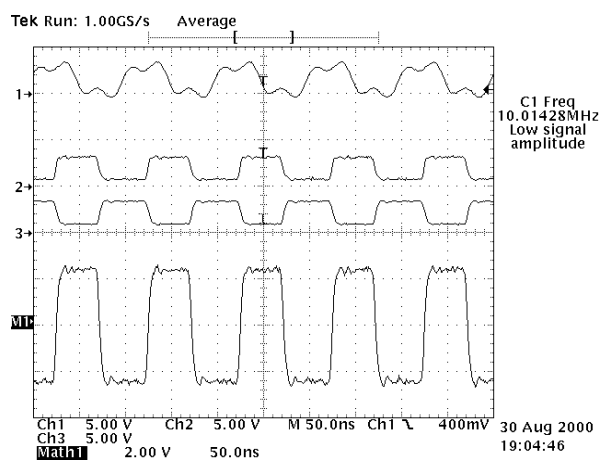


FIGURE 44. TYPICAL V.35 DRIVER OUTPUT WAVEFORM

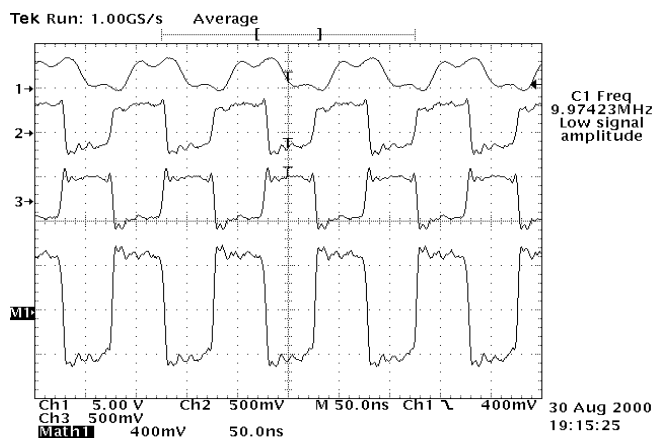


FIGURE 45. FUNCTIONAL DIAGRAM

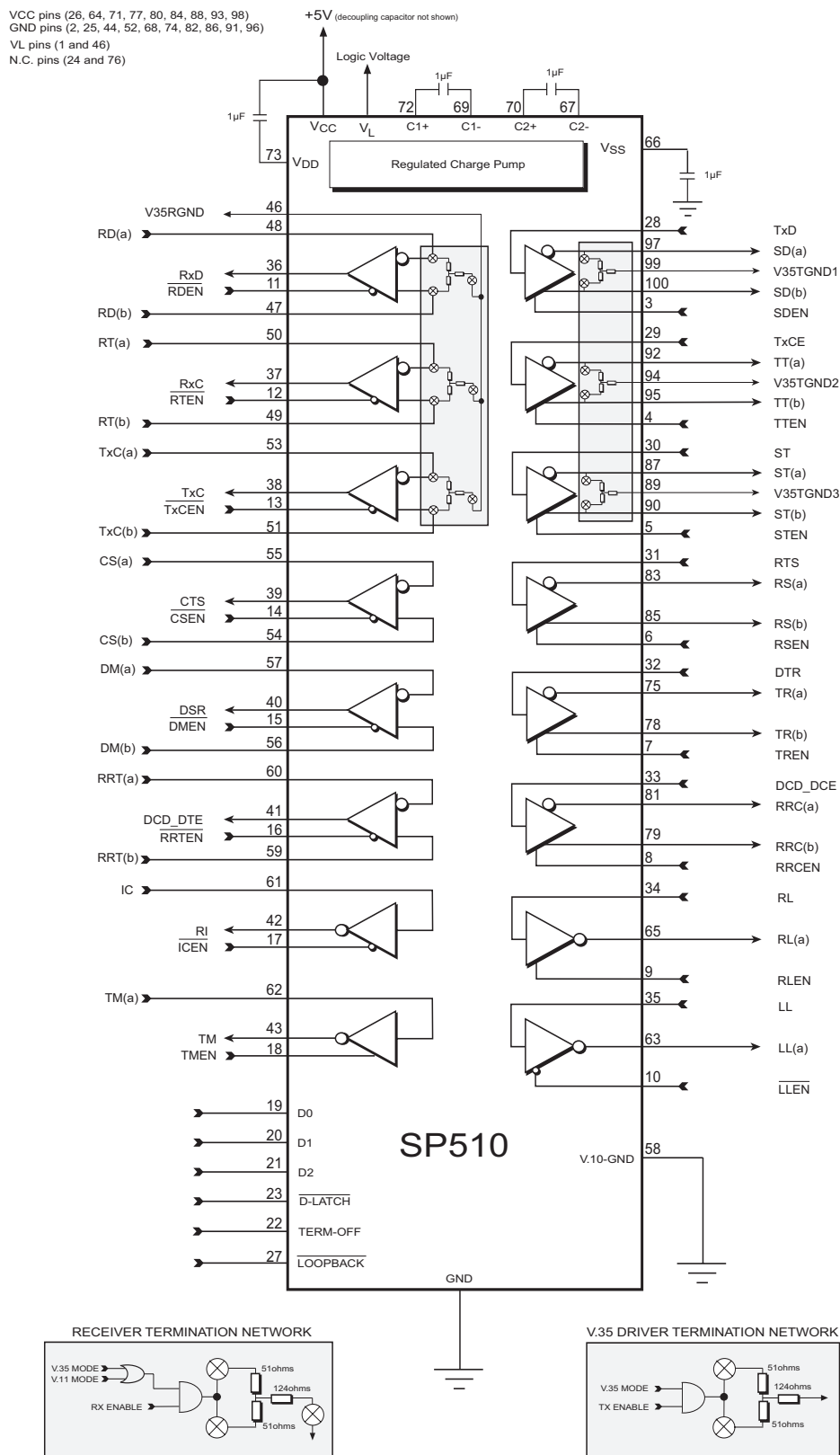


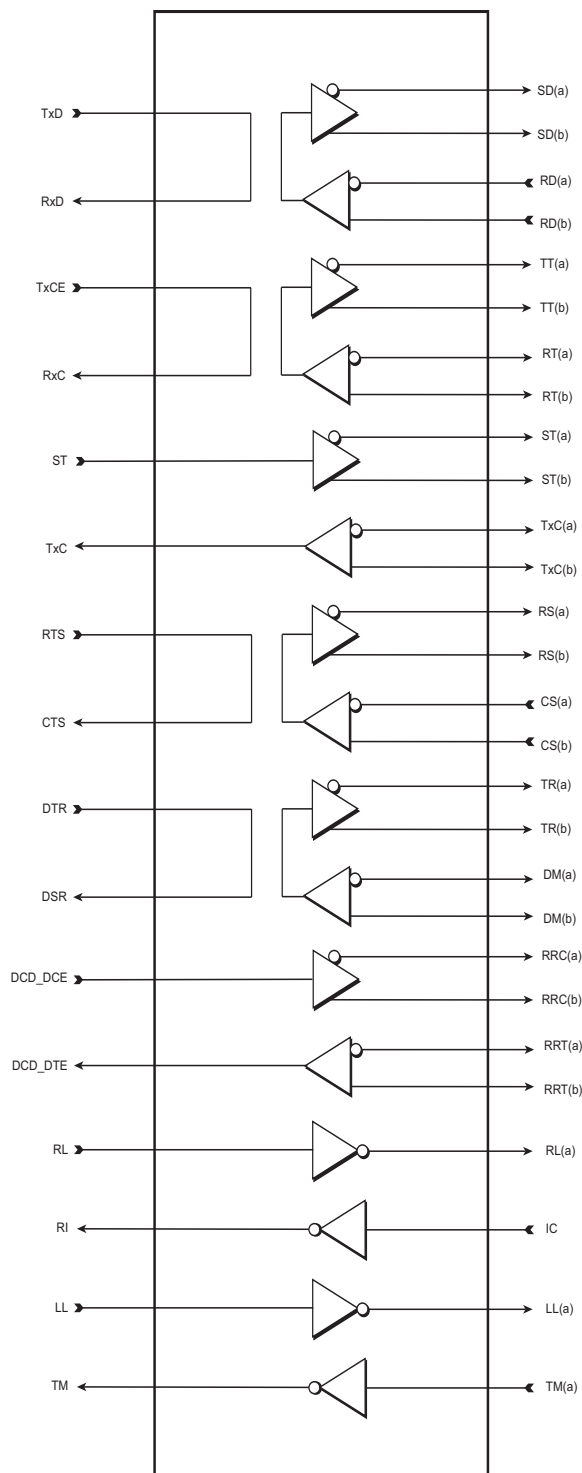
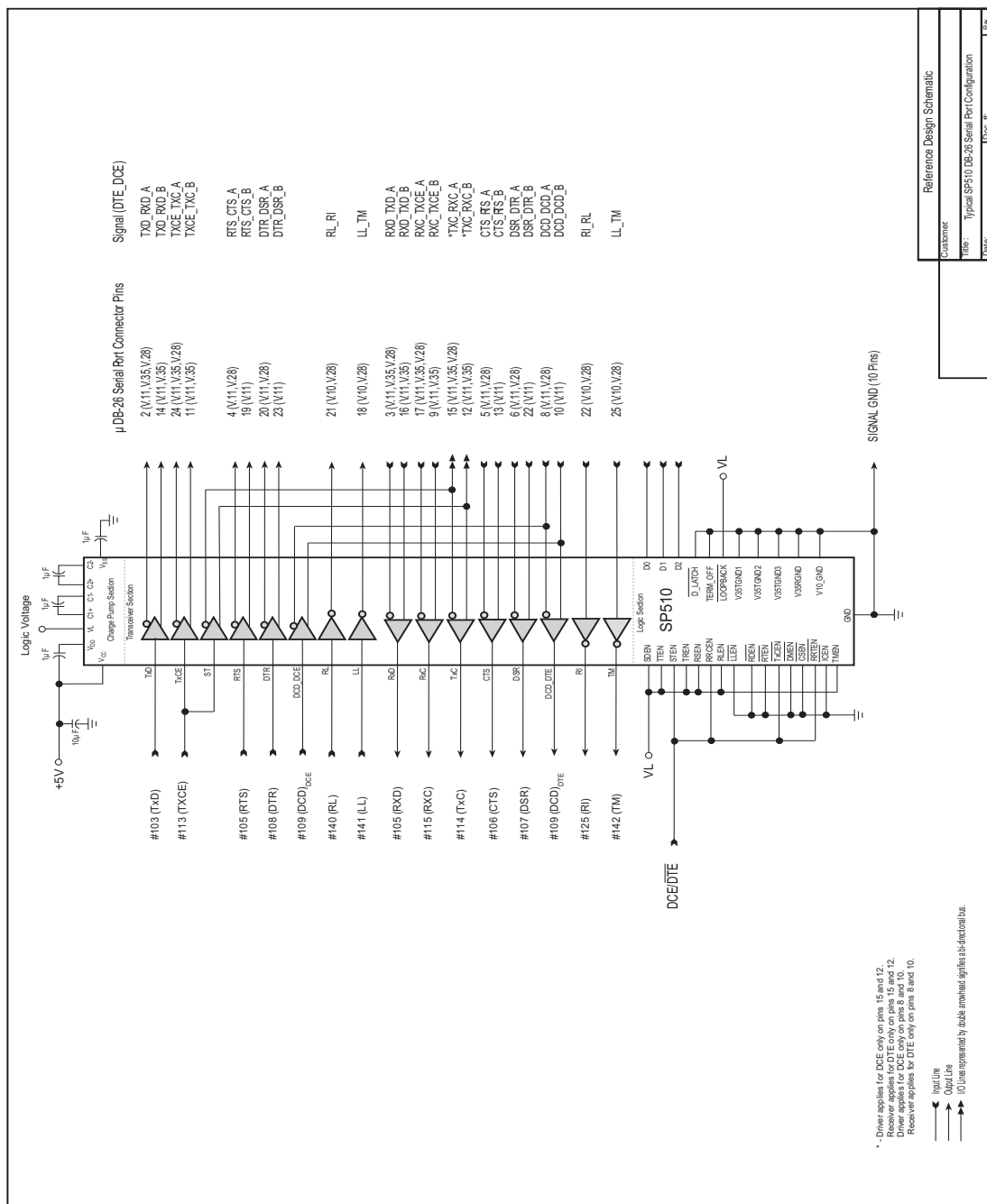
FIGURE 46. SP510 LOOPBACK PATH


FIGURE 47. TYPICAL OPERATING CONFIGURATION TO SERIAL PORT CONNECTOR WITH DCE/DTE PROGRAMMABILITY

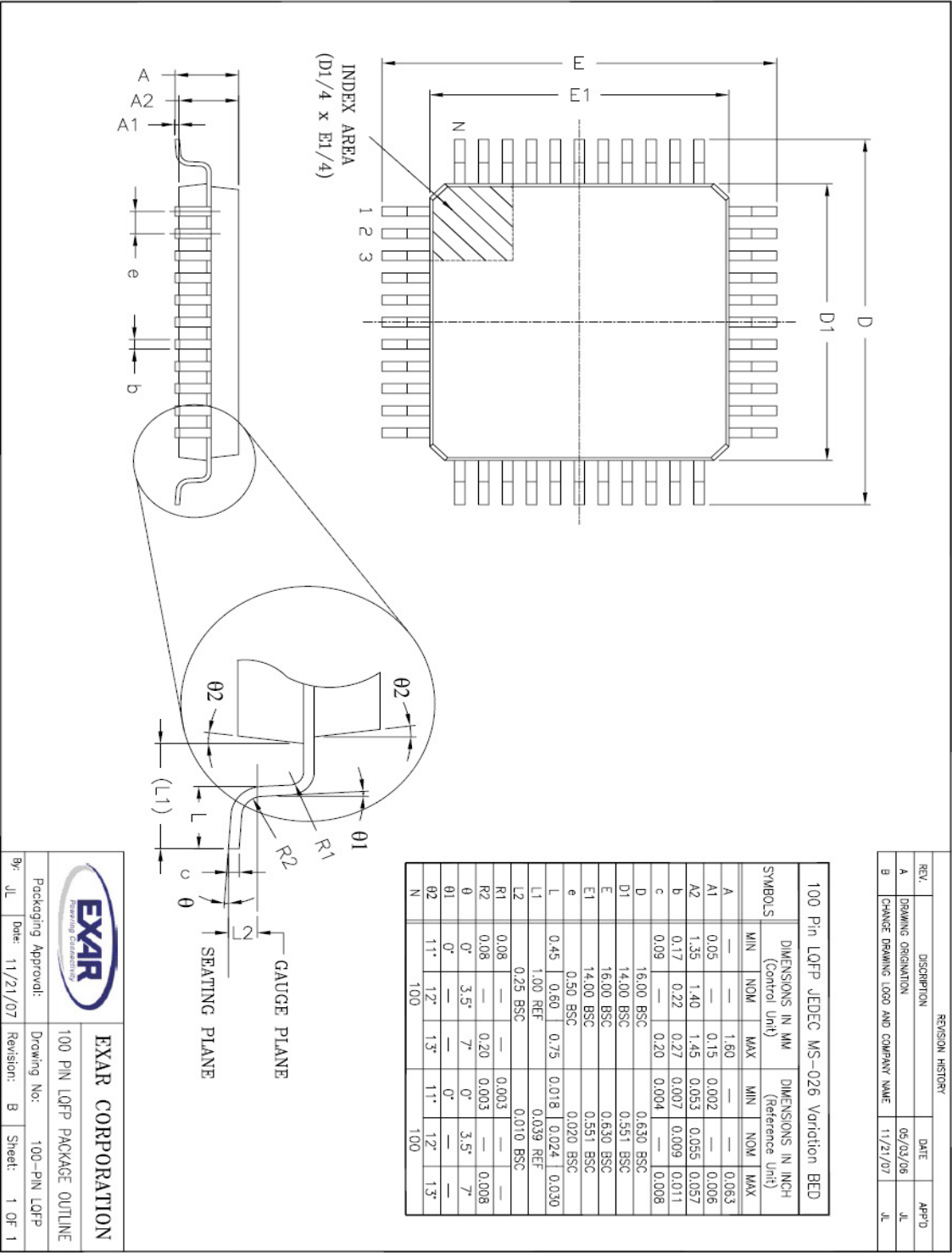


Thermal Considerations

High speed devices like the SP510 dissipate heat during normal operation. Actual power dissipation is a function of the switching frequency and loading. For maximum system performance and reliability designers should ensure sufficient air flow. Other commonly used methods for managing heat include heat sinks for higher powered devices, forced air flow (fans) and lower density board stuffing.

PCB Design

The use of multi layer printed circuit boards is recommended to provide both a better ground plane and a thermal path for heat dissipation. If possible, the ground plane should face the bottom of the package to form the thermal conduction plane. Two-sided printed circuit boards may be used where board dimensions and package count are small, but multi-layer boards allow for improved signal routing as well as improved signal integrity. A multi layer board allows the use of microstrip line techniques to provide for high speed signal interconnections. On multi-layer boards route the high speed signal lines on the inner layers.



**REVISION HISTORY**

| DATE | REVISION | DESCRIPTION |
|---------------|-----------|---|
| December 2009 | Rev 1.0.0 | Final datasheet. |
| June 2011 | Rev 1.0.1 | Correct type error on mode select tables and update ordering information. |

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