THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[b, c, f]	R_{thJA}	82	99	°C/W
Maximum Junction-to-Foot (Drain) (MOSFET)	R_{thJF}	35	45	
Maximum Junction-to-Ambient (Schottky)[b, c, g]	R_{thJA}	54	65	
Maximum Junction-to-Foot (Drain) (Schottky)	R_{thJF}	30	40	

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on FR4 board.
c. t ≤ 5 s.
d. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions for MOSFETs is 130 °C/W.
g. Maximum under steady state conditions for Schottky is 115 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS/TJ}$	I_D = - 250 µA		- 19		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)/TJ}$			2		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.45		- 1	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	ns
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 2.5 A		0.120	0.144	Ω
		V_{GS} = - 2.5 V, I_D = - 2.2 A		0.150	0.180	
		V_{GS} = - 1.8 V, I_D = - 2.0 A		0.185	0.222	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 2.5 A		18		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		276		pF
Output Capacitance	C_{oss}			60		
Reverse Transfer Capacitance	C_{rss}			43		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 5 V, I_D = - 2.5 A		4.5	6.8	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 2.5 A		4.1	6.2	
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.0		
Gate Resistance	R_g	f = 1 MHz	1.1	5.5	11	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 5 Ω I_D ≅ - 2 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		11	17	ns
Rise Time	t_r			34	51	
Turn-Off Delay Time	$t_{d(off)}$			22	33	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 5 Ω I_D ≅ - 2 A, V_{GEN} = - 5 V, R_g = 1 Ω		5	10	
Rise Time	t_r			14	21	
Turn-Off Delay Time	$t_{d(off)}$			17	26	
Fall Time	t_f			8	16	

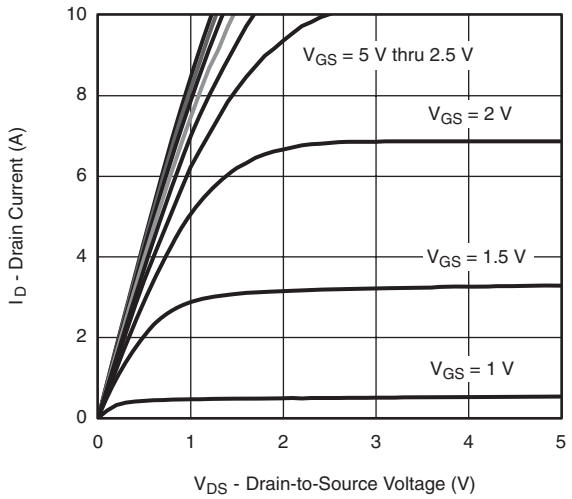
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 2.3	A
Pulse Diode Forward Current	I_{SM}				- 10	
Body Diode Voltage	V_{SD}	I_S = - 2 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 2 A dI/dt = 100 A/µs T_J = 25 °C		23	35	ns
Body Diode Reverse Recovery Charge	Q_{rr}			13	20	nC
Reverse Recovery Fall Time	t_a			10		ns
Reverse Recovery Rise Time	t_b			13		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

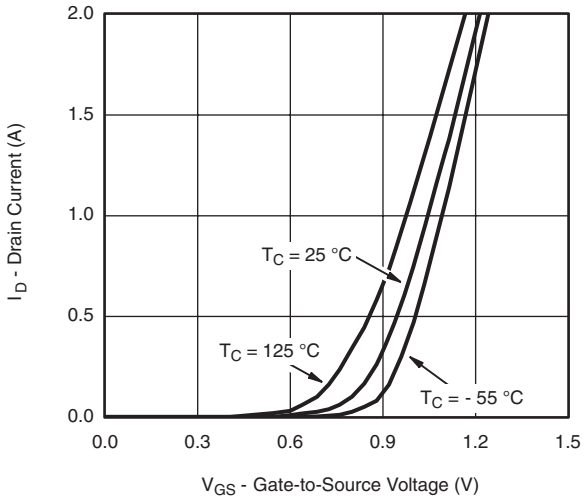
SCHOTTKY SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Forward Voltage Drop	V_F	I_F = 1 A		0.34	0.375	V
		I_F = 1 A, T_J = 125 °C		0.255	0.290	
Maximum Reverse Leakage Current	I_{rm}	V_r = 20 V		0.05	0.500	mA
		V_r = 20 V, T_J = 85 °C		2	20	
		V_r = 20 V, T_J = 125 °C		10	100	
Junction Capacitance	C_T	V_r = 10 V		90		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

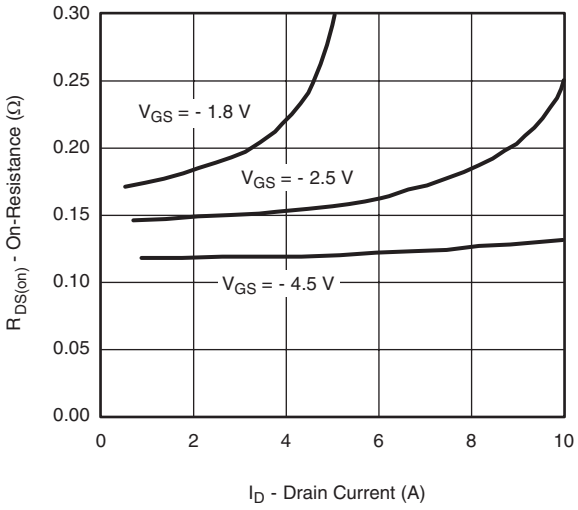


Output Characteristics

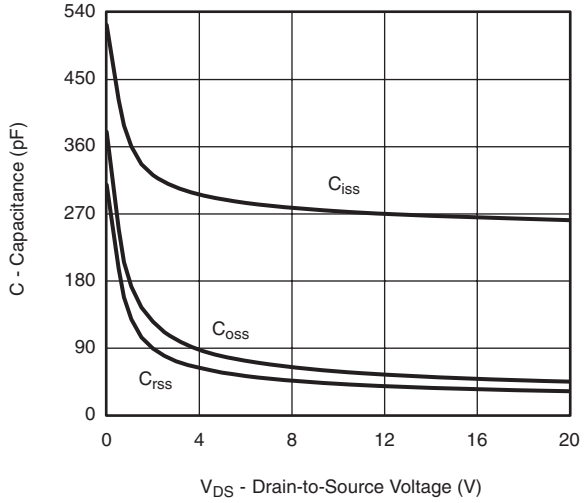


Transfer Characteristics

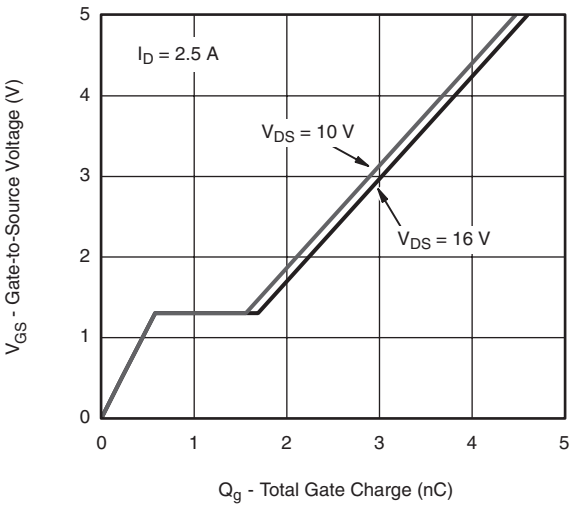
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



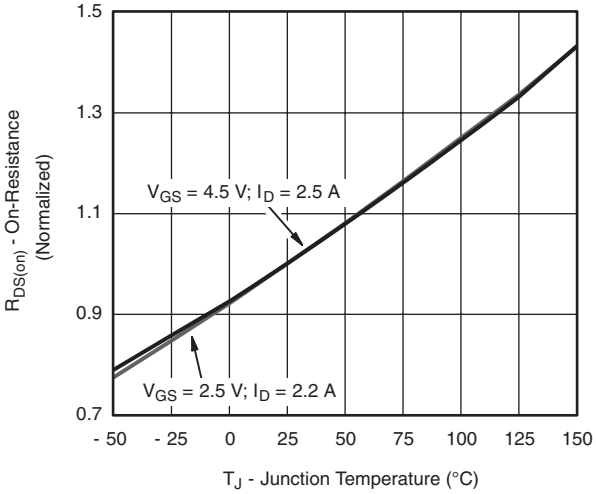
On Resistance vs. Drain Current



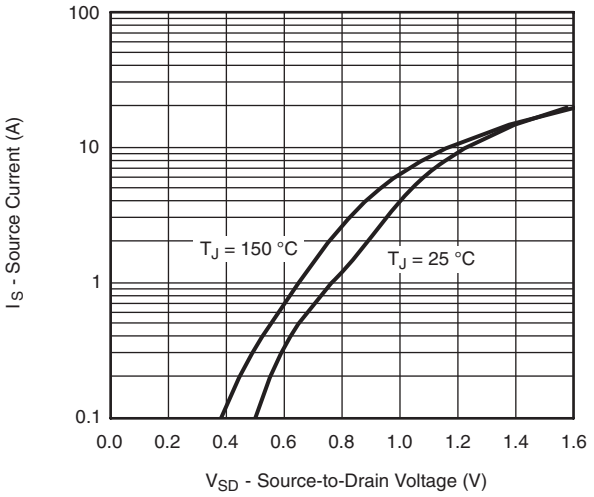
Capacitance



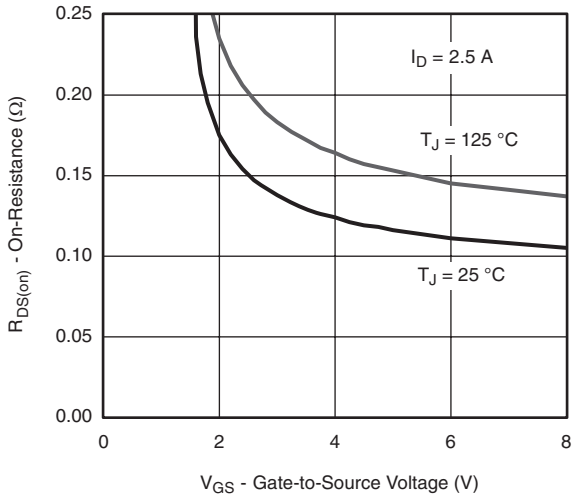
Gate Charge



On-Resistance vs. Junction Temperature

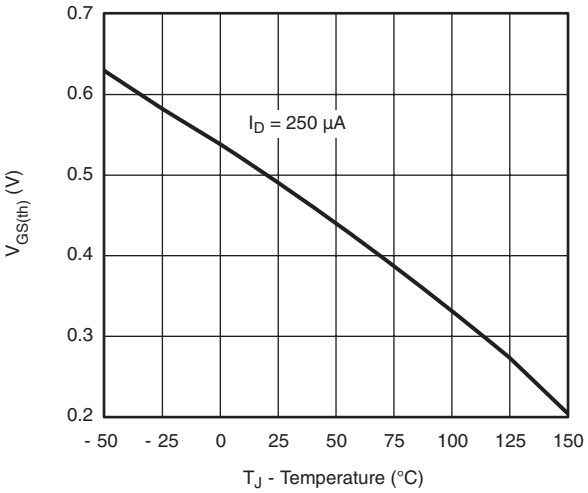


Forward Diode Voltage vs. Temp.

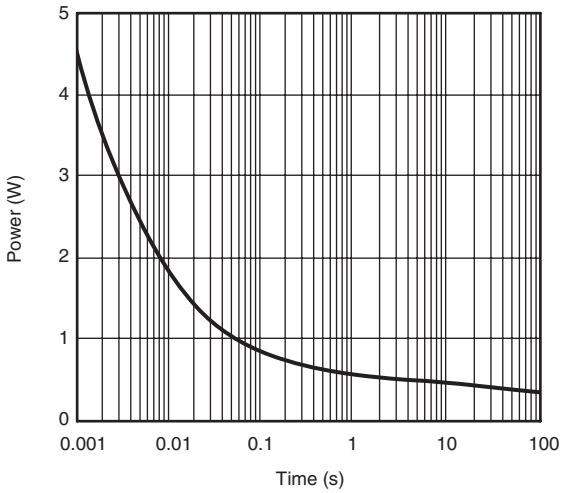


On-Resistance vs. Gate-to-Source Voltage

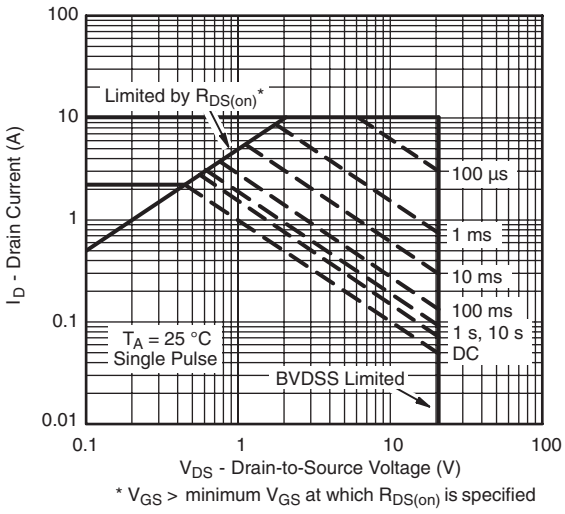
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Threshold Voltage



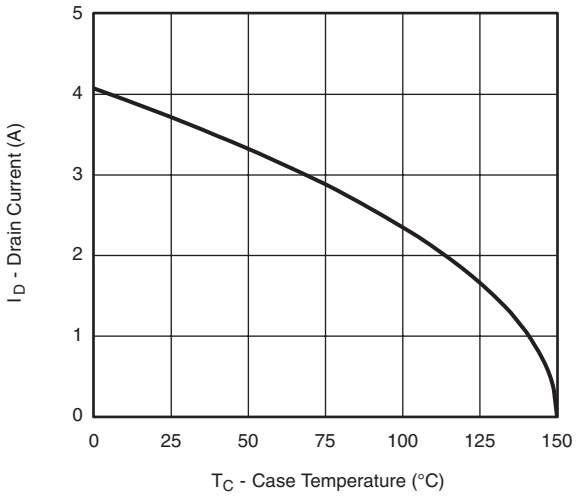
Single Pulse Power



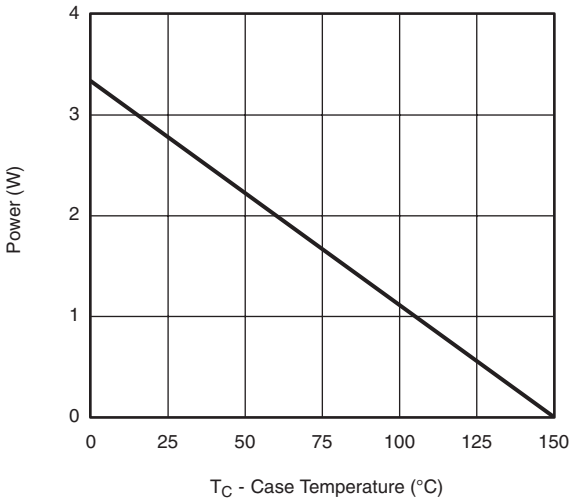
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

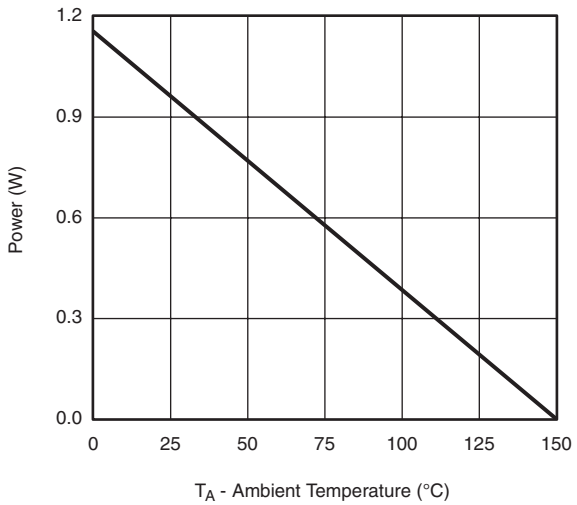
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



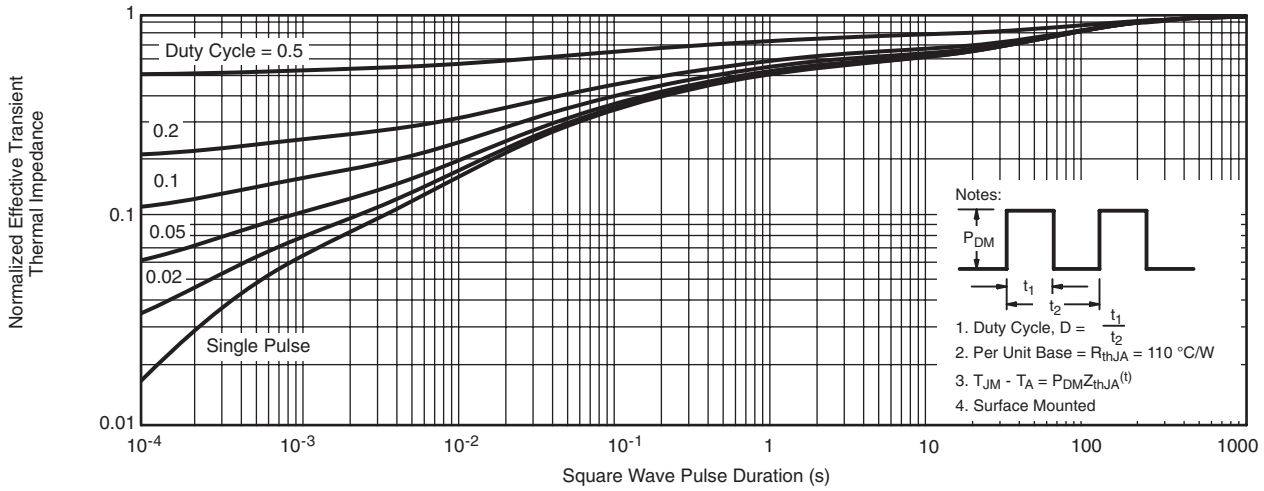
Power, Junction-to-Foot



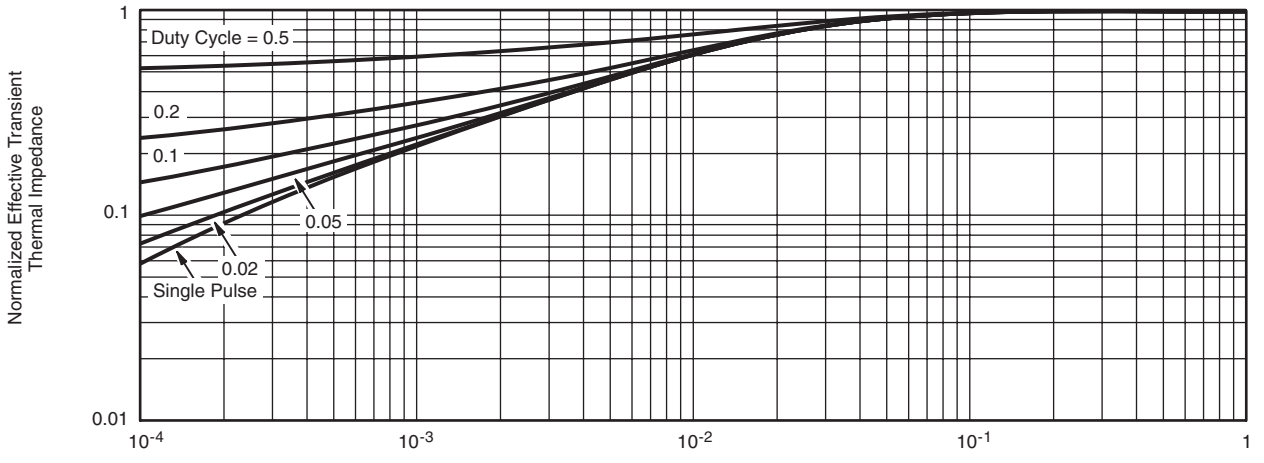
Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

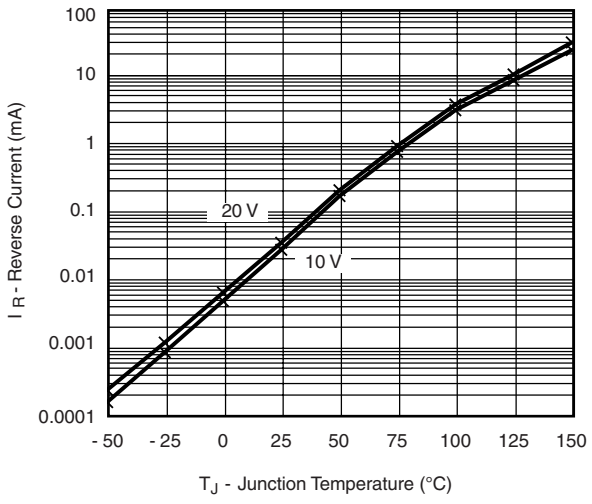


Normalized Thermal Transient Impedance, Junction-to-Ambient

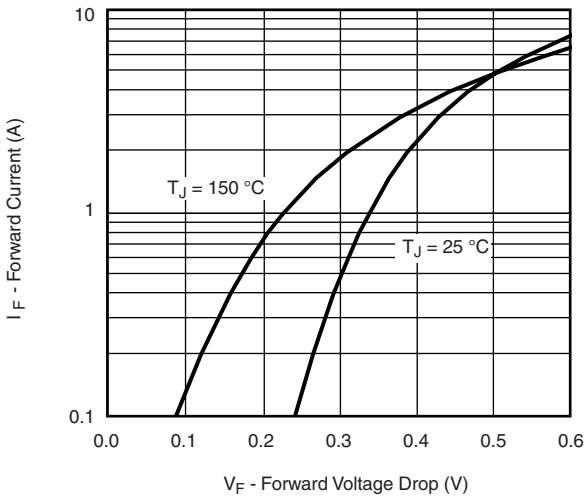


Normalized Thermal Transient Impedance, Junction-to-Foot

SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

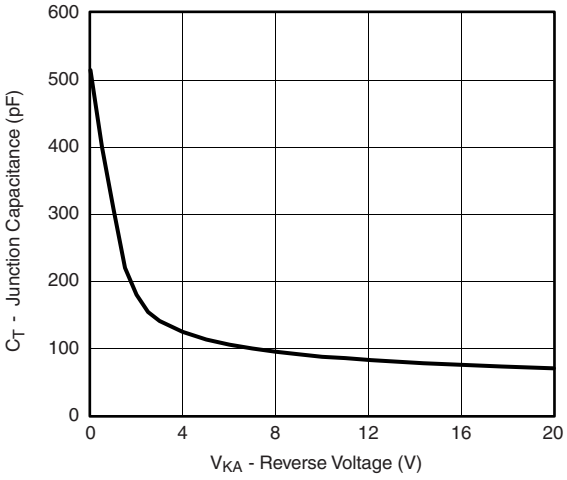


Reverse Current vs. Junction Temperature

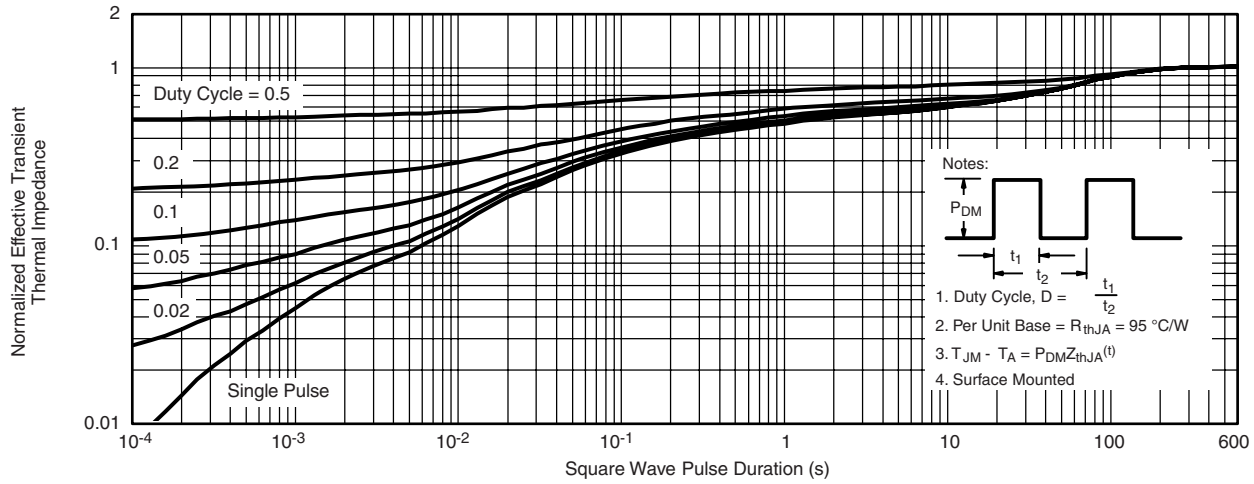


Forward Voltage Drop

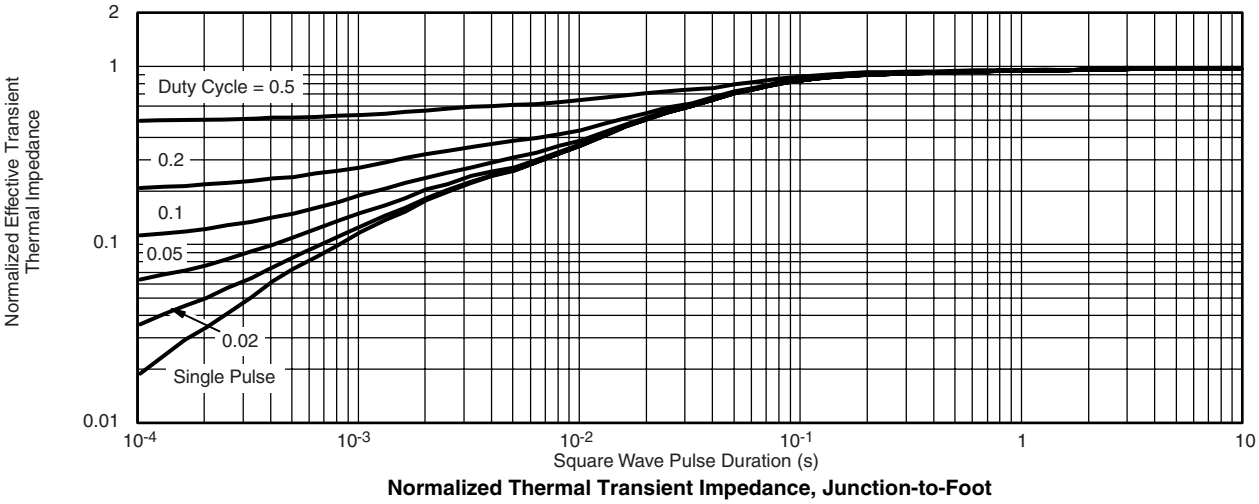
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Capacitance



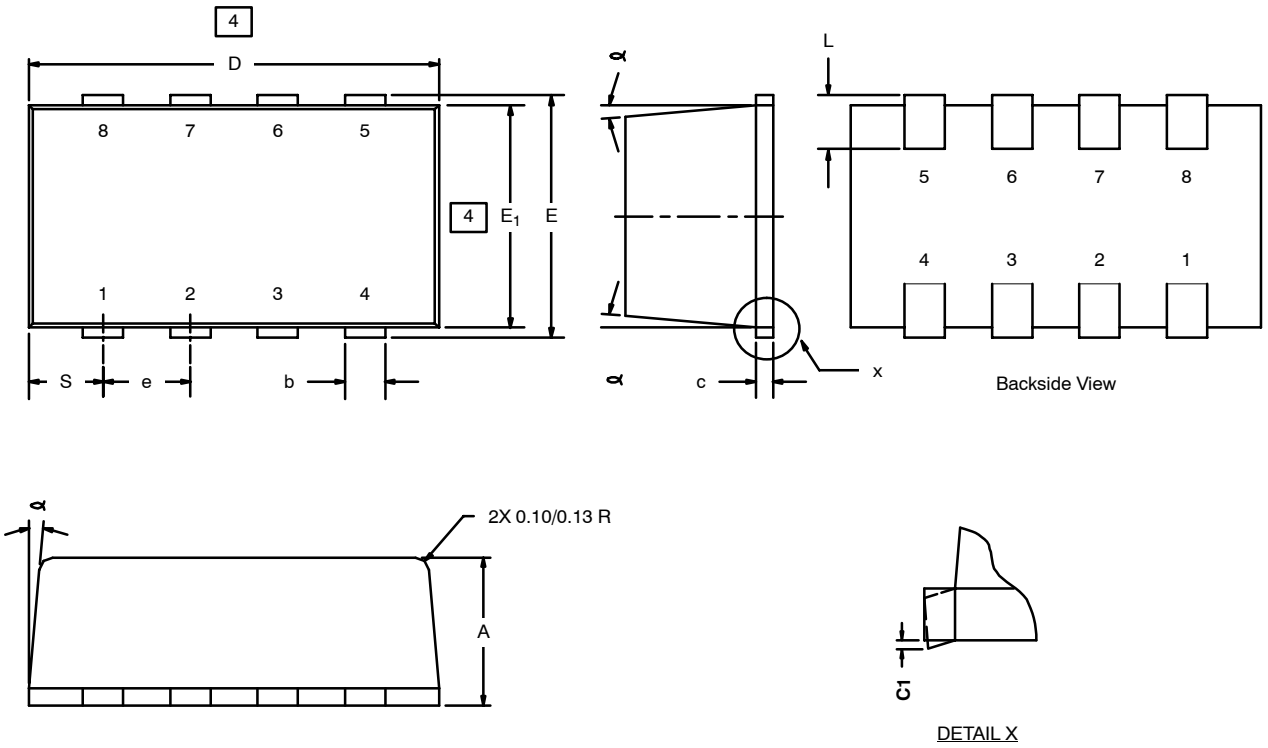
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68910.

1206-8 ChipFET®



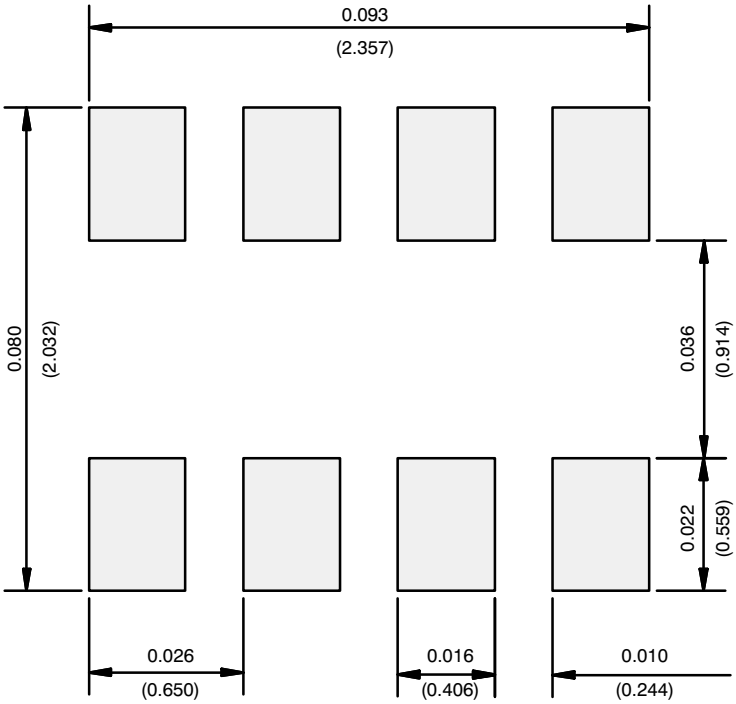
NOTES:

1. All dimensions are in millimeaters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		

ECN: C-03528—Rev. F, 19-Jan-04
DWG: 5547

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

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