# 1. Ordering Guide

**Table 1.1. Ordering Guide**

| Part Number | Package Type | Temperature |
|---|---|---|
| Si53102-A1-GM | 8-pin TDFN | Extended, –40 to 85 °C |
| Si53102-A1-GMR | 8-pin TDFN—Tape and Reel | Extended, –40 to 85 °C |
| Si53102-A2-GM | 8-pin TDFN | Extended, –40 to 85 °C |
| Si53102-A2-GMR | 8-pin TDFN—Tape and Reel | Extended, –40 to 85 °C |
| Si53102-A3-GM | 8-pin TDFN | Extended, –40 to 85 °C |
| Si53102-A3-GMR | 8-pin TDFN—Tape and Reel | Extended, –40 to 85 °C |

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# 2. Electrical Specifications

**Table 2.1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage (3.3 V Supply) | $V_{DD}$ | 3.3 V ± 10% | 2.97 | 3.3 | 3.63 | V |
| Supply Voltage (2.5 V Supply) | $V_{DD}$ | 2.5 V ± 10% | 2.25 | 2.5 | 2.75 | V |

**Table 2.2. DC Electrical Specifications**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage ($V_{DD}$ = 3.3 V) | $V_{DD}$ | 3.3 V ± 10% | 2.97 | 3.30 | 3.63 | V |
| Operating Voltage ($V_{DD}$ = 2.5 V) | $V_{DD}$ | 2.5 V ± 10% | 2.25 | 2.5 | 2.75 | V |
| Operating Supply Current | $I_{DD}$ | Full Active | — | — | 15 | mA |
| Input Pin Capacitance | $C_{IN}$ | Input Pin Capacitance | — | 3 | 5 | pF |
| Output Pin Capacitance | $C_{OUT}$ | Output Pin Capacitance | — | — | 5 | pF |

**Table 2.3. AC Electrical Specifications[1, 2, 3]**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DIFFIN at 0.7 V** | | | | | | |
| Input frequency | Fin | | 10 | 100 | 175 | MHz |
| DIFFIN and DIFFINb<br>Rising/Falling Slew Rate | $T_R$ / $T_F$ | Single ended measurement:<br>$V_{OL}$ = 0.175 to $V_{OH}$ = 0.525 V (Averaged) | 0.6 | — | 4 | V/ns |
| Differential Input High Voltage | $V_{IH}$ | | 150 | — | — | mV |
| Differential Input Low Voltage | $V_{IL}$ | | — | — | –150 | mV |
| Crossing Point Voltage at 0.7 V Swing | $V_{OX}$ | Single-ended measurement | 250 | — | 550 | mV |
| Vcross Variation Over All edges | $\Delta V_{OX}$ | Single-ended measurement | — | — | 140 | mV |
| Differential Ringback Voltage | $V_{RB}$ | | –100 | — | 100 | mV |
| Time before Ringback Allowed | $T_{STABLE}$ | | 500 | — | — | ps |
| Absolute Maximum Input Voltage | $V_{MAX}$ | | | — | 1.15 | V |
| Absolute Minimum Input Voltage | $V_{MIN}$ | | –0.3 | — | — | V |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DIFFIN and DIFFINb Duty Cycle | $T_{DC}$ | Measured at crossing point VOX | 45 | — | 55 | % |
| Rise/Fall Matching | $T_{RFM}$ | Determined as a fraction of 2 x (TR – TF)/(TR + TF) | — | — | 20 | % |
| **DIFF Clocks** | | | | | | |
| Duty Cycle | $T_{DC}$ | Measured at crossing point VOX | 45 | — | 55 | % |
| Output Skew | $T_{SKEW}$ | Measured at 0 V differential | — | — | 100 | ps |
| Frequency Accuracy | $F_{ACC}$ | All output clocks | — | — | 100 | ppm |
| Slew Rate | $t_{r/f2}$ | Measured differentially from ±150 mV | 0.6 | — | 4.0 | V/ns |
| PCIe Gen 1 Pk-Pk Additive Jitter | $Pk\text{-}Pk_{GEN1}$ | PCIe Gen 1 Si53102-A1 | — | — | 10 | ps |
| PCIe Gen 2 Additive Phase Jitter | $RMS_{GEN2}$ | 10 kHz < F < 1.5 MHz, Si53102-A2 | — | — | 0.50 | ps |
| PCIe Gen 2 Additive Phase Jitter | $RMS_{GEN2}$ | 1.5 MHz < F < Nyquist, Si53102-A2 | — | — | 0.50 | ps |
| PCIe Gen 3 Additive Phase Jitter | $RMS_{GEN3}$ | Includes PLL BW 2–4 MHz, CDR = 10 MHz, Si53102-A3, VDD=3.3 V | — | — | 0.22 | ps |
| | | Includes PLL BW 2–4 MHz, CDR = 10 MHz, Si53102-A3, VDD=2.5V | — | — | 0.25 | ps |
| PCIe Gen 4 Additive Phase Jitter | $RMS_{GEN4}$ | PCIe Gen4, VDD=3.3V | — | — | 0.22 | ps |
| | | PCIe Gen4, VDD=2.5V | | | 0.25 | ps |
| Crossing Point Voltage at 0.7 V Swing | $V_{OX}$ | VDD = 3.3 V | 300 | — | 550 | mV |
| | | VDD = 2.5 V | 200 | — | 550 | mV |
| **Enable/Disable and Setup** | | | | | | |
| Clock Stabilization from Powerup | $T_{STABLE}$ | Power up to first output | — | — | 3.0 | ms |

**Note:**

1. Visit www.pcisig.com for complete PCIe specifications
2. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
3. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

**Table 2.4. Thermal Conditions**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature, Storage | $T_S$ | Non-functional | –65 | | 150 | °C |
| Temperature, Operating Ambient | $T_A$ | Functional | –40 | | 85 | °C |
| Temperature, Junction | $T_J$ | Functional | — | | 150 | °C |
| Dissipation, Junction to Case | $\theta_{JC}$ | JEDEC (JESD 51) | — | | 38.3 | °C/W |
| Dissipation, Junction to Ambient | $\theta_{JA}$ | JEDEC (JESD 51) | — | | 90.4 | °C/W |

**Table 2.5. Absolute Maximum Conditions**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Main Supply Voltage | $V_{DD\_3.3V}$ | | — | | 4.6 | V |
| Input Voltage | $V_{IN}$ | Relative to $V_{SS}$ | –0.5 | | 4.6 | $V_{DC}$ |
| ESD Protection (Human Body Model) | $ESD_{HBM}$ | JEDEC (JESD 22-A114) | 2000 | | — | V |
| Flammability Rating | UL-94 | UL (Class) | | V–0 | | |

## 3. Test and Measurement Setup

The following figures show the test load configurations for the differential clock signals.

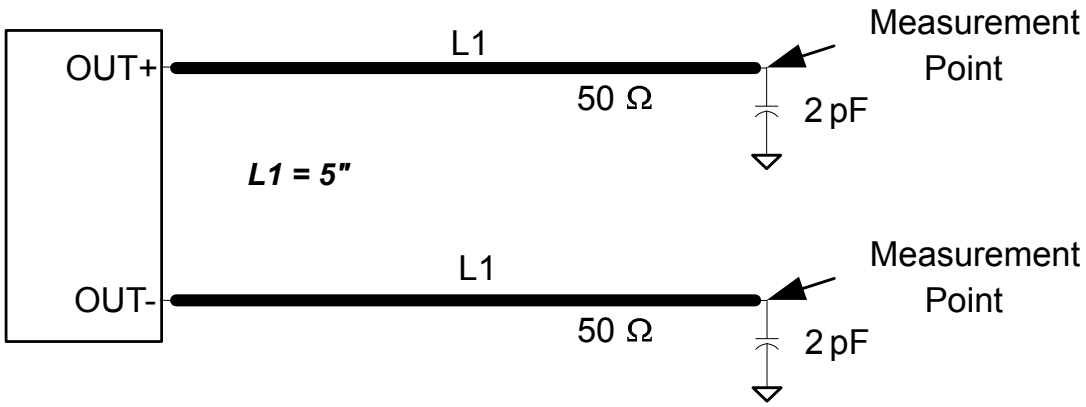


**Figure 3.1. 0.7 V Differential Load Configuration**

The outputs from this device can also support LVDS, LVPECL, or CML differential signaling levels using alternative termination. For recommendations on how to achieve this, see "AN781: Alternative Output Termination for Si5211x, Si5213x, Si5214x, Si5216x, Si5310x, Si5311x, and Si5315x PCIe Clock Generator and Buffer Families.

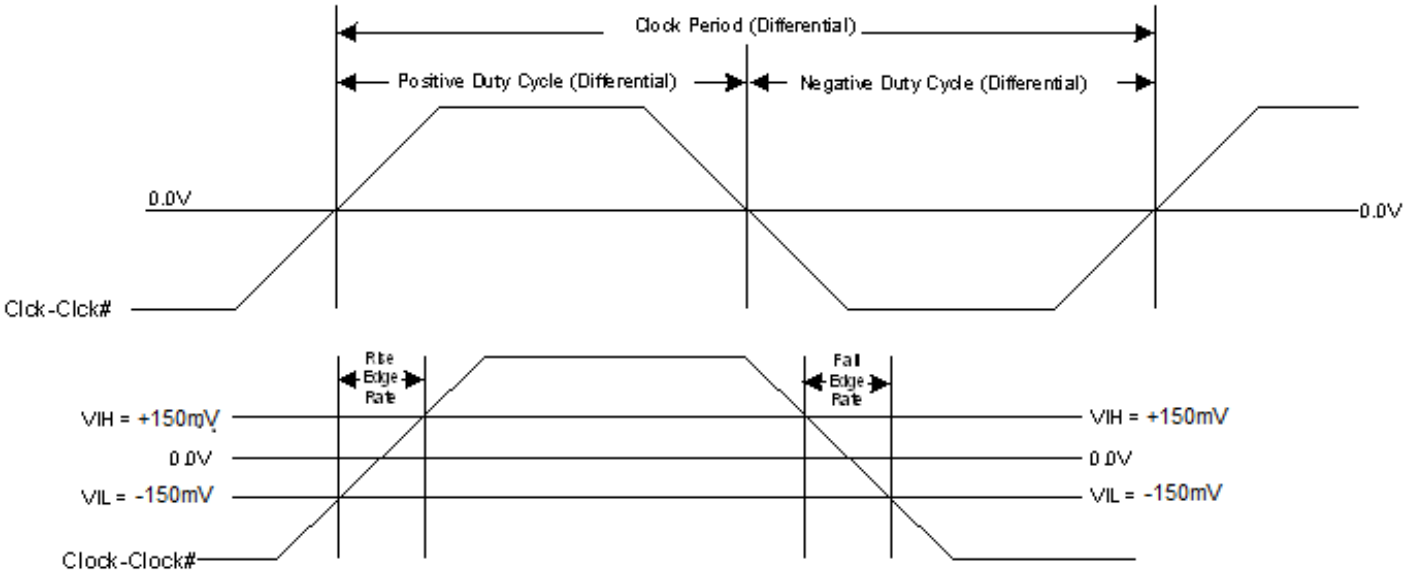


**Figure 3.2. Differential Measurement for Differential Output Signals (AC Parameters Measurement)**

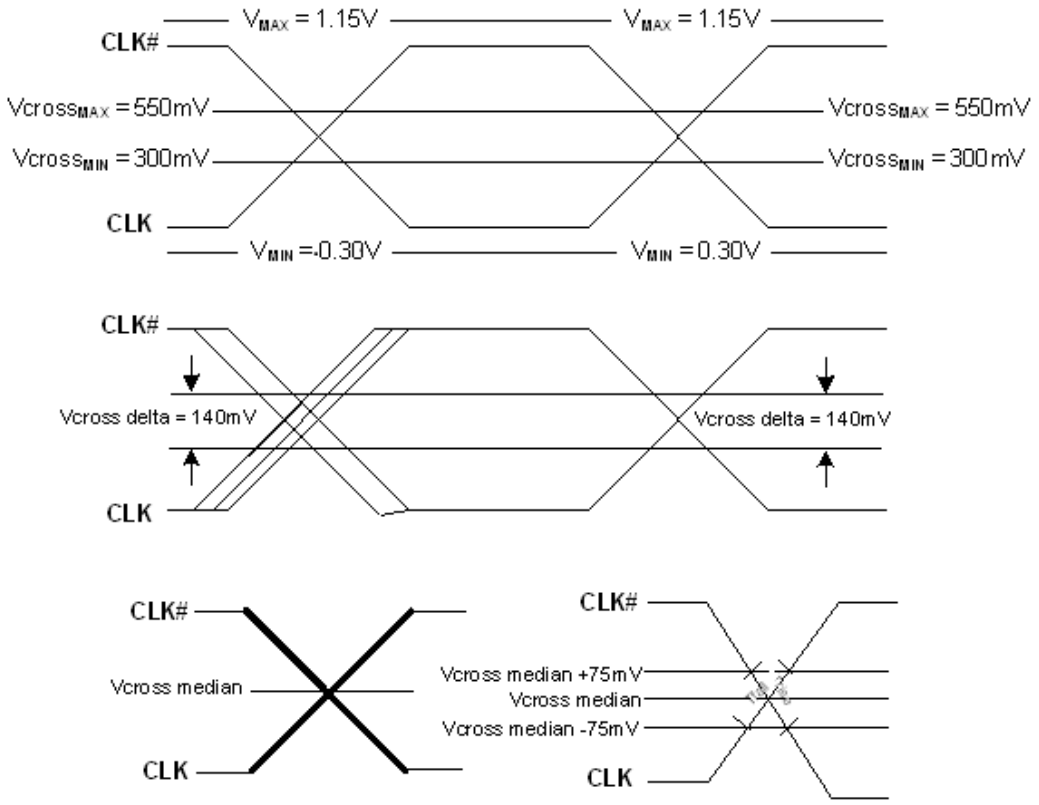


**Figure 3.3. Single-Ended Measurement for Differential Output Signals (AC Parameters Measurement)**

## 4. Recommended Design Guideline

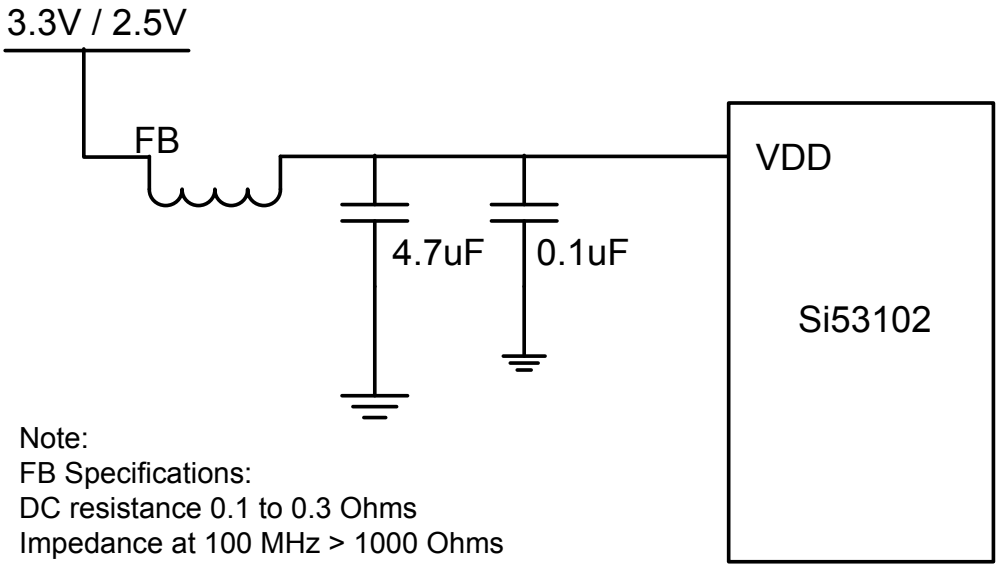


**Figure 4.1. Recommended Application Schematic**

## 5. Pin Descriptions

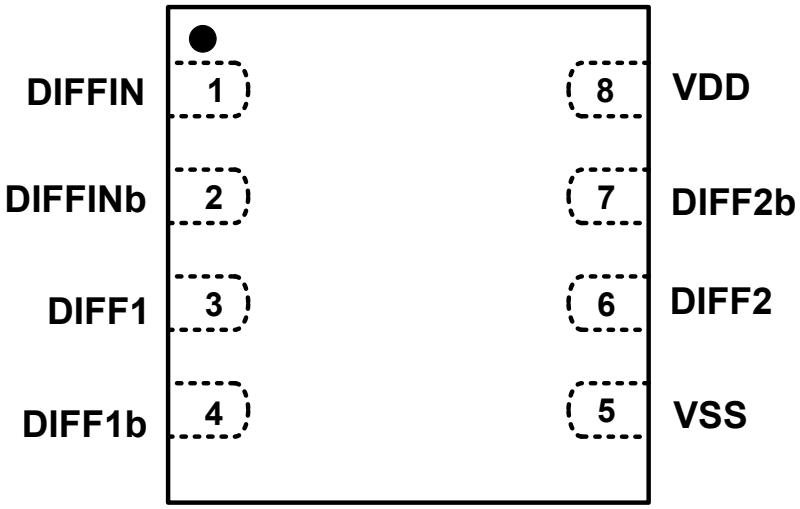


**Figure 5.1. 8-Pin TDFN**

**Table 5.1. Si53102-Ax-GM 8-Pin TDFN Descriptions**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | DIFFIN | O, DIF | 0.7 V, 100 MHz differentials clock input |
| 2 | DIFFINb | O, DIF | 0.7 V, 100 MHz differentials clock input |
| 3 | DIFF1 | O, DIF | 0.7 V, 100 MHz differential clock output |
| 4 | DIFF1b | O, DIF | 0.7 V, 100 MHz differential clock output |
| 5 | GND | GND | Ground |
| 6 | DIFF2 | O, DIF | 0.7 V, 100 MHz differential clock output |
| 7 | DIFF2b | O, DIF | 0.7 V, 100 MHz differential clock output |
| 8 | VDD | PWR | 2.5 V or 3.3 V Power supply |

## 6. Package Outline

The figure below illustrates the package details for the Si53102-A1-A2-A3 in an 8-Pin TDFN package. The table lists the values for the dimensions shown in the illustration.

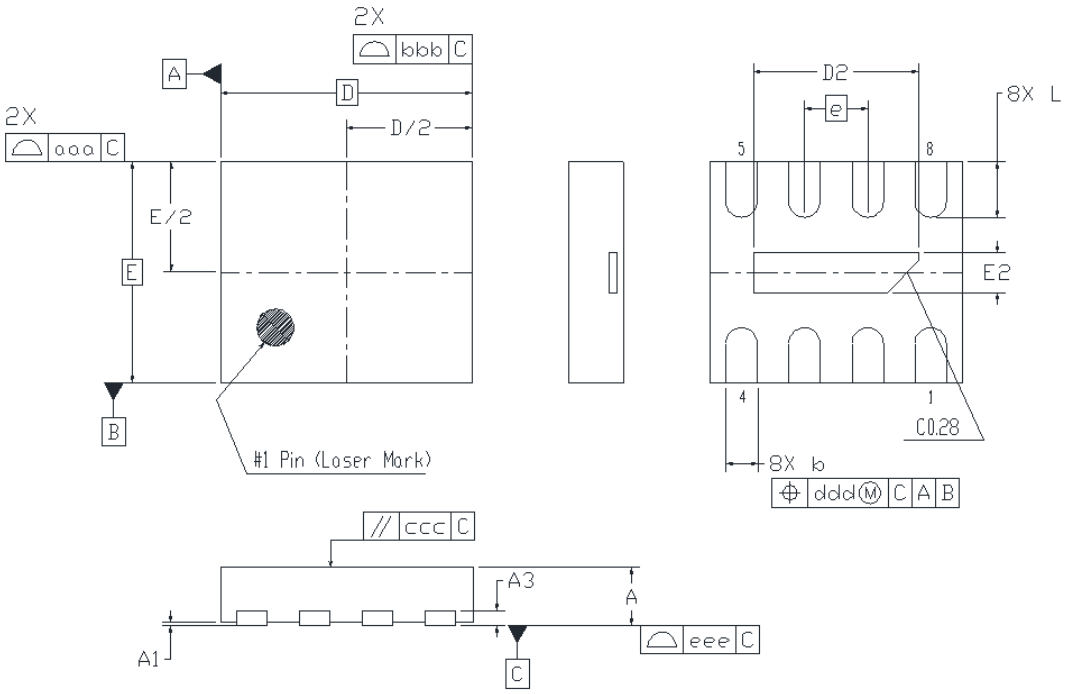


**Figure 6.1. 8-Pin TDFN Package Drawing**

**Table 6.1. Package Diagram Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF. | |
| b | 0.15 | 0.20 | 0.25 |
| D | | 1.60 BSC | |
| D2 | 1.00 | 1.05 | 1.10 |
| e | | 0.40 BSC | |
| E | | 1.40 BSC | |
| E2 | 0.20 | 0.25 | 0.30 |
| L | 0.30 | 0.35 | 0.40 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.07 | |
| eee | | 0.08 | |

| Dimension | Min | Nom | Max |
|---|---|---|---|

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. Land Pattern

The following figure illustrates the land pattern details for the Si53102-A1-A2-A3 in an 8-Pin TDFN package. The table lists the values for the dimensions shown in the illustration.

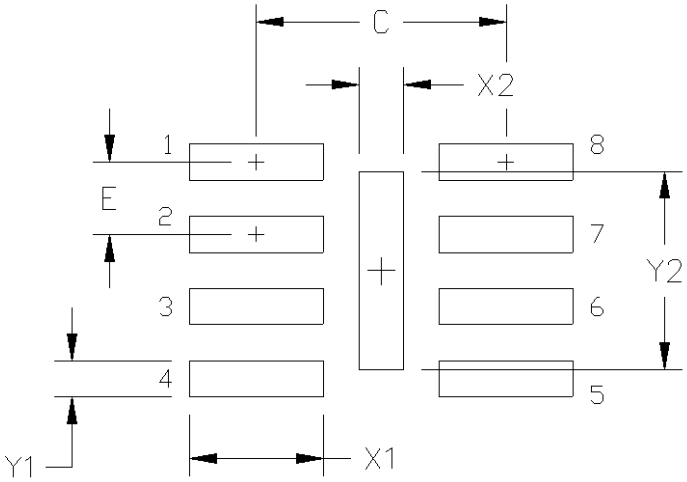


**Figure 7.1. 8-Pin TDFN Land Pattern**

**Table 7.1. Land Pattern Dimensions**

| Dimension | mm |
|---|---|
| C1 | 1.40 |
| E | 0.40 |
| X1 | 0.75 |
| Y1 | 0.20 |
| X2 | 0.25 |
| Y2 | 1.10 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 8. Revision History

## 8.1 Revision 1.0

July 25, 2013

Full-production revision from Rev 0.4

- Updated AC Electrical Specifications table.
  - Updated input frequency min and max specs.
- Updated Test and Measurement Setup section.
  - Added text and reference to AN781.

## 8.2 Revision 1.1

August 5, 2013

- Moved Recommended Design Guideline section.
- Updated Pin Descriptions.
- Updated Package Outline.
- Added Land Pattern.

## 8.3 Revision 1.2

December 2, 2015

- Updated Features.
- Updated Description.
- Updated AC Electrical Specifications table.

## 8.4 Revision 1.3

July 21, 2017

- Updated IDD max specification.
- Separated VOX into 2.5 V and 3.3 V specifications.
- Separated PCie Gen3 jitter into 2.5 V and 3.3 V specifications.
- Separated PCIe Gen4 jitter into 2.5 V and 3.3 V specifications.

## 8.5 Revision 1.4

July 28, 2017

- Updated 2. Electrical Specifications.
  - Updated PCIe Gen 4 Additive Phase Jitter max spec.
- Updated 6. Package Outline.
  - Added notes to Table 6.1 Package Diagram Dimensions on page 11.

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