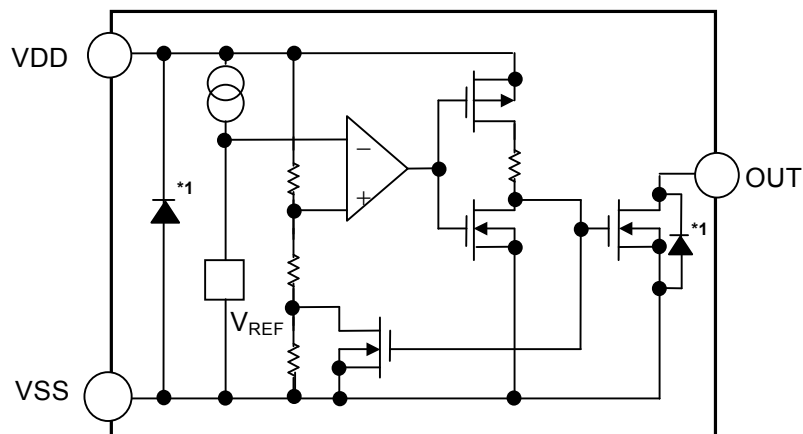


■ Block Diagrams

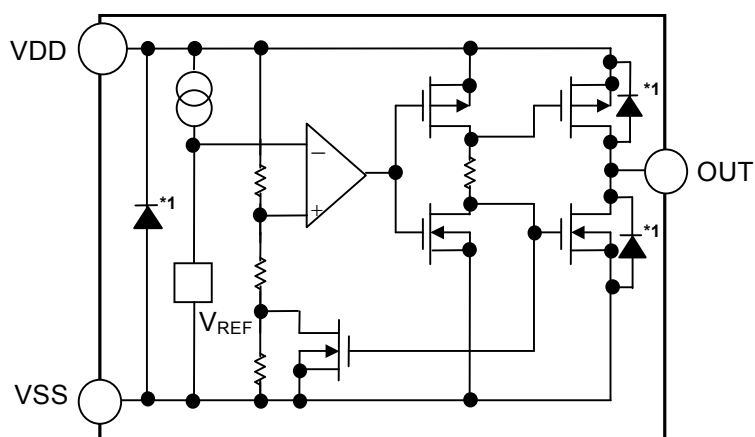
1. Nch Open-drain Output Products



*1. Parasitic diode

Figure 1

2. CMOS Output Products



*1. Parasitic diode

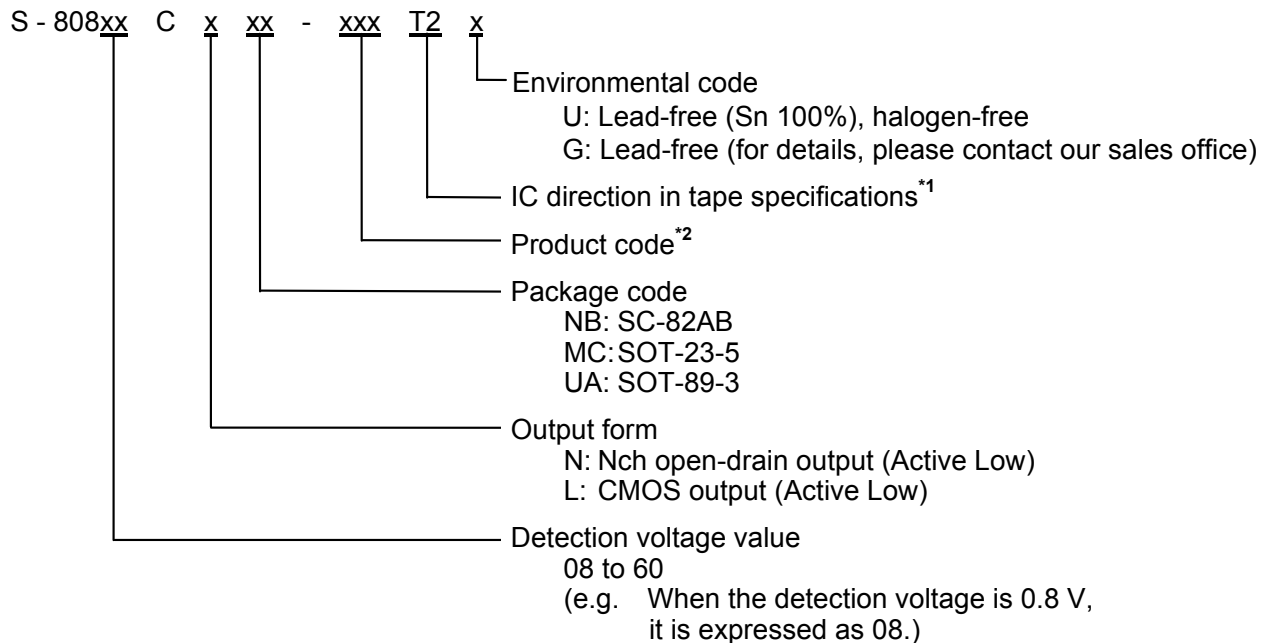
Figure 2

■ Product Name Structure

The detection voltage, output form and packages for S-808xxC Series can be selected at the user's request. Refer to the “**1. Product Name**” for the construction of the product name, “**2. Packages**” regarding the package drawings and “**3. Product Name List**” for the full product names.

1. Product Name

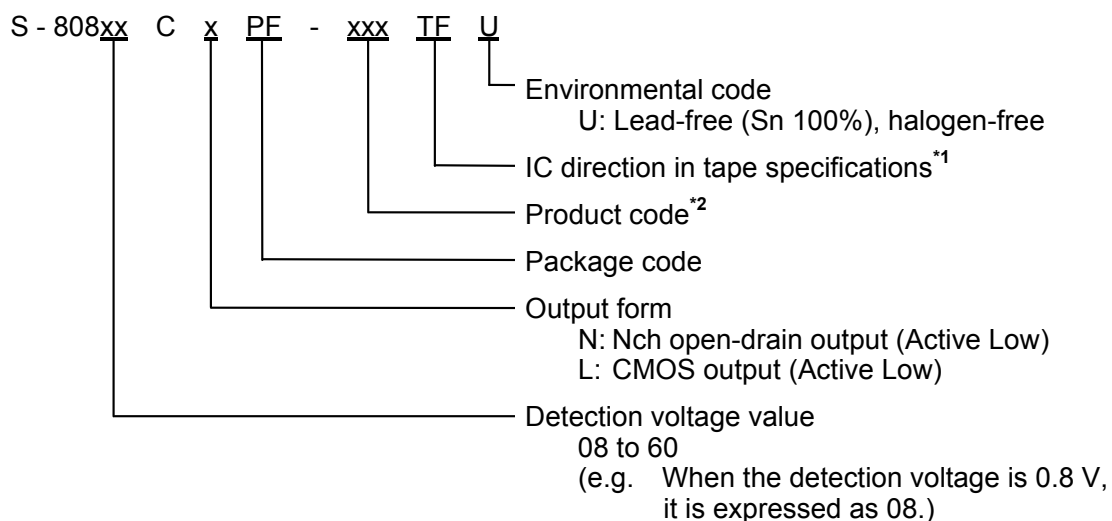
1-1. SC-82AB, SOT-23-5, SOT-89-3



^{*1}. Refer to the tape specifications at the end of this book.

^{*2}. Refer to the **Table 1 and 3** in the “**3. Product Name List**”

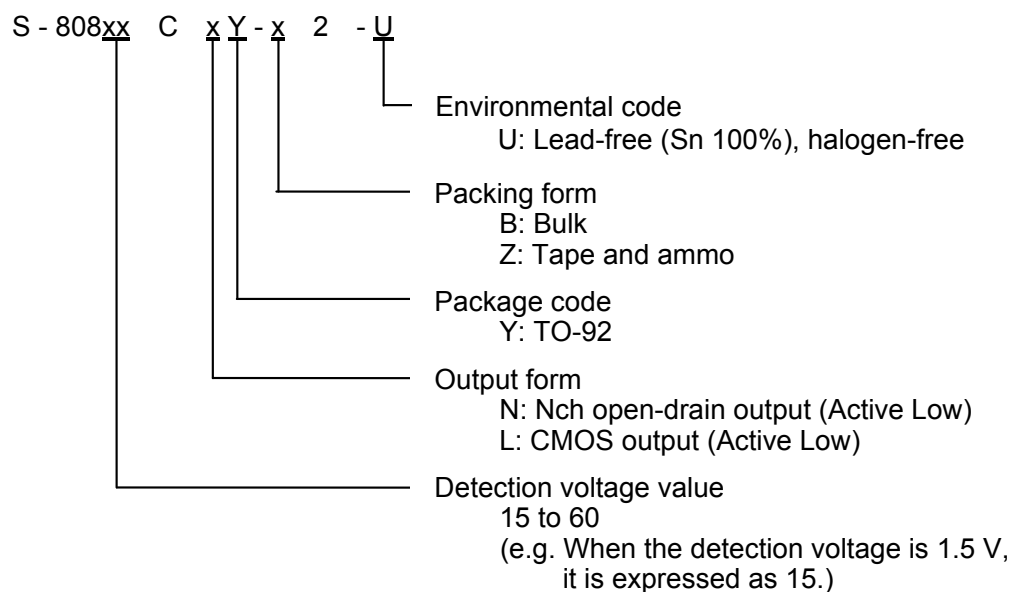
1-2. SNT-4A



^{*1}. Refer to the tape specifications at the end of this book.

^{*2}. Refer to the **Table 2 and 4** in the “**3. Product Name List**”

1-3. TO-92



2. Packages

Package name	Drawing code				
	Package	Tape	Reel	Zigzag	Land
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD	—	—
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	—	—
SOT-89-3	UP003-A-P-SD	UP003-A-C-SD	UP003-A-R-SD	—	—
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	—	PF004-A-L-SD
TO-92 (Bulk)	YS003-D-P-SD	—	—	—	—
TO-92 (Tape and ammo)	YZ003-E-P-SD	YZ003-E-C-SD	—	YZ003-E-Z-SD	—

3. Product Name List

3-1. Nch Open-drain Output Products

Table 1 (1/2)

Detection voltage range	Hysteresis width (Typ.)	SC-82AB	SOT-23-5	SOT-89-3
0.8 V±2.0 %	0.034 V	S-80808CNNB-B9MT2x	—	—
0.9 V±2.0 %	0.044 V	S-80809CNNB-B9NT2x	—	—
1.0 V±2.0 %	0.054 V	S-80810CNNB-B9OT2x	—	—
1.1 V±2.0 %	0.064 V	S-80811CNNB-B9PT2x	—	—
1.2 V±2.0 %	0.073 V	S-80812CNNB-B9QT2x	—	—
1.3 V±2.0 %	0.083 V	S-80813CNNB-B9RT2x	—	—
1.4 V±2.0 %	0.093 V	S-80814CNNB-B9ST2x	—	—
1.5 V±2.0 %	0.075 V	S-80815CNNB-B8AT2x	S-80815CNMC-B8AT2x	S-80815CNUA-B8AT2x
1.6 V±2.0 %	0.080 V	S-80816CNNB-B8BT2x	S-80816CNMC-B8BT2x	S-80816CNUA-B8BT2x
1.7 V±2.0 %	0.085 V	S-80817CNNB-B8CT2x	S-80817CNMC-B8CT2x	S-80817CNUA-B8CT2x
1.8 V±2.0 %	0.090 V	S-80818CNNB-B8DT2x	S-80818CNMC-B8DT2x	S-80818CNUA-B8DT2x
1.9 V±2.0 %	0.095 V	S-80819CNNB-B8ET2x	S-80819CNMC-B8ET2x	S-80819CNUA-B8ET2x
2.0 V±2.0 %	0.100 V	S-80820CNNB-B8FT2x	S-80820CNMC-B8FT2x	S-80820CNUA-B8FT2x
2.1 V±2.0 %	0.105 V	S-80821CNNB-B8GT2x	S-80821CNMC-B8GT2x	S-80821CNUA-B8GT2x
2.2 V±2.0 %	0.110 V	S-80822CNNB-B8HT2x	S-80822CNMC-B8HT2x	S-80822CNUA-B8HT2x
2.3 V±2.0 %	0.115 V	S-80823CNNB-B8IT2x	S-80823CNMC-B8IT2x	S-80823CNUA-B8IT2x
2.4 V±2.0 %	0.120 V	S-80824CNNB-B8JT2x	S-80824CNMC-B8JT2x	S-80824CNUA-B8JT2x
2.4 V typ.	4.4 ± 0.1 V ^{*1}	—	—	S-80824KNUA-D2BT2x ^{*2}
2.5 V±2.0 %	0.125 V	S-80825CNNB-B8KT2x	S-80825CNMC-B8KT2x	S-80825CNUA-B8KT2x
2.6 V±2.0 %	0.130 V	S-80826CNNB-B8LT2x	S-80826CNMC-B8LT2x	S-80826CNUA-B8LT2x
2.7 V±2.0 %	0.135 V	S-80827CNNB-B8MT2x	S-80827CNMC-B8MT2x	S-80827CNUA-B8MT2x
2.8 V±2.0 %	0.140 V	S-80828CNNB-B8NT2x	S-80828CNMC-B8NT2x	S-80828CNUA-B8NT2x
2.9 V±2.0 %	0.145 V	S-80829CNNB-B8OT2x	S-80829CNMC-B8OT2x	S-80829CNUA-B8OT2x
3.0 V±2.0 %	0.150 V	S-80830CNNB-B8PT2x	S-80830CNMC-B8PT2x	S-80830CNUA-B8PT2x
3.1 V±2.0 %	0.155 V	S-80831CNNB-B8QT2x	S-80831CNMC-B8QT2x	S-80831CNUA-B8QT2x
3.2 V±2.0 %	0.160 V	S-80832CNNB-B8RT2x	S-80832CNMC-B8RT2x	S-80832CNUA-B8RT2x
3.3 V±2.0 %	0.165 V	S-80833CNNB-B8ST2x	S-80833CNMC-B8ST2x	S-80833CNUA-B8ST2x
3.4 V±2.0 %	0.170 V	S-80834CNNB-B8TT2x	S-80834CNMC-B8TT2x	S-80834CNUA-B8TT2x
3.5 V±2.0 %	0.175 V	S-80835CNNB-B8UT2x	S-80835CNMC-B8UT2x	S-80835CNUA-B8UT2x
3.6 V±2.0 %	0.180 V	S-80836CNNB-B8VT2x	S-80836CNMC-B8VT2x	S-80836CNUA-B8VT2x
3.7 V±2.0 %	0.185 V	S-80837CNNB-B8WT2x	S-80837CNMC-B8WT2x	S-80837CNUA-B8WT2x
3.8 V±2.0 %	0.190 V	S-80838CNNB-B8XT2x	S-80838CNMC-B8XT2x	S-80838CNUA-B8XT2x
3.9 V±2.0 %	0.195 V	S-80839CNNB-B8YT2x	S-80839CNMC-B8YT2x	S-80839CNUA-B8YT2x

Table 1 (2/2)

Detection voltage range	Hysteresis width (Typ.)	SC-82AB	SOT-23-5	SOT-89-3
4.0 V $\pm$ 2.0 %	0.200 V	S-80840CNNB-B8ZT2x	S-80840CNMC-B8ZT2x	S-80840CNUA-B8ZT2x
4.1 V $\pm$ 2.0 %	0.205 V	S-80841CNNB-B82T2x	S-80841CNMC-B82T2x	S-80841CNUA-B82T2x
4.2 V $\pm$ 2.0 %	0.210 V	S-80842CNNB-B83T2x	S-80842CNMC-B83T2x	S-80842CNUA-B83T2x
4.3 V $\pm$ 2.0 %	0.215 V	S-80843CNNB-B84T2x	S-80843CNMC-B84T2x	S-80843CNUA-B84T2x
4.4 V $\pm$ 2.0 %	0.220 V	S-80844CNNB-B85T2x	S-80844CNMC-B85T2x	S-80844CNUA-B85T2x
4.5 V $\pm$ 2.0 %	0.225 V	S-80845CNNB-B86T2x	S-80845CNMC-B86T2x	S-80845CNUA-B86T2x
4.6 V $\pm$ 2.0 %	0.230 V	S-80846CNNB-B87T2x	S-80846CNMC-B87T2x	S-80846CNUA-B87T2x
4.6 V $\pm$ 0.10 V	0.10 V max.	—	—	S-80846KNUA-D2CT2x ^{*3}
4.7 V $\pm$ 2.0 %	0.235 V	S-80847CNNB-B88T2x	S-80847CNMC-B88T2x	S-80847CNUA-B88T2x
4.8 V $\pm$ 2.0 %	0.240 V	S-80848CNNB-B89T2x	S-80848CNMC-B89T2x	S-80848CNUA-B89T2x
4.9 V $\pm$ 2.0 %	0.245 V	S-80849CNNB-B9AT2x	S-80849CNMC-B9AT2x	S-80849CNUA-B9AT2x
5.0 V $\pm$ 2.0 %	0.250 V	S-80850CNNB-B9BT2x	S-80850CNMC-B9BT2x	S-80850CNUA-B9BT2x
5.1 V $\pm$ 2.0 %	0.255 V	S-80851CNNB-B9CT2x	S-80851CNMC-B9CT2x	S-80851CNUA-B9CT2x
5.2 V $\pm$ 2.0 %	0.260 V	S-80852CNNB-B9DT2x	S-80852CNMC-B9DT2x	S-80852CNUA-B9DT2x
5.3 V $\pm$ 2.0 %	0.265 V	S-80853CNNB-B9ET2x	S-80853CNMC-B9ET2x	S-80853CNUA-B9ET2x
5.4 V $\pm$ 2.0 %	0.270 V	S-80854CNNB-B9FT2x	S-80854CNMC-B9FT2x	S-80854CNUA-B9FT2x
5.5 V $\pm$ 2.0 %	0.275 V	S-80855CNNB-B9GT2x	S-80855CNMC-B9GT2x	S-80855CNUA-B9GT2x
5.6 V $\pm$ 2.0 %	0.280 V	S-80856CNNB-B9HT2x	S-80856CNMC-B9HT2x	S-80856CNUA-B9HT2x
5.7 V $\pm$ 2.0 %	0.285 V	S-80857CNNB-B9IT2x	S-80857CNMC-B9IT2x	S-80857CNUA-B9IT2x
5.8 V $\pm$ 2.0 %	0.290 V	S-80858CNNB-B9JT2x	S-80858CNMC-B9JT2x	S-80858CNUA-B9JT2x
5.9 V $\pm$ 2.0 %	0.295 V	S-80859CNNB-B9KT2x	S-80859CNMC-B9KT2x	S-80859CNUA-B9KT2x
6.0 V $\pm$ 2.0 %	0.300 V	S-80860CNNB-B9LT2x	S-80860CNMC-B9LT2x	S-80860CNUA-B9LT2x

*1. Describes the release voltage.

*2. Refer to the **Table 18** in “■ Electrical Characteristics for Customized Products” for electrical characteristics.

*3. Refer to the **Table 20** in “■ Electrical Characteristics for Customized Products” for electrical characteristics

Remark 1. x: G or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

Table 2 (1/2)

Detection voltage range	Hysteresis width (Typ.)	SNT-4A	TO-92 ^{*1}
0.8 V±2.0 %	0.034 V	S-80808CNPFB-B9MTFU	—
0.9 V±2.0 %	0.044 V	S-80809CNPFB-B9NTFU	—
1.0 V±2.0 %	0.054 V	S-80810CNPFB-B9OTFU	—
1.1 V±2.0 %	0.064 V	S-80811CNPFB-B9PTFU	—
1.2 V±2.0 %	0.073 V	S-80812CNPFB-B9QTFU	—
1.3 V±2.0 %	0.083 V	S-80813CNPFB-B9RTFU	—
1.4 V±2.0 %	0.093 V	S-80814CNPFB-B9STFU	—
1.5 V±2.0 %	0.075 V	S-80815CNPFB-B8ATFU	S-80815CNY-n2-U
1.6 V±2.0 %	0.080 V	S-80816CNPFB-B8BTFU	S-80816CNY-n2-U
1.7 V±2.0 %	0.085 V	S-80817CNPFB-B8CTFU	S-80817CNY-n2-U
1.8 V±2.0 %	0.090 V	S-80818CNPFB-B8DTFU	S-80818CNY-n2-U
1.9 V±2.0 %	0.095 V	S-80819CNPFB-B8ETFU	S-80819CNY-n2-U
2.0 V±2.0 %	0.100 V	S-80820CNPFB-B8FTFU	S-80820CNY-n2-U
2.1 V±2.0 %	0.105 V	S-80821CNPFB-B8GTFU	S-80821CNY-n2-U
2.2 V±2.0 %	0.110 V	S-80822CNPFB-B8HTFU	S-80822CNY-n2-U
2.3 V±2.0 %	0.115 V	S-80823CNPFB-B8ITFU	S-80823CNY-n2-U
2.4 V±2.0 %	0.120 V	S-80824CNPFB-B8JTFU	S-80824CNY-n2-U
2.4 V typ.	4.4 ± 0.1 V ^{*2}	—	S-80824KNY-n2-U ^{*3}
2.5 V±2.0 %	0.125 V	S-80825CNPFB-B8KTFU	S-80825CNY-n2-U
2.6 V±2.0 %	0.130 V	S-80826CNPFB-B8LTFU	S-80826CNY-n2-U
2.7 V±2.0 %	0.135 V	S-80827CNPFB-B8MTFU	S-80827CNY-n2-U
2.8 V±2.0 %	0.140 V	S-80828CNPFB-B8NTFU	S-80828CNY-n2-U
2.9 V±2.0 %	0.145 V	S-80829CNPFB-B8OTFU	S-80829CNY-n2-U
3.0 V±2.0 %	0.150 V	S-80830CNPFB-B8PTFU	S-80830CNY-n2-U
3.1 V±2.0 %	0.155 V	S-80831CNPFB-B8QTFU	S-80831CNY-n2-U
3.2 V±2.0 %	0.160 V	S-80832CNPFB-B8RTFU	S-80832CNY-n2-U
3.3 V±2.0 %	0.165 V	S-80833CNPFB-B8STFU	S-80833CNY-n2-U
3.4 V±2.0 %	0.170 V	S-80834CNPFB-B8TTFU	S-80834CNY-n2-U
3.5 V±2.0 %	0.175 V	S-80835CNPFB-B8UTFU	S-80835CNY-n2-U
3.6 V±2.0 %	0.180 V	S-80836CNPFB-B8VTFU	S-80836CNY-n2-U
3.7 V±2.0 %	0.185 V	S-80837CNPFB-B8WTFU	S-80837CNY-n2-U
3.8 V±2.0 %	0.190 V	S-80838CNPFB-B8XTFU	S-80838CNY-n2-U
3.9 V±2.0 %	0.195 V	S-80839CNPFB-B8YTFU	S-80839CNY-n2-U
4.0 V±2.0 %	0.200 V	S-80840CNPFB-B8ZTFU	S-80840CNY-n2-U
4.1 V±2.0 %	0.205 V	S-80841CNPFB-B82TFU	S-80841CNY-n2-U
4.2 V±2.0 %	0.210 V	S-80842CNPFB-B83TFU	S-80842CNY-n2-U
4.3 V±2.0 %	0.215 V	S-80843CNPFB-B84TFU	S-80843CNY-n2-U
4.4 V±2.0 %	0.220 V	S-80844CNPFB-B85TFU	S-80844CNY-n2-U
4.5 V±2.0 %	0.225 V	S-80845CNPFB-B86TFU	S-80845CNY-n2-U
4.6 V±2.0 %	0.230 V	S-80846CNPFB-B87TFU	S-80846CNY-n2-U
4.6 V±0.10 V	0.10 V max.	—	S-80846KNY-n2-U ^{*4}
4.7 V±2.0 %	0.235 V	S-80847CNPFB-B88TFU	S-80847CNY-n2-U
4.8 V±2.0 %	0.240 V	S-80848CNPFB-B89TFU	S-80848CNY-n2-U
4.9 V±2.0 %	0.245 V	S-80849CNPFB-B9ATFU	S-80849CNY-n2-U
5.0 V±2.0 %	0.250 V	S-80850CNPFB-B9BTFU	S-80850CNY-n2-U
5.1 V±2.0 %	0.255 V	S-80851CNPFB-B9CTFU	S-80851CNY-n2-U

Table 2 (2/2)

Detection voltage range	Hysteresis width (Typ.)	SNT-4A	TO-92 ^{*1}
5.2 V±2.0 %	0.260 V	S-80852CNPF-B9DTFU	S-80852CNY-n2-U
5.3 V±2.0 %	0.265 V	S-80853CNPF-B9ETFU	S-80853CNY-n2-U
5.4 V±2.0 %	0.270 V	S-80854CNPF-B9FTFU	S-80854CNY-n2-U
5.5 V±2.0 %	0.275 V	S-80855CNPF-B9GTFU	S-80855CNY-n2-U
5.6 V±2.0 %	0.280 V	S-80856CNPF-B9HTFU	S-80856CNY-n2-U
5.7 V±2.0 %	0.285 V	S-80857CNPF-B9ITFU	S-80857CNY-n2-U
5.8 V±2.0 %	0.290 V	S-80858CNPF-B9JTFU	S-80858CNY-n2-U
5.9 V±2.0 %	0.295 V	S-80859CNPF-B9KTFU	S-80859CNY-n2-U
6.0 V±2.0 %	0.300 V	S-80860CNPF-B9LTFU	S-80860CNY-n2-U

*1. n changes according to the packing form in TO-92. B: Bulk, Z: Tape and ammo

*2. Describes the release voltage.

*3. Refer to the **Table 18** in “■ Electrical Characteristics for Customized Products” for electrical characteristics.

*4. Refer to the **Table 20** in “■ Electrical Characteristics for Customized Products” for electrical characteristics.

3-2. CMOS Output Products

Table 3 (1/2)

Detection voltage range	Hysteresis width (Typ.)	SC-82AB	SOT-23-5	SOT-89-3
0.8 V±2.0 %	0.034 V	S-80808CLNB-B7MT2x	—	—
0.9 V±2.0 %	0.044 V	S-80809CLNB-B7NT2x	—	—
1.0 V±2.0 %	0.054 V	S-80810CLNB-B7OT2x	—	—
1.1 V±2.0 %	0.064 V	S-80811CLNB-B7PT2x	—	—
1.2 V±2.0 %	0.073 V	S-80812CLNB-B7QT2x	—	—
1.3 V±2.0 %	0.083 V	S-80813CLNB-B7RT2x	—	—
1.4 V±2.0 %	0.093 V	S-80814CLNB-B7ST2x	—	—
1.5 V±2.0 %	0.075 V	S-80815CLNB-B6AT2x	S-80815CLMC-B6AT2x	S-80815CLUA-B6AT2x
1.6 V±2.0 %	0.080 V	S-80816CLNB-B6BT2x	S-80816CLMC-B6BT2x	S-80816CLUA-B6BT2x
1.7 V±2.0 %	0.085 V	S-80817CLNB-B6CT2x	S-80817CLMC-B6CT2x	S-80817CLUA-B6CT2x
1.8 V±2.0 %	0.090 V	S-80818CLNB-B6DT2x	S-80818CLMC-B6DT2x	S-80818CLUA-B6DT2x
1.9 V±2.0 %	0.095 V	S-80819CLNB-B6ET2x	S-80819CLMC-B6ET2x	S-80819CLUA-B6ET2x
2.0 V±2.0 %	0.100 V	S-80820CLNB-B6FT2x	S-80820CLMC-B6FT2x	S-80820CLUA-B6FT2x
2.1 V±2.0 %	0.105 V	S-80821CLNB-B6GT2x	S-80821CLMC-B6GT2x	S-80821CLUA-B6GT2x
2.2 V±2.0 %	0.110 V	S-80822CLNB-B6HT2x	S-80822CLMC-B6HT2x	S-80822CLUA-B6HT2x
2.3 V±2.0 %	0.115 V	S-80823CLNB-B6IT2x	S-80823CLMC-B6IT2x	S-80823CLUA-B6IT2x
2.4 V±2.0 %	0.120 V	S-80824CLNB-B6JT2x	S-80824CLMC-B6JT2x	S-80824CLUA-B6JT2x
2.5 V±2.0 %	0.125 V	S-80825CLNB-B6KT2x	S-80825CLMC-B6KT2x	S-80825CLUA-B6KT2x
2.6 V±2.0 %	0.130 V	S-80826CLNB-B6LT2x	S-80826CLMC-B6LT2x	S-80826CLUA-B6LT2x
2.7 V±2.0 %	0.135 V	S-80827CLNB-B6MT2x	S-80827CLMC-B6MT2x	S-80827CLUA-B6MT2x
2.8 V±2.0 %	0.140 V	S-80828CLNB-B6NT2x	S-80828CLMC-B6NT2x	S-80828CLUA-B6NT2x
2.9 V±2.0 %	0.145 V	S-80829CLNB-B6OT2x	S-80829CLMC-B6OT2x	S-80829CLUA-B6OT2x
3.0 V±2.0 %	0.150 V	S-80830CLNB-B6PT2x	S-80830CLMC-B6PT2x	S-80830CLUA-B6PT2x
3.1 V±2.0 %	0.155 V	S-80831CLNB-B6QT2x	S-80831CLMC-B6QT2x	S-80831CLUA-B6QT2x
3.2 V±2.0 %	0.160 V	S-80832CLNB-B6RT2x	S-80832CLMC-B6RT2x	S-80832CLUA-B6RT2x
3.3 V±2.0 %	0.165 V	S-80833CLNB-B6ST2x	S-80833CLMC-B6ST2x	S-80833CLUA-B6ST2x
3.4 V±2.0 %	0.170 V	S-80834CLNB-B6TT2x	S-80834CLMC-B6TT2x	S-80834CLUA-B6TT2x
3.5 V±2.0 %	0.175 V	S-80835CLNB-B6UT2x	S-80835CLMC-B6UT2x	S-80835CLUA-B6UT2x
3.6 V±2.0 %	0.180 V	S-80836CLNB-B6VT2x	S-80836CLMC-B6VT2x	S-80836CLUA-B6VT2x
3.7 V±2.0 %	0.185 V	S-80837CLNB-B6WT2x	S-80837CLMC-B6WT2x	S-80837CLUA-B6WT2x
3.8 V±2.0 %	0.190 V	S-80838CLNB-B6XT2x	S-80838CLMC-B6XT2x	S-80838CLUA-B6XT2x
3.9 V±2.0 %	0.195 V	S-80839CLNB-B6YT2x	S-80839CLMC-B6YT2x	S-80839CLUA-B6YT2x
4.0 V±2.0 %	0.200 V	S-80840CLNB-B6ZT2x	S-80840CLMC-B6ZT2x	S-80840CLUA-B6ZT2x
4.1 V±2.0 %	0.205 V	S-80841CLNB-B62T2x	S-80841CLMC-B62T2x	S-80841CLUA-B62T2x
4.2 V±2.0 %	0.210 V	S-80842CLNB-B63T2x	S-80842CLMC-B63T2x	S-80842CLUA-B63T2x
4.3 V±2.0 %	0.215 V	S-80843CLNB-B64T2x	S-80843CLMC-B64T2x	S-80843CLUA-B64T2x
4.4 V±2.0 %	0.220 V	S-80844CLNB-B65T2x	S-80844CLMC-B65T2x	S-80844CLUA-B65T2x
4.45 V typ.	4.70 V max.*1	—	—	S-80844KLUA-D2AT2x*2
4.5 V±2.0 %	0.225 V	S-80845CLNB-B66T2x	S-80845CLMC-B66T2x	S-80845CLUA-B66T2x
4.6 V±2.0 %	0.230 V	S-80846CLNB-B67T2x	S-80846CLMC-B67T2x	S-80846CLUA-B67T2x
4.7 V±2.0 %	0.235 V	S-80847CLNB-B68T2x	S-80847CLMC-B68T2x	S-80847CLUA-B68T2x
4.8 V±2.0 %	0.240 V	S-80848CLNB-B69T2x	S-80848CLMC-B69T2x	S-80848CLUA-B69T2x
4.9 V±2.0 %	0.245 V	S-80849CLNB-B7AT2x	S-80849CLMC-B7AT2x	S-80849CLUA-B7AT2x
5.0 V±2.0 %	0.250 V	S-80850CLNB-B7BT2x	S-80850CLMC-B7BT2x	S-80850CLUA-B7BT2x
5.1 V±2.0 %	0.255 V	S-80851CLNB-B7CT2x	S-80851CLMC-B7CT2x	S-80851CLUA-B7CT2x

Table 3 (2/2)

Detection voltage range	Hysteresis width (Typ.)	SC-82AB	SOT-23-5	SOT-89-3
5.2 V±2.0 %	0.260 V	S-80852CLNB-B7DT2x	S-80852CLMC-B7DT2x	S-80852CLUA-B7DT2x
5.3 V±2.0 %	0.265 V	S-80853CLNB-B7ET2x	S-80853CLMC-B7ET2x	S-80853CLUA-B7ET2x
5.4 V±2.0 %	0.270 V	S-80854CLNB-B7FT2x	S-80854CLMC-B7FT2x	S-80854CLUA-B7FT2x
5.5 V±2.0 %	0.275 V	S-80855CLNB-B7GT2x	S-80855CLMC-B7GT2x	S-80855CLUA-B7GT2x
5.6 V±2.0 %	0.280 V	S-80856CLNB-B7HT2x	S-80856CLMC-B7HT2x	S-80856CLUA-B7HT2x
5.7 V±2.0 %	0.285 V	S-80857CLNB-B7IT2x	S-80857CLMC-B7IT2x	S-80857CLUA-B7IT2x
5.8 V±2.0 %	0.290 V	S-80858CLNB-B7JT2x	S-80858CLMC-B7JT2x	S-80858CLUA-B7JT2x
5.9 V±2.0 %	0.295 V	S-80859CLNB-B7KT2x	S-80859CLMC-B7KT2x	S-80859CLUA-B7KT2x
6.0 V±2.0 %	0.300 V	S-80860CLNB-B7LT2x	S-80860CLMC-B7LT2x	S-80860CLUA-B7LT2x

*1. Describes the release voltage.

*2. Refer to the **Table 19** in “■ Electrical Characteristics for Customized Products” for electrical characteristics.

Remark 1. x: G or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

Table 4 (1/2)

Detection voltage range	Hysteresis width (Typ.)	SNT-4A	TO-92 ^{*1}
0.8 V±2.0 %	0.034 V	S-80808CLPF-B7MTFU	—
0.9 V±2.0 %	0.044 V	S-80809CLPF-B7NTFU	—
1.0 V±2.0 %	0.054 V	S-80810CLPF-B7OTFU	—
1.1 V±2.0 %	0.064 V	S-80811CLPF-B7PTFU	—
1.2 V±2.0 %	0.073 V	S-80812CLPF-B7QTFU	—
1.3 V±2.0 %	0.083 V	S-80813CLPF-B7RTFU	—
1.4 V±2.0 %	0.093 V	S-80814CLPF-B7STFU	—
1.5 V±2.0 %	0.075 V	S-80815CLPF-B6ATFU	S-80815CLY-n2-U
1.6 V±2.0 %	0.080 V	S-80816CLPF-B6BTFU	S-80816CLY-n2-U
1.7 V±2.0 %	0.085 V	S-80817CLPF-B6CTFU	S-80817CLY-n2-U
1.8 V±2.0 %	0.090 V	S-80818CLPF-B6DTFU	S-80818CLY-n2-U
1.9 V±2.0 %	0.095 V	S-80819CLPF-B6ETFU	S-80819CLY-n2-U
2.0 V±2.0 %	0.100 V	S-80820CLPF-B6FTFU	S-80820CLY-n2-U
2.1 V±2.0 %	0.105 V	S-80821CLPF-B6GTFU	S-80821CLY-n2-U
2.2 V±2.0 %	0.110 V	S-80822CLPF-B6HTFU	S-80822CLY-n2-U
2.3 V±2.0 %	0.115 V	S-80823CLPF-B6ITFU	S-80823CLY-n2-U
2.4 V±2.0 %	0.120 V	S-80824CLPF-B6JTFU	S-80824CLY-n2-U
2.5 V±2.0 %	0.125 V	S-80825CLPF-B6KTFU	S-80825CLY-n2-U
2.6 V±2.0 %	0.130 V	S-80826CLPF-B6LTFU	S-80826CLY-n2-U
2.7 V±2.0 %	0.135 V	S-80827CLPF-B6MTFU	S-80827CLY-n2-U
2.8 V±2.0 %	0.140 V	S-80828CLPF-B6NTFU	S-80828CLY-n2-U
2.9 V±2.0 %	0.145 V	S-80829CLPF-B6OTFU	S-80829CLY-n2-U
3.0 V±2.0 %	0.150 V	S-80830CLPF-B6PTFU	S-80830CLY-n2-U
3.1 V±2.0 %	0.155 V	S-80831CLPF-B6QTFU	S-80831CLY-n2-U
3.2 V±2.0 %	0.160 V	S-80832CLPF-B6RTFU	S-80832CLY-n2-U
3.3 V±2.0 %	0.165 V	S-80833CLPF-B6STFU	S-80833CLY-n2-U
3.4 V±2.0 %	0.170 V	S-80834CLPF-B6TTFU	S-80834CLY-n2-U
3.5 V±2.0 %	0.175 V	S-80835CLPF-B6UTFU	S-80835CLY-n2-U
3.6 V±2.0 %	0.180 V	S-80836CLPF-B6VTFU	S-80836CLY-n2-U
3.7 V±2.0 %	0.185 V	S-80837CLPF-B6WTFU	S-80837CLY-n2-U
3.8 V±2.0 %	0.190 V	S-80838CLPF-B6XTFU	S-80838CLY-n2-U

Table 4 (2/2)

Detection voltage range	Hysteresis width (Typ.)	SNT-4A	TO-92 ^{*1}
3.9 V±2.0 %	0.195 V	S-80839CLPF-B6YTFU	S-80839CLY-n2-U
4.0 V±2.0 %	0.200 V	S-80840CLPF-B6ZTFU	S-80840CLY-n2-U
4.1 V±2.0 %	0.205 V	S-80841CLPF-B62TFU	S-80841CLY-n2-U
4.2 V±2.0 %	0.210 V	S-80842CLPF-B63TFU	S-80842CLY-n2-U
4.3 V±2.0 %	0.215 V	S-80843CLPF-B64TFU	S-80843CLY-n2-U
4.4 V±2.0 %	0.220 V	S-80844CLPF-B65TFU	S-80844CLY-n2-U
4.45 V typ.	4.70 V max. ^{*2}	—	S-80844KLY-n2-U ^{*3}
4.5 V±2.0 %	0.225 V	S-80845CLPF-B66TFU	S-80845CLY-n2-U
4.6 V±2.0 %	0.230 V	S-80846CLPF-B67TFU	S-80846CLY-n2-U
4.7 V±2.0 %	0.235 V	S-80847CLPF-B68TFU	S-80847CLY-n2-U
4.8 V±2.0 %	0.240 V	S-80848CLPF-B69TFU	S-80848CLY-n2-U
4.9 V±2.0 %	0.245 V	S-80849CLPF-B7ATFU	S-80849CLY-n2-U
5.0 V±2.0 %	0.250 V	S-80850CLPF-B7BTFU	S-80850CLY-n2-U
5.1 V±2.0 %	0.255 V	S-80851CLPF-B7CTFU	S-80851CLY-n2-U
5.2 V±2.0 %	0.260 V	S-80852CLPF-B7DTFU	S-80852CLY-n2-U
5.3 V±2.0 %	0.265 V	S-80853CLPF-B7ETFU	S-80853CLY-n2-U
5.4 V±2.0 %	0.270 V	S-80854CLPF-B7FTFU	S-80854CLY-n2-U
5.5 V±2.0 %	0.275 V	S-80855CLPF-B7GTFU	S-80855CLY-n2-U
5.6 V±2.0 %	0.280 V	S-80856CLPF-B7HTFU	S-80856CLY-n2-U
5.7 V±2.0 %	0.285 V	S-80857CLPF-B7ITFU	S-80857CLY-n2-U
5.8 V±2.0 %	0.290 V	S-80858CLPF-B7JTFU	S-80858CLY-n2-U
5.9 V±2.0 %	0.295 V	S-80859CLPF-B7KTFU	S-80859CLY-n2-U
6.0 V±2.0 %	0.300 V	S-80860CLPF-B7LTFU	S-80860CLY-n2-U

*1. n changes according to the packing form in TO-92. B: Bulk, Z: Tape and ammo

*2. Describes the release voltage.

*3. Refer to the **Table 19** in “■ Electrical Characteristics for Customized Products” for electrical characteristics.

■ Output Forms

1. Output Forms in S-808xxC Series

Table 5

	Nch open-drain output products (Active Low)	CMOS output products (Active Low)
S-808xxC Series	"N" is the last letter of the product name. e.g. S-80815CN	"L" is the last letter of the product name. e.g. S-80815CL

2. Output Forms and Their Usage

Table 6

Usage	Nch open-drain output products (Active Low)	CMOS output products (Active Low)
Different power supplies	Yes	No
Active Low reset for CPUs	Yes	Yes
Active High reset for CPUs	No	No
Detection voltage change by resistor divider	Yes	No

- Example for two power supplies
- Example for one power supply

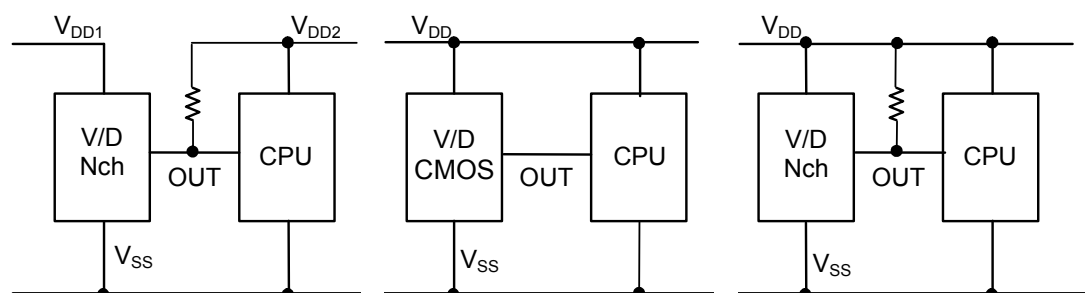


Figure 3

■ **Pin Configurations**

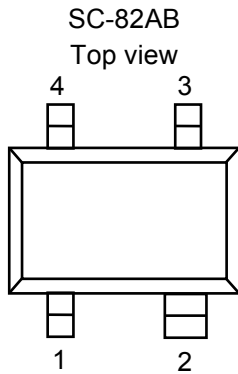


Figure 4

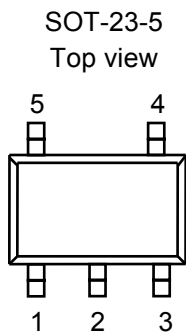


Figure 5

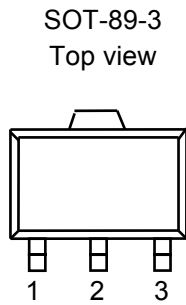


Figure 6

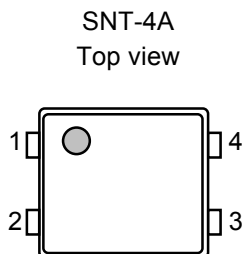


Figure 7

Table 7

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	NC ^{*1}	No connection
4	VSS	GND pin

^{*1}. The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

Table 8

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin
4	NC ^{*1}	No connection
5	NC ^{*1}	No connection

^{*1}. The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

Table 9

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin

Table 10

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VSS	GND pin
3	NC ^{*1}	No connection
4	VDD	Voltage input pin

^{*1}. The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

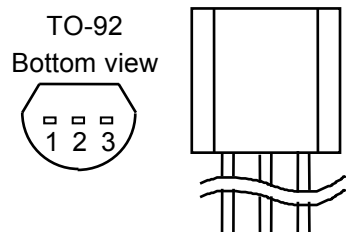


Figure 8

Table 11

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	GND pin

■ Absolute Maximum Ratings

1. Detection Voltage Typ. 1.4 V or Less Products

Table 12

(Ta = 25 °C unless otherwise specified)

Item		Symbol	Absolute maximum ratings	Unit
Power supply voltage		$V_{DD}-V_{SS}$	7	V
Output voltage	Nch open-drain output products	V_{OUT}	$V_{SS}-0.3$ to $V_{SS}+7$	V
	CMOS output products		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output current		I_{OUT}	50	mA
Power dissipation	SC-82AB	P_D	150 (When not mounted on board)	mW
			350^{*1}	mW
	SNT-4A		140 (When not mounted on board)	mW
			300^{*1}	mW
Operating ambient temperature		T_{opr}	-40 to +85	°C
Storage temperature		T_{stg}	-40 to +125	°C

*1. When mounted on board

[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

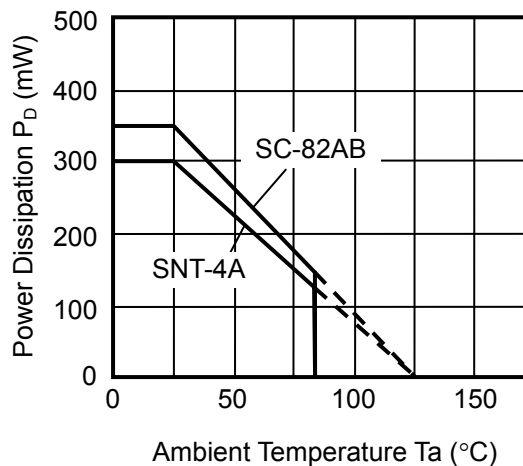


Figure 9 Power Dissipation of Package (When Mounted on Board)

2. Detection Voltage Typ. 1.5 V or More Products

Table 13

(Ta = 25 °C unless otherwise specified)

Item		Symbol	Absolute maximum ratings	Unit
Power supply voltage		$V_{DD}-V_{SS}$	12	V
Output voltage	Nch open-drain output products	V_{OUT}	$V_{SS}-0.3$ to $V_{SS}+12$	V
	CMOS output products		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output current		I_{OUT}	50	mA
Power dissipation	SC-82AB	P_D	150 (When not mounted on board)	mW
			350 ^{*1}	mW
	SOT-23-5		250 (When not mounted on board)	mW
			600 ^{*1}	mW
	SOT-89-3		500 (When not mounted on board)	mW
			1000 ^{*1}	mW
	SNT-4A		140 (When not mounted on board)	mW
			300 ^{*1}	mW
	TO-92		400 (When not mounted on board)	mW
			800 ^{*1}	mW
Operating ambient temperature		T_{opr}	-40 to +85	°C
Storage temperature		T_{stg}	-40 to +125	°C

*1. When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

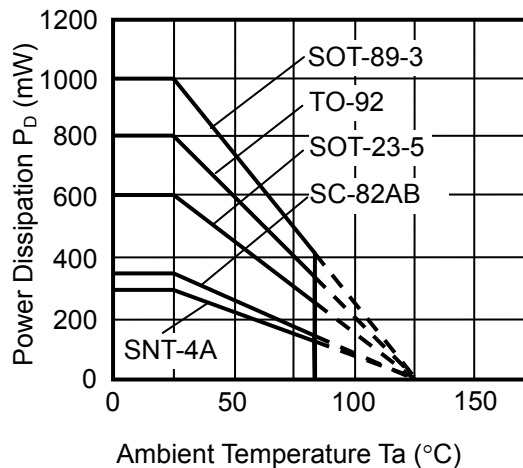


Figure 10 Power Dissipation of Package (When Mounted on Board)

■ **Electrical Characteristics**

1. Nch Open-drain Output Products

1-1. Detection Voltage Typ.1.4 V or Less Products

Table 14

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Detection voltage*1	$-V_{DET}$	—	$-V_{DET(S)} \times 0.98$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02$	V	1
Release voltage	$+V_{DET}$	S-80808	0.802	0.834	0.867	V	1
		S-80809	0.910	0.944	0.979	V	1
		S-80810	1.017	1.054	1.091	V	1
		S-80811	1.125	1.164	1.203	V	1
		S-80812	1.232	1.273	1.315	V	1
		S-80813	1.340	1.383	1.427	V	1
		S-80814	1.448	1.493	1.538	V	1
Hysteresis width	V_{HYS}	S-80808	0.018	0.034	0.051	V	1
		S-80809	0.028	0.044	0.061	V	1
		S-80810	0.037	0.054	0.071	V	1
		S-80811	0.047	0.064	0.081	V	1
		S-80812	0.056	0.073	0.091	V	1
		S-80813	0.066	0.083	0.101	V	1
		S-80814	0.076	0.093	0.110	V	1
Current consumption	I_{SS}	$V_{DD} = 1.5 \text{ V}$ S-80808 to 09	—	1.3	3.5	μA	2
		$V_{DD} = 2.0 \text{ V}$ S-80810 to 14	—	1.3	3.5	μA	2
Operating voltage	V_{DD}	—	0.65	—	5.0	V	1
Output current	I_{OUT}	Output transistor, Nch, $V_{DS} = 0.5 \text{ V}$, $V_{DD} = 0.7 \text{ V}$	0.04	0.2	—	mA	3
Leakage current	I_{LEAK}	Output transistor, Nch, $V_{DS} = 5.0 \text{ V}$, $V_{DD} = 5.0 \text{ V}$	—	—	60	nA	3
Response time	t_{PLH}	—	—	—	60	μs	1
Detection voltage temperature coefficient*2	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	$Ta = -40 \text{ to } +85 \text{ }^{\circ}\text{C}$	—	±100	±350	ppm/ °C	1

*1. $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 1 to 2**.)

*2. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^{\circ}\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^{\circ}\text{C}]^{*3} \div 1000$$

*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

1-2. Detection Voltage Typ.1.5 V or More Products

Table 15

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Detection voltage ^{*1}	$-V_{DET}$	—	$-V_{DET(S)} \times 0.98$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02$	V	1
Hysteresis width	V_{HYS}	—	$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.08$	V	1
Current consumption	I_{SS}	$V_{DD} = 3.5\text{ V}$ S-80815 to 26	—	0.8	2.4	μA	2
		$V_{DD} = 4.5\text{ V}$ S-80827 to 39	—	0.8	2.4	μA	2
		$V_{DD} = 6.0\text{ V}$ S-80840 to 56	—	0.9	2.7	μA	2
		$V_{DD} = 7.5\text{ V}$ S-80857 to 60	—	0.9	2.7	μA	2
Operating voltage	V_{DD}	—	0.95	—	10.0	V	1
Output current	I_{OUT}	Output transistor, $V_{DD} = 1.2\text{ V}$ Nch, $V_{DS} = 0.5\text{ V}$ S-80815 to 60	0.59	1.36	—	mA	3
		$V_{DD} = 2.4\text{ V}$ S-80827 to 60	2.88	4.98	—	mA	3
Leakage current	I_{LEAK}	Output transistor, Nch, $V_{DS} = 10.0\text{ V}$, $V_{DD} = 10.0\text{ V}$	—	—	100	nA	3
Response time	t_{PLH}	—	—	—	60	μs	1
Detection voltage temperature coefficient ^{*2}	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = -40 to +85 °C	—	±100	±350	ppm/°C	1

*1. $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 1 to 2**.)

*2. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^{\circ}\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^{\circ}\text{C}]^{*3} \div 1000$$

*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

2. CMOS Output Products

2-1. Detection Voltage Typ.1.4 V or Less Products

Table 16

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Detection voltage ^{*1}	$-V_{DET}$	—	$-V_{DET(S)} \times 0.98$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02$	V	1
Release voltage	$+V_{DET}$	S-80808	0.802	0.834	0.867	V	1
		S-80809	0.910	0.944	0.979	V	1
		S-80810	1.017	1.054	1.091	V	1
		S-80811	1.125	1.164	1.203	V	1
		S-80812	1.232	1.273	1.315	V	1
		S-80813	1.340	1.383	1.427	V	1
		S-80814	1.448	1.493	1.538	V	1
Hysteresis width	V_{HYS}	S-80808	0.018	0.034	0.051	V	1
		S-80809	0.028	0.044	0.061	V	1
		S-80810	0.037	0.054	0.071	V	1
		S-80811	0.047	0.064	0.081	V	1
		S-80812	0.056	0.073	0.091	V	1
		S-80813	0.066	0.083	0.101	V	1
		S-80814	0.076	0.093	0.110	V	1
Current consumption	I_{SS}	$V_{DD} = 1.5 \text{ V}$ S-80808 to 09	—	1.3	3.5	μA	2
		$V_{DD} = 2.0 \text{ V}$ S-80810 to 14	—	1.3	3.5	μA	2
Operating voltage	V_{DD}	—	0.65	—	5.0	V	1
Output current	I_{OUT}	Output transistor, Nch, $V_{DS} = 0.5 \text{ V}$, $V_{DD} = 0.7 \text{ V}$	0.04	0.2	—	mA	3
		Output transistor, Pch, $V_{DS} = 2.1 \text{ V}$, $V_{DD} = 4.5 \text{ V}$	2.9	5.8	—	mA	4
Response time	t_{PLH}	—	—	—	60	μs	1
Detection voltage temperature coefficient ^{*2}	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	$Ta = -40 \text{ to } +85 \text{ }^{\circ}\text{C}$	—	±100	±350	ppm/ °C	1

*1. $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 3 to 4**.)

*2. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^{\circ}\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^{\circ}\text{C}]^{*3} \div 1000$$

*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

2-2. Detection Voltage Typ.1.5 V or More Products

Table 17

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage ^{*1}	−V _{DET}	—		−V _{DET(S)} ×0.98	−V _{DET(S)}	−V _{DET(S)} ×1.02	V	1
Hysteresis width	V _{HYS}	—		−V _{DET} ×0.03	−V _{DET} ×0.05	−V _{DET} ×0.08	V	1
Current consumption	I _{SS}	V _{DD} = 3.5 V	S-80815 to 26	—	0.8	2.4	μA	2
		V _{DD} = 4.5 V	S-80827 to 39	—	0.8	2.4	μA	2
		V _{DD} = 6.0 V	S-80840 to 56	—	0.9	2.7	μA	2
		V _{DD} = 7.5 V	S-80857 to 60	—	0.9	2.7	μA	2
Operating voltage	V _{DD}	—		0.95	—	10.0	V	1
Output current	I _{OUT}	Output transistor, Nch, V _{DS} = 0.5 V	V _{DD} = 1.2 V S-80815 to 60	0.59	1.36	—	mA	3
			V _{DD} = 2.4 V S-80827 to 60	2.88	4.98	—	mA	3
		Output transistor, Pch, V _{DS} = 0.5 V	V _{DD} = 4.8 V S-80815 to 39	1.43	2.39	—	mA	4
			V _{DD} = 6.0 V S-80840 to 56	1.68	2.78	—	mA	4
			V _{DD} = 8.4 V S-80857 to 60	2.08	3.42	—	mA	4
Response time	t _{PLH}	—		—	—	60	μs	1
Detection voltage temperature coefficient ^{*2}	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40 to +85 °C		—	±100	±350	ppm/°C	1

*1. $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 3 to 4**.)

*2. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^{\circ}\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^{\circ}\text{C}]^{*3} \div 1000$$

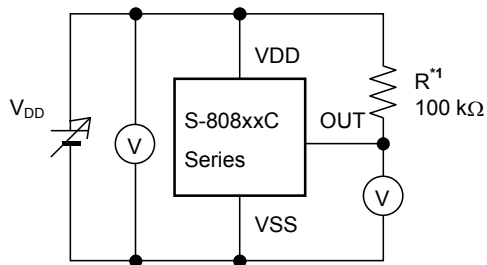
*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

■ Test Circuits

1.



*1. R is unnecessary for CMOS output products.

Figure 11

2.

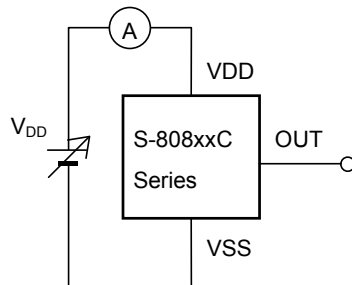


Figure 12

3.

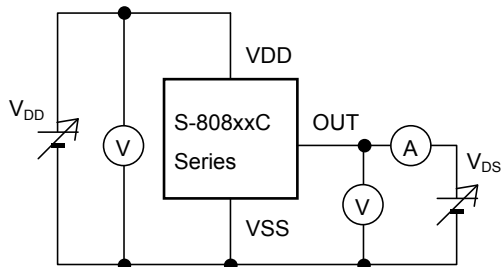


Figure 13

4.

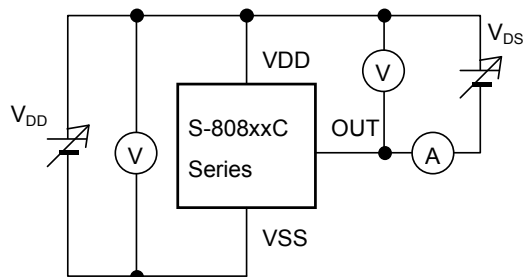


Figure 14

■ Timing Chart

1. Nch Open-drain Output Products

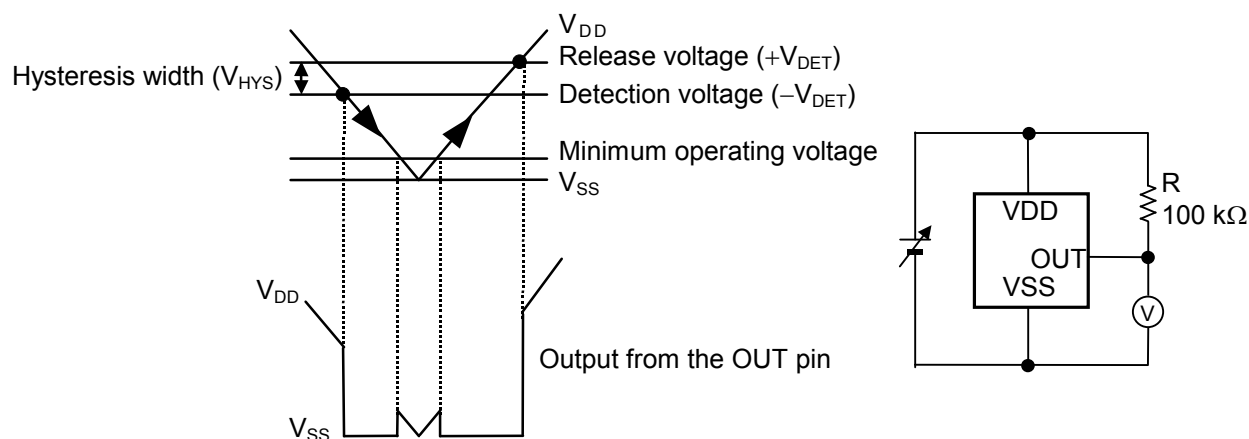
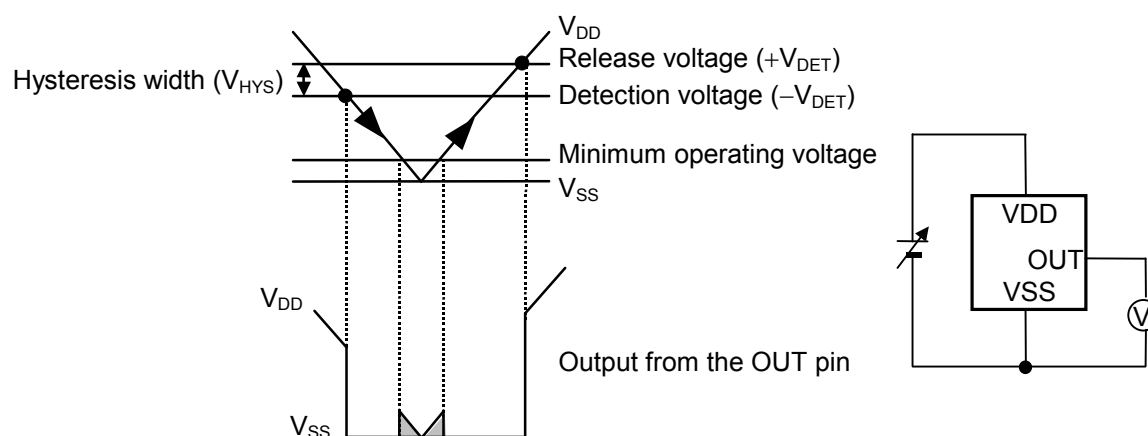


Figure 15

2. CMOS Output Products



Remark For values of V_{DD} less than minimum operating voltage, values of OUT terminal output is free in the shaded region.

Figure 16

■ Operation

1. Basic Operation: CMOS Output (Active Low)

1-1. When the power supply voltage (V_{DD}) is higher than the release voltage ($+V_{DET}$), the Nch transistor is OFF and the Pch transistor is ON to provide V_{DD} (high) at the output. Since the Nch transistor N1 in

Figure 17 is OFF, the comparator input voltage is $\frac{(R_B + R_C) \cdot V_{DD}}{R_A + R_B + R_C}$.

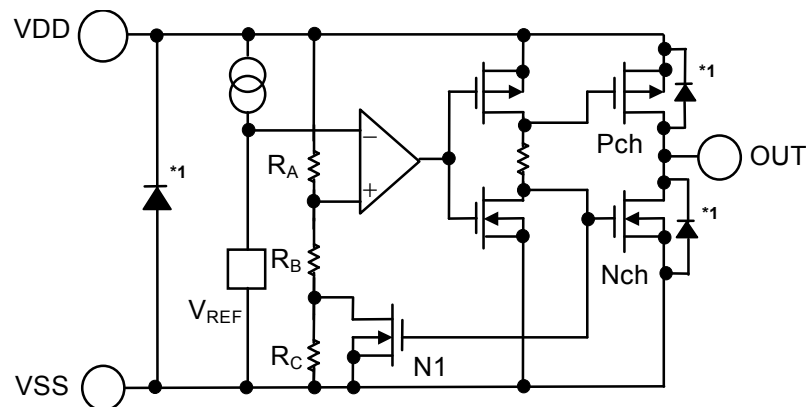
1-2. When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as the V_{DD} remains above the detection voltage $-V_{DET}$. When the V_{DD} falls below $-V_{DET}$ (point A in **Figure 18**), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the V_{SS} level appears at the output. At this time the Nch transistor N1 in **Figure 17** becomes ON, the comparator input voltage is changed to

$$\frac{R_B \cdot V_{DD}}{R_A + R_B}$$

1-3. When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to the V_{DD} when the output is pulled up to the V_{DD} .

1-4. The V_{SS} level appears when the V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when the V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

1-5. When the V_{DD} rises above $+V_{DET}$ (point B in **Figure 18**), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide V_{DD} level at the output.



*1. Parasitic diode

Figure 17 Operation 1

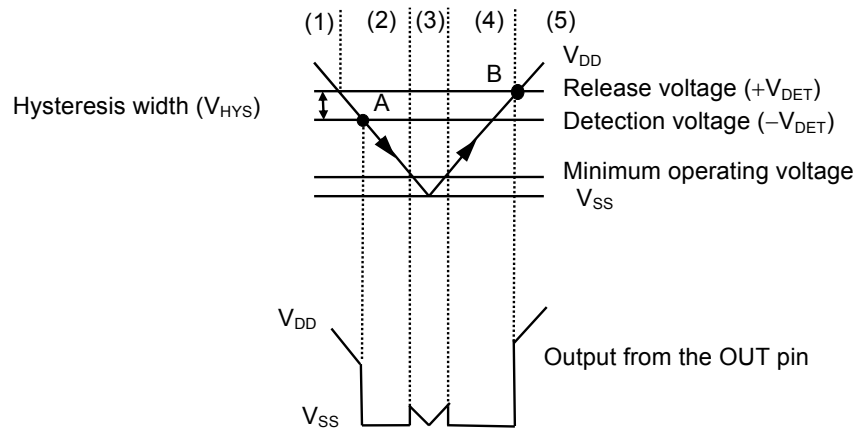
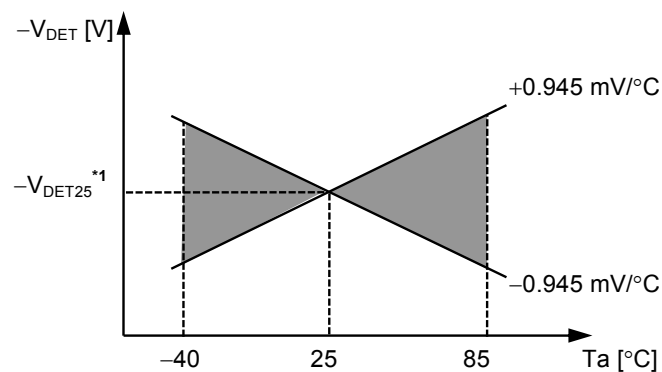


Figure 18 Operation 2

2. Other Characteristics

2-1. Temperature Characteristics of Detection Voltage

The shaded area in **Figure 19** shows the temperature characteristics of the detection voltage.



*1. $-V_{DET25}$ is an actual detection voltage value at 25°C.

Figure 19 Temperature Characteristics of Detection Voltage (Example for S-80827C)

2-2. Temperature Characteristics of Release Voltage

The temperature change $\frac{\Delta + V_{DET}}{\Delta T_a}$ of the release voltage is calculated by using the temperature

change $\frac{\Delta - V_{DET}}{\Delta T_a}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta T_a} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta T_a}$$

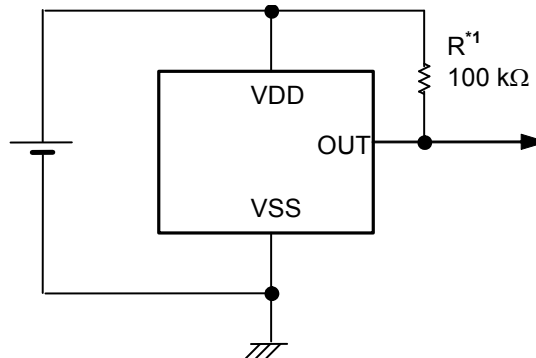
The temperature change of the release voltage and the detection voltage have the same sign consequently.

2-3. Temperature Characteristics of Hysteresis Voltage

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta T_a} - \frac{\Delta - V_{DET}}{\Delta T_a}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta T_a} - \frac{\Delta - V_{DET}}{\Delta T_a} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta T_a}$$

■ Standard Circuit



*1. R is unnecessary for CMOS output products.

Figure 20

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Technical Terms

1. Detection Voltage ($-V_{DET}$), Release Voltage ($+V_{DET}$)

The detection voltage ($-V_{DET}$) is a voltage at which the output turns to low. The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$) Min. and the maximum ($-V_{DET}$) Max. is called the detection voltage range (Refer to **Figure 21**).

Example: For the S-80815CN, the detection voltage lies in the range of $1.470 \leq (-V_{DET}) \leq 1.530$.
This means that some S-80815CNs have 1.470 V for $-V_{DET}$ and some have 1.530 V.

The release voltage ($+V_{DET}$) is a voltage at which the output turns to high. The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$) Min. and the maximum ($+V_{DET}$) Max. is called the release voltage range (Refer to **Figure 22**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is expressed by $-V_{DET} \times 1.03 \leq +V_{DET} \leq -V_{DET} \times 1.08$.

Example: For the S-80815CN, the release voltage lies in the range of $1.514 \leq (+V_{DET}) \leq 1.652$.
This means that some S-80815CNs have 1.514 V for $+V_{DET}$ and some have 1.652 V.

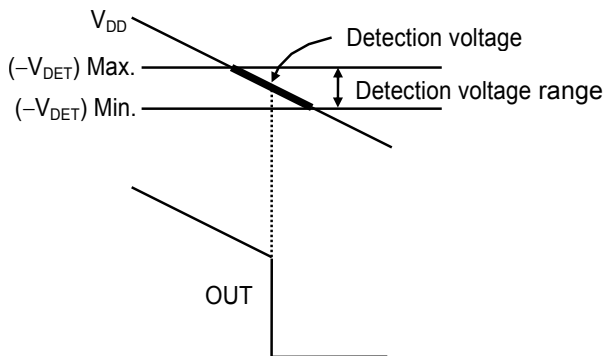


Figure 21 Detection Voltage (CMOS Output Products)

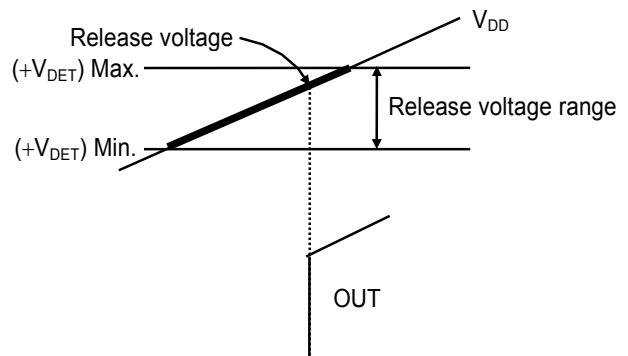


Figure 22 Release Voltage (CMOS Output Products)

Remark Although the detection voltage and release voltage overlap in the range of 1.514 V to 1.530 V, $+V_{DET}$ is always larger than $-V_{DET}$.

2. Hysteresis Width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (The voltage at point B – The voltage at point A = V_{HYS} in **Figure 18**). The existence of the hysteresis width prevents malfunction caused by noise on input signal.

3. Through-type Current

The through-type current refers to the current that flows instantaneously at the time of detection and release of a voltage detector. The through-type current is large in CMOS output products, small in Nch open-drain output products.

4. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 23**), taking a CMOS active low product for example, the through-type current which is generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the through-type current stops and its resultant voltage drop disappears, and the output goes from low to high. A through-type current is again generated, a voltage drop appears, and repeating the process finally induces oscillation.

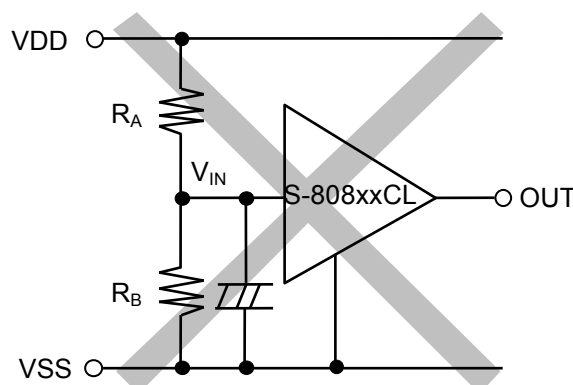


Figure 23 An Example for Bad Implementation of Input Voltage Divider

■ **Electrical Characteristics for Customized Products**

1. S-80824KNUA-D2BT2x, S-80824KNY-n2-U

Table 18

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Detection voltage ^{*1}	$-V_{DET}$	—	2.295	2.400 ^{*2}	2.505	V	1
Release voltage	$+V_{DET}$	—	4.300	4.400	4.500	V	1
Current consumption	I_{SS}	$V_{DD}=6.0\text{ V}$	—	0.8	2.4	μA	2
Operating voltage	V_{DD}	—	0.95	—	10.0	V	1
Output current	I_{OUT}	Output transistor, $V_{DD} = 0.95\text{ V}$	0.03	0.24	—	mA	3
		Nch, $V_{DS} = 0.5\text{ V}$ $V_{DD} = 1.2\text{ V}$	0.23	0.50	—	mA	3
Leakage current	I_{LEAK}	Output transistor, Nch, $V_{DD} = 10.0\text{ V}$, $V_{DS} = 10.0\text{ V}$	—	—	0.1	μA	3
Response time	t_{PLH}	—	—	—	60	μs	1
Detection voltage temperature coefficient ^{*3}	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	$Ta = -40\text{ to }85\text{ }^{\circ}\text{C}$	—	±100	±350	ppm/°C	1

*1. $-V_{DET}$: Actual detection voltage value

*2. Specified detection voltage value ($-V_{DET(S)}$)

*3. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^{\circ}\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^{\circ}\text{C}]^{*3} \div 1000$$

*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

2. S-80844KLUA-D2AT2x, S-80844KLY-n2-U

Table 19

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage ^{*1}	−V _{DET}	—		4.295	4.450 ^{*2}	4.605	V	1
Release voltage	+V _{DET}	—		—	—	4.700	V	1
Current consumption	I _{SS}	V _{DD} = 6.0 V		—	1.0	3.0	μA	2
Operating voltage	V _{DD}	—		0.95	—	10.0	V	1
Output current	I _{OUT}	Output transistor, Nch, V _{DS} = 0.5 V	V _{DD} = 1.2 V	0.23	0.50	—	mA	3
			V _{DD} = 2.4 V	1.60	3.70	—	mA	3
		Output transistor, Pch, V _{DS} = 0.5 V	V _{DD} = 4.8 V	0.36	0.62	—	mA	4
Response time	t _{PLH}	—		—	—	60	μs	1
Detection voltage temperature coefficient ^{*3}	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40 to 85 °C		—	±100	±350	ppm/°C	1

*1. $-V_{DET}$: Actual detection voltage value

*2. Specified detection voltage value ($-V_{DET(S)}$)

*3. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV/°C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm/°C}]^{*3} \div 1000$$

*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

3. S-80846KNUA-D2CT2x, S-80846KNY-n2-U

Table 20

(Ta = 25 °C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Detection voltage ^{*1}	$-V_{DET}$	—	4.500	4.600 ^{*2}	4.700	V	1
Hysteresis width	V_{HYS}	—	—	0.05	0.10	V	1
Current consumption	I_{SS}	$V_{DD} = 6.0 \text{ V}$	—	0.9	2.7	μA	2
Operating voltage	V_{DD}	—	0.95	—	10.0	V	1
Output current	I_{OUT}	Output transistor, $V_{DD} = 1.2 \text{ V}$	0.59	1.36	—	mA	3
		Nch, $V_{DS} = 0.5 \text{ V}$ $V_{DD} = 2.4 \text{ V}$	2.88	4.98	—	mA	3
Leakage current	I_{LEAK}	Output transistor, Nch, $V_{DD} = 10.0 \text{ V}$, $V_{DS} = 10.0 \text{ V}$	—	—	0.1	μA	3
Response time	t_{PLH}	—	—	—	60	μs	1
Detection voltage temperature coefficient ^{*3}	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	$Ta = -40 \text{ to } 85 \text{ } ^\circ\text{C}$	—	±100	±350	ppm/°C	1

*1. $-V_{DET}$: Actual detection voltage value

*2. Specified detection voltage value ($-V_{DET(S)}$)

*3. The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^\circ\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^\circ\text{C}]^{*3} \div 1000$$

*1. Temperature change of the detection voltage

*2. Specified detection voltage

*3. Detection voltage temperature coefficient

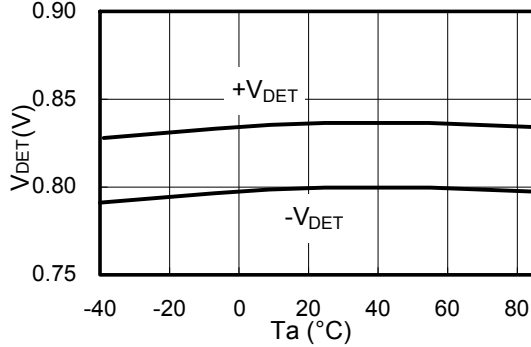
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output products of the S-808xxC series, the through-type current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the through-type current during releasing.
- In CMOS output products oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for the products on the circuits described herein.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

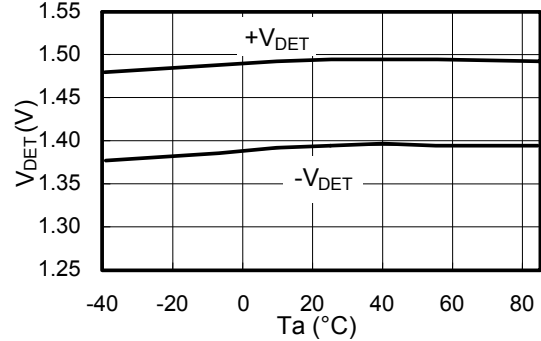
■ **Typical Characteristics (Typical Data)**

1. Detection Voltage (V_{DET}) - Temperature (T_a)

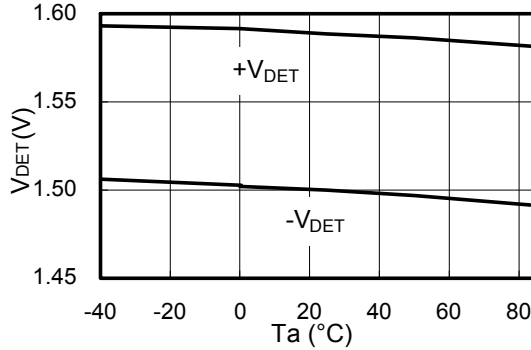
S-80808CL



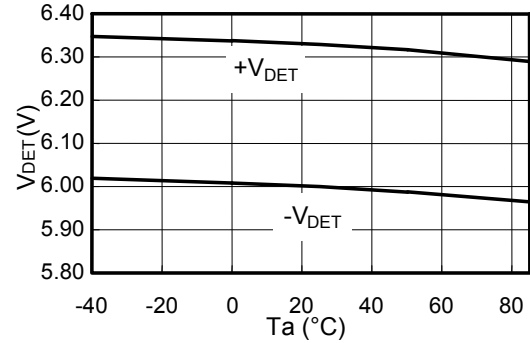
S-80814CL



S-80815CL

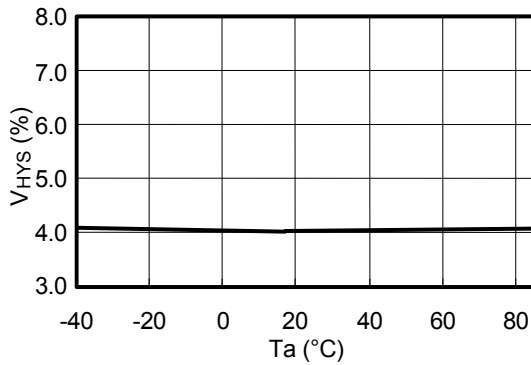


S-80860CL

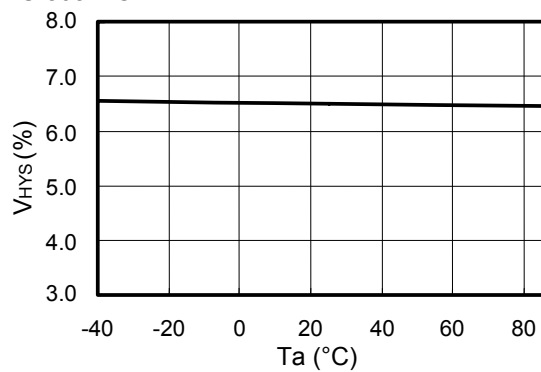


2. Hysteresis Voltage Width (V_{HYS}) - Temperature (T_a)

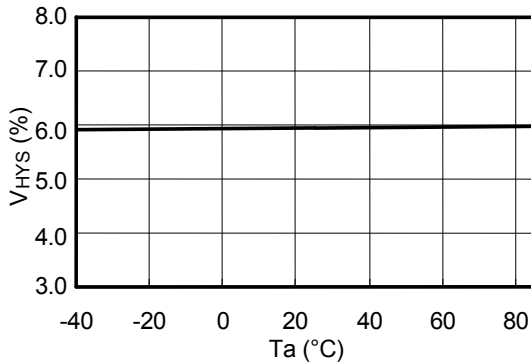
S-80808CL



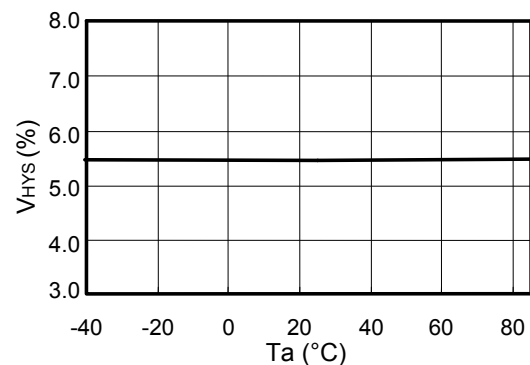
S-80814CL



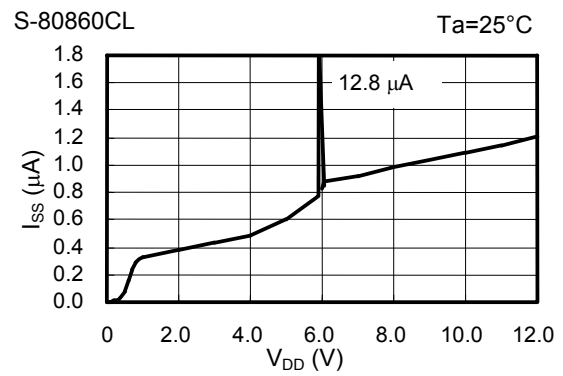
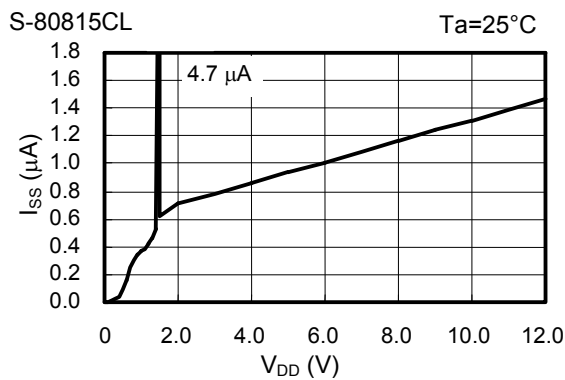
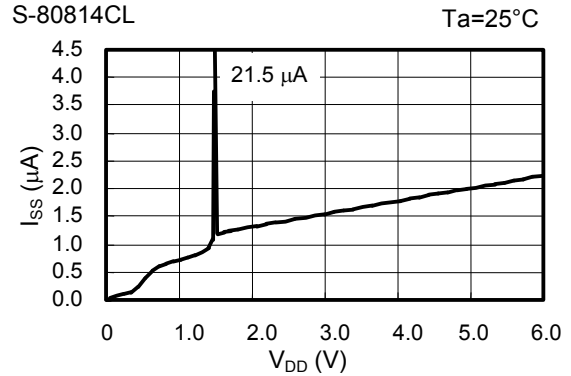
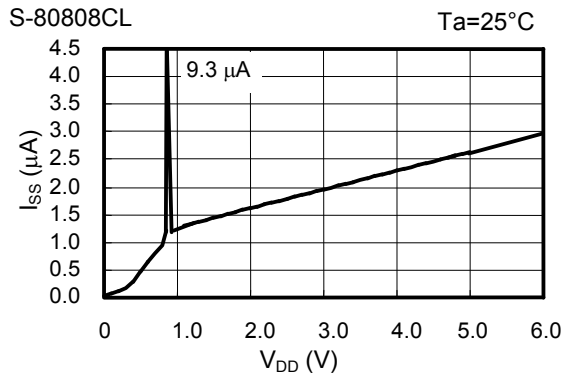
S-80815CL



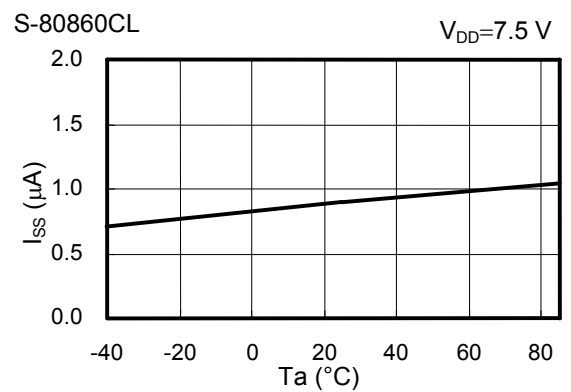
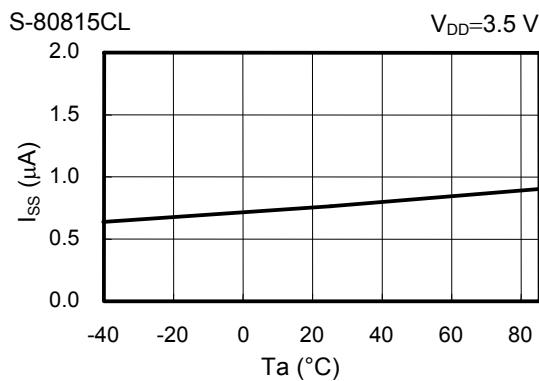
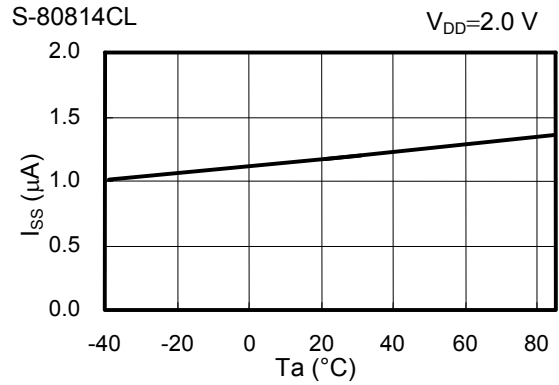
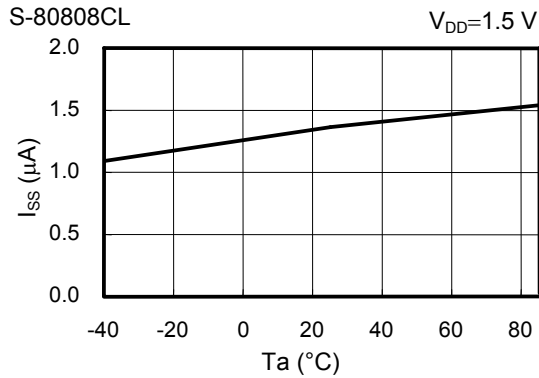
S-80860CL



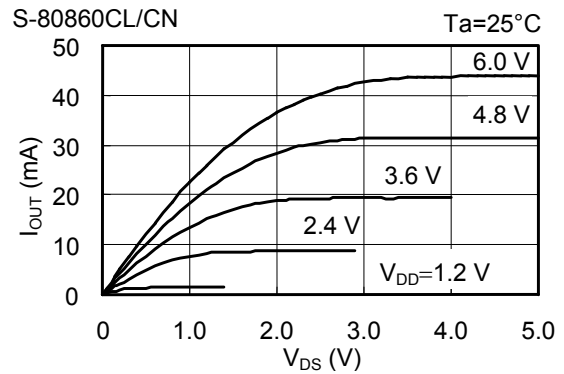
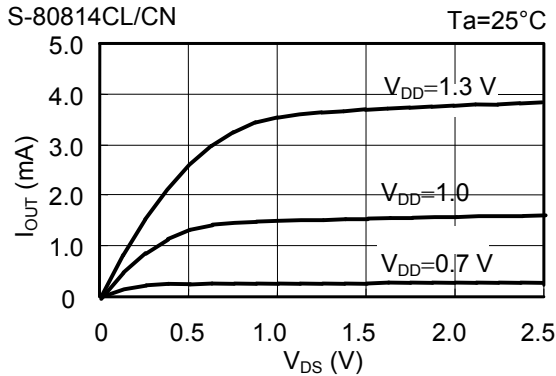
3. Current Consumption (I_{SS}) - Input Voltage (V_{DD})



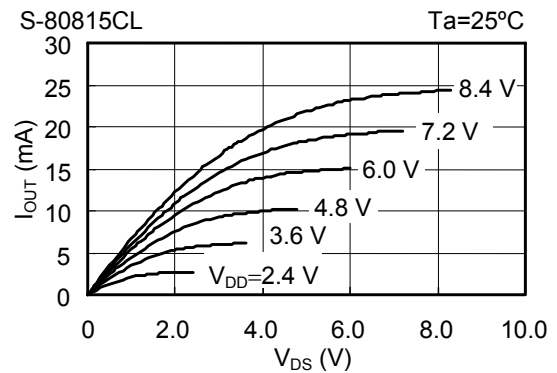
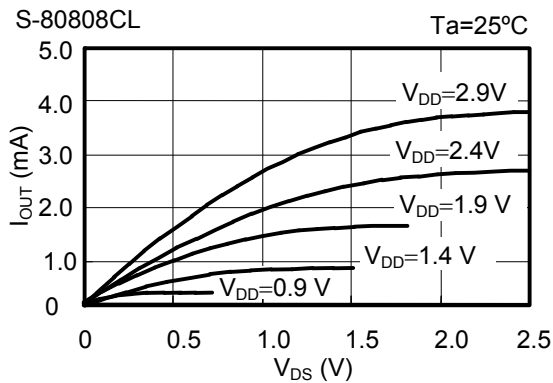
4. Current Consumption (I_{SS}) - Temperature (T_a)



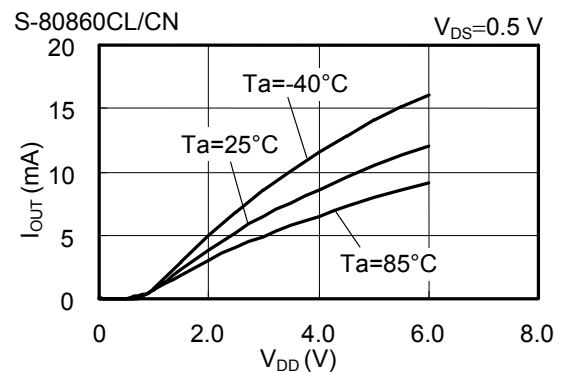
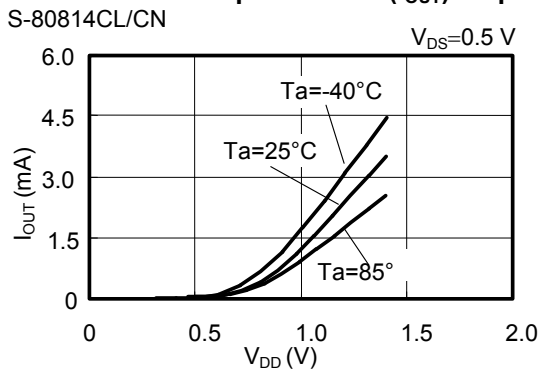
5. Nch Transistor Output Current (I_{OUT}) - V_{DS}



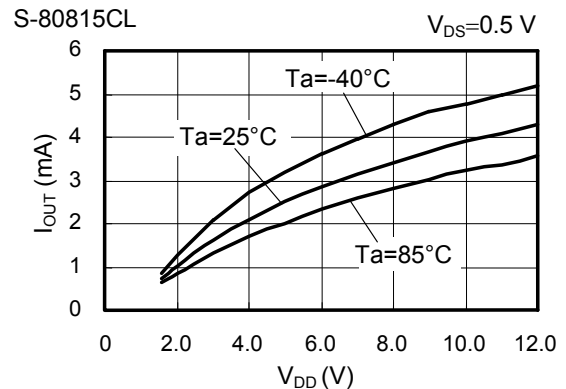
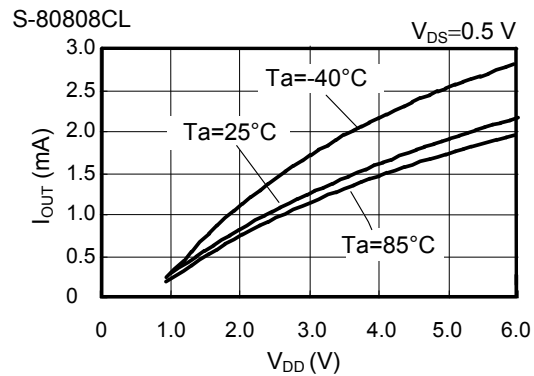
6. Pch Transistor Output Current (I_{OUT}) - V_{DS}



7. Nch Transistor Output Current (I_{OUT}) - Input Voltage (V_{DD})



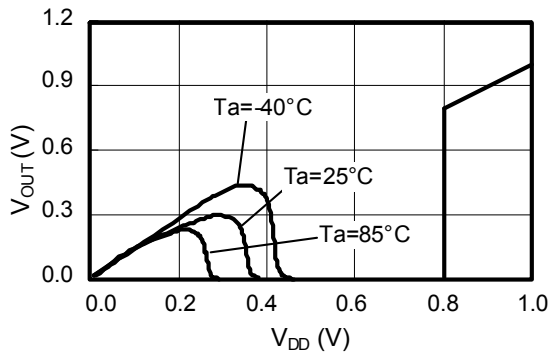
8. Pch Transistor Output Current (I_{OUT}) - Input Voltage (V_{DD})



9. Minimum Operating Voltage - Input Voltage (V_{DD})

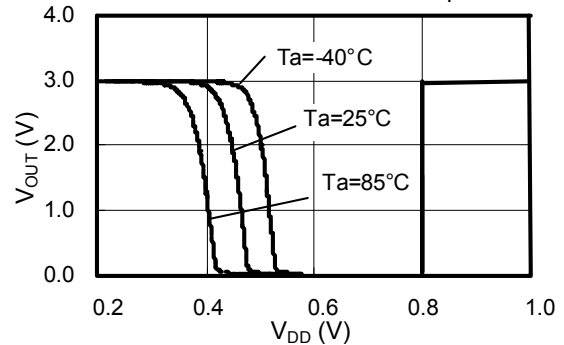
S-80808CN

Pull-up to V_{DD} 100 k Ω



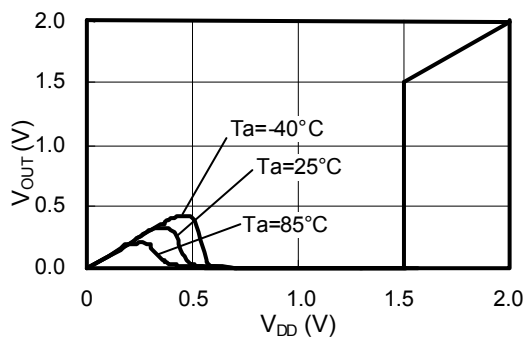
S-80808CN

Pull-up to 3 V



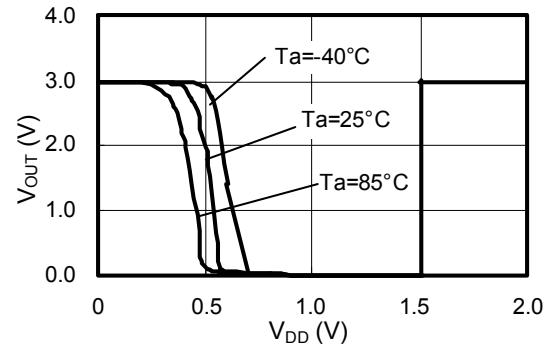
S-80815CN

Pull-up to V_{DD} 100 k Ω



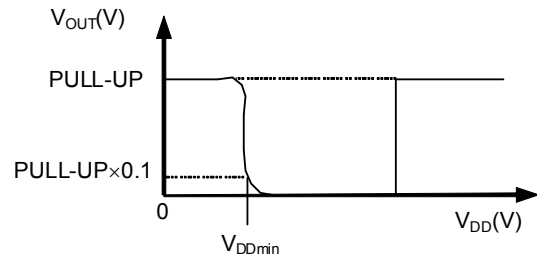
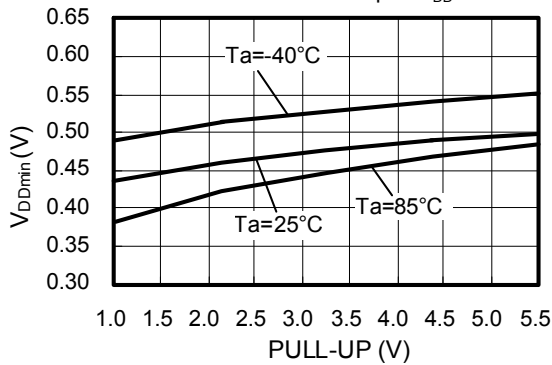
S-80815CN

Pull-up to 3 V



S-80808CN

Pull-up to V_{DD} :100 k Ω



Remark V_{DDmin} is defined by the V_{DD} voltage at which V_{OUT} goes below 10% of PULL-UP voltage when the V_{DD} increase from 0 V.

S-80815CN

Pull-up to V_{DD} :100 k Ω

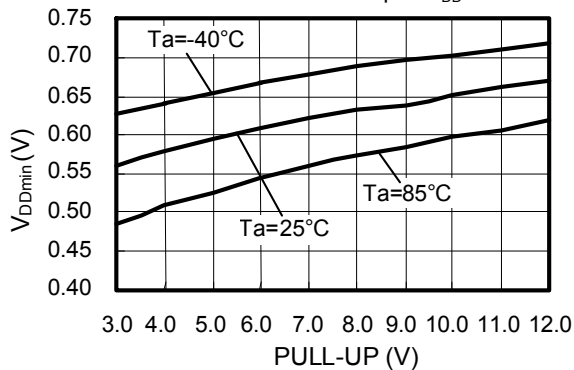
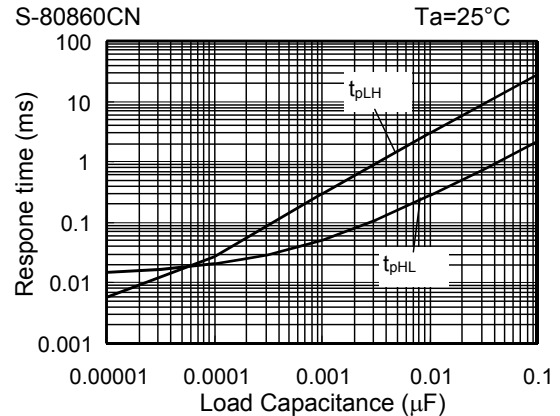
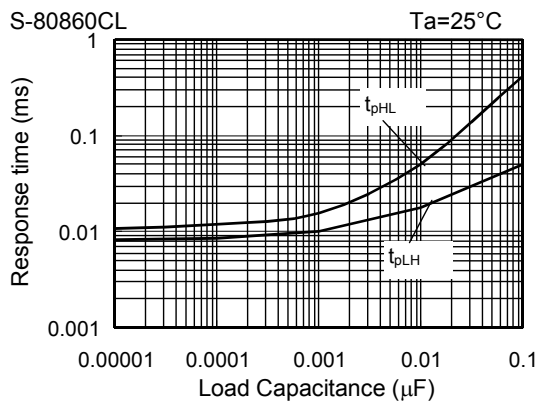
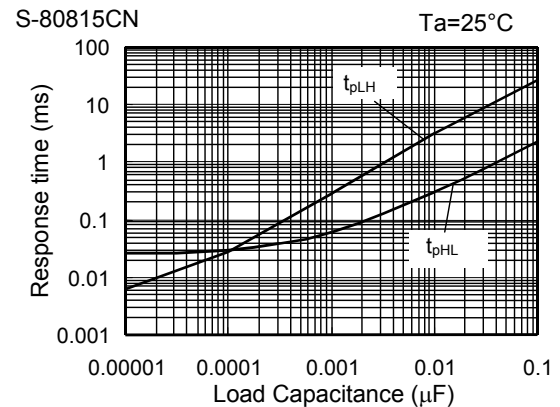
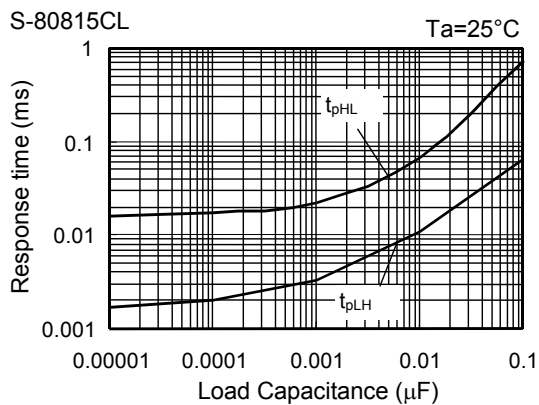
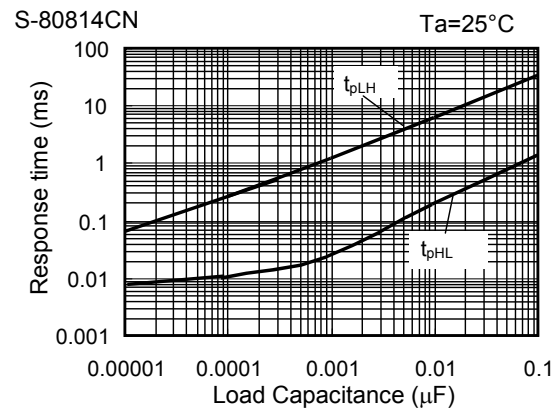
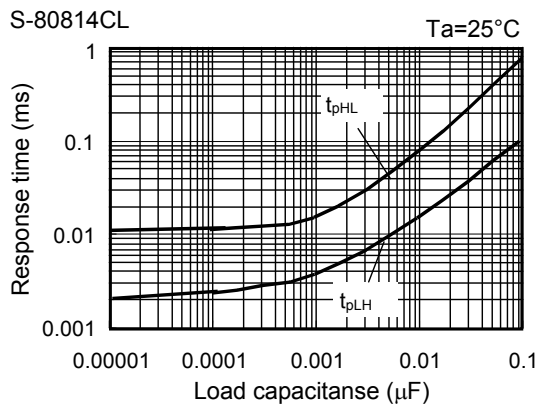
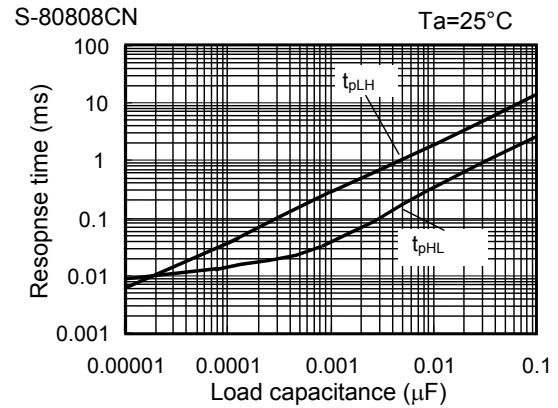
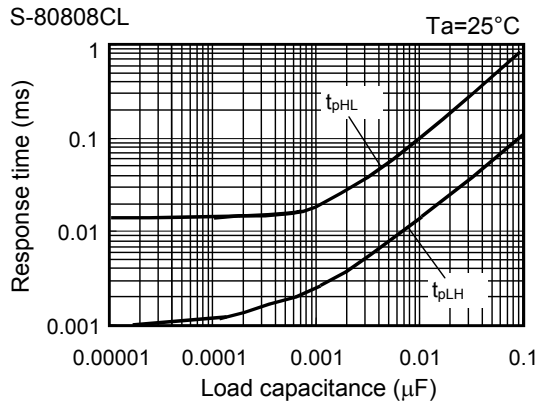


Figure 24

10. Dynamic Response - C_{OUT}



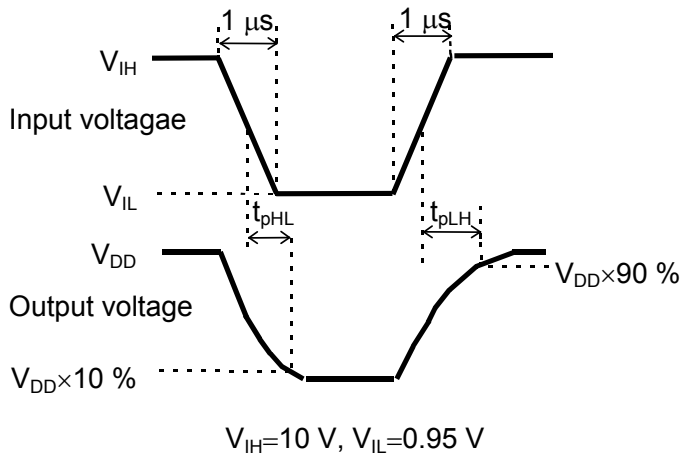
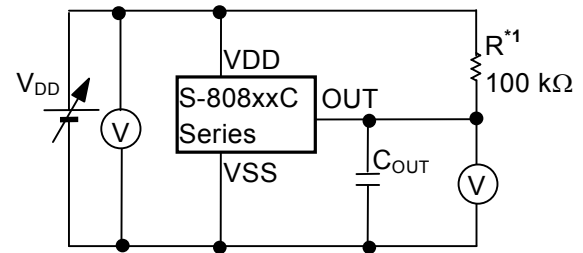


Figure 25 Measurement Condition for Response Time



*1. R is unnecessary for CMOS output products.

Figure 26 Measurement Circuit for Response Time

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

■ Application Circuit Examples

1. Microcomputer Reset Circuits

If the power supply voltage to a microcomputer falls below the specified level, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to normal, the microcomputer needs to be initialized before normal operations can be done. Reset circuits protect microcomputers in the event of current being momentarily switched off or lowered. Reset circuits shown in **Figures 27 to 28** can be easily constructed with the help of the S-808xxC series, that has low operating voltage, a high-precision detection voltage and hysteresis.

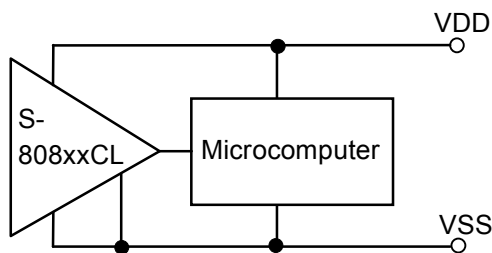
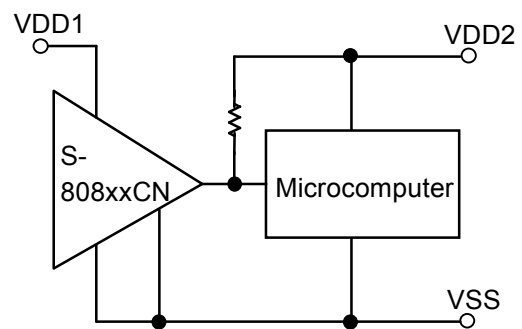


Figure 27 Reset Circuit Example (S-808xxCL)



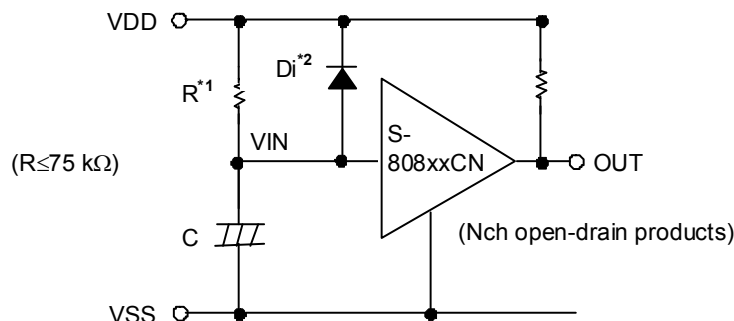
(Only for Nch open-drain products)

Figure 28 Reset Circuit Example (S-808xxCN)

Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

2. Power-on Reset Circuit

A power-on reset circuit can be constructed using Nch open-drain output product of S-808xxC Series.



- *1. Resistor R should be 75 kΩ or less to prevent oscillation.
- *2. Diode Di instantaneously discharges the charge stored in the capacitor (C) at the power falling, Di can be removed when the delay of the falling time is not important.

Figure 29

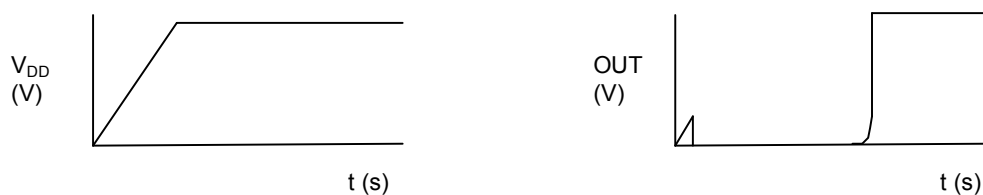


Figure 30

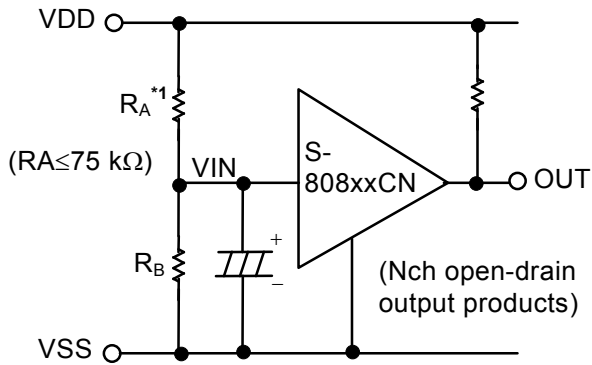
Remark When the power rises sharply as shown in the **Figure 31** left, the output may goes to the high level for an instant in the undefined region where the output voltage is undefined since the power voltage is less than the minimum operation voltage.



Figure 31

3. Change of Detection Voltage

In Nch open-drain output products of the S-808xxC series, detection voltage can be changed using resistance dividers or diodes as shown in **Figures 32 to 33**. In **Figure 32**, hysteresis width also changes.



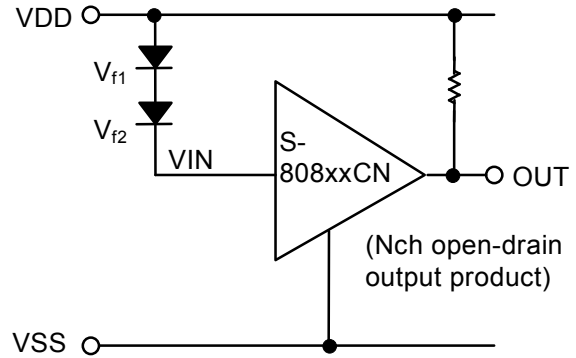
$$\text{Detection voltage} = \frac{R_A + R_B}{R_B} \cdot -V_{DET}$$

$$\text{Hysteresis width} = \frac{R_A + R_B}{R_B} \cdot V_{HYS}$$

*1. RA should be 75 kΩ or less to prevent oscillation.

Caution If RA and RB are large, the hysteresis width may also be larger than the value given by the above equation due to the through-type current (which flows slightly in an Nch open-drain product).

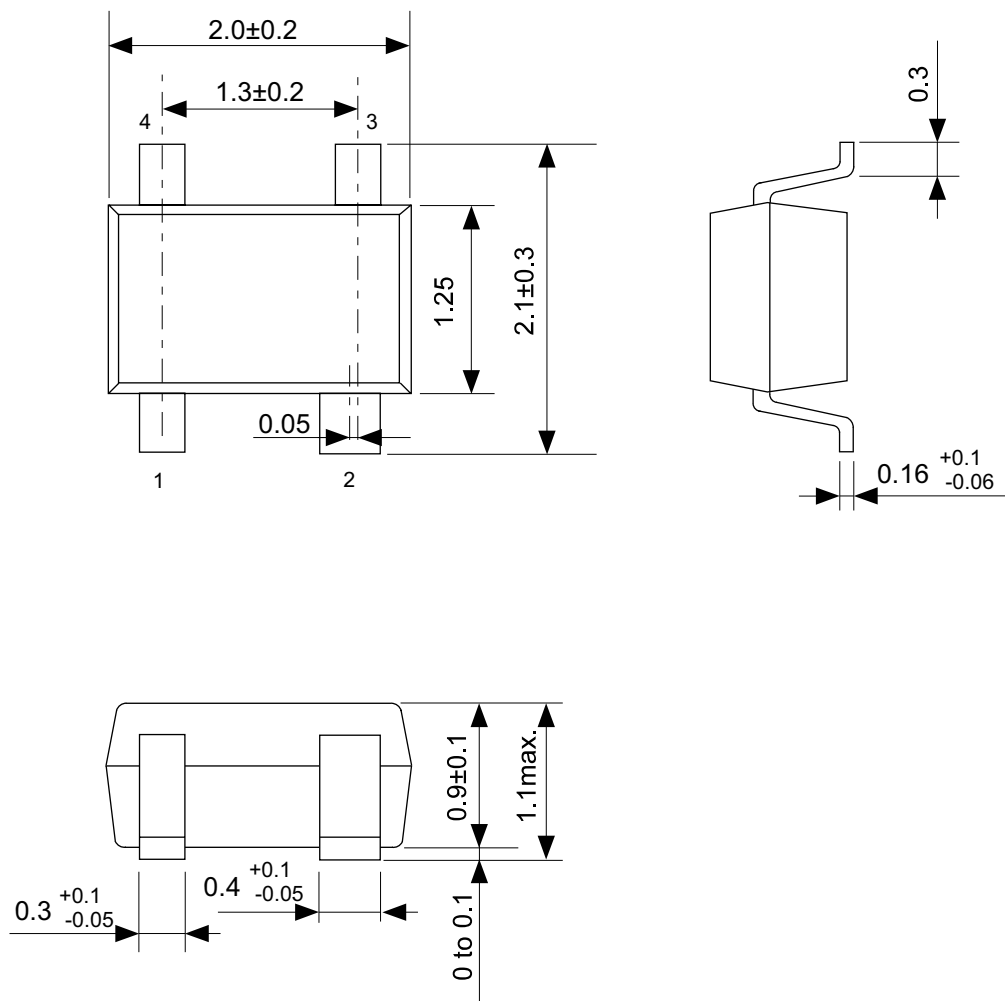
Figure 32



$$\text{Detection voltage} = V_{f1} + V_{f2} + (-V_{DET})$$

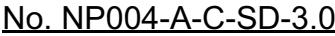
Figure 33

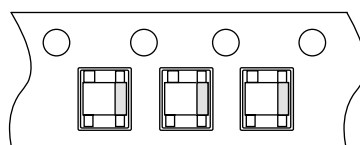
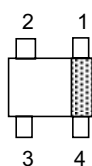
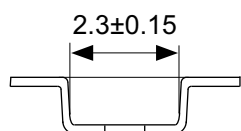
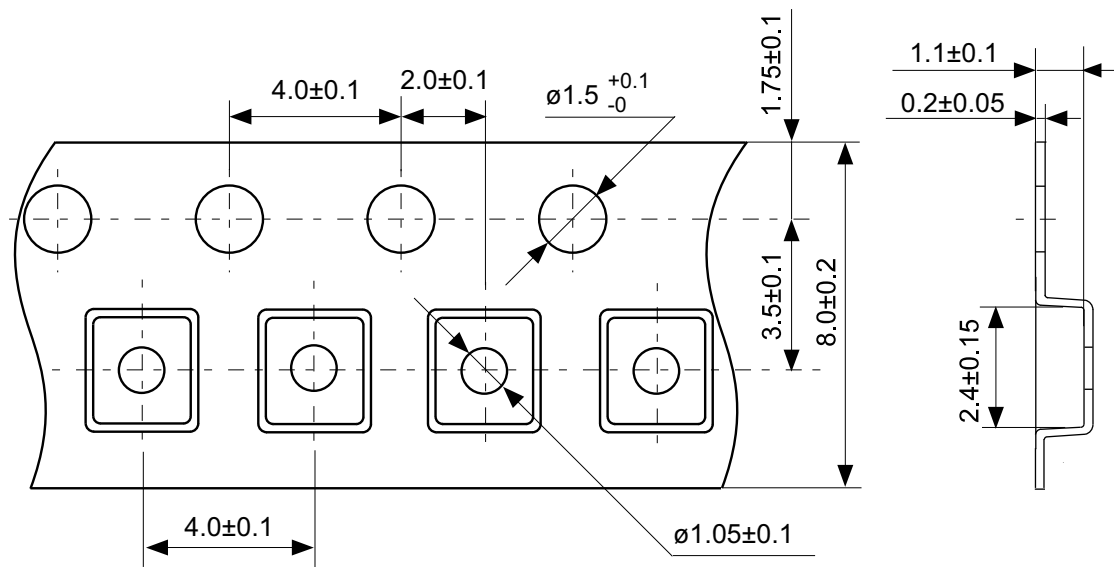
Caution The above connection diagram and constants do not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.



No. NP004-A-P-SD-2.0

TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

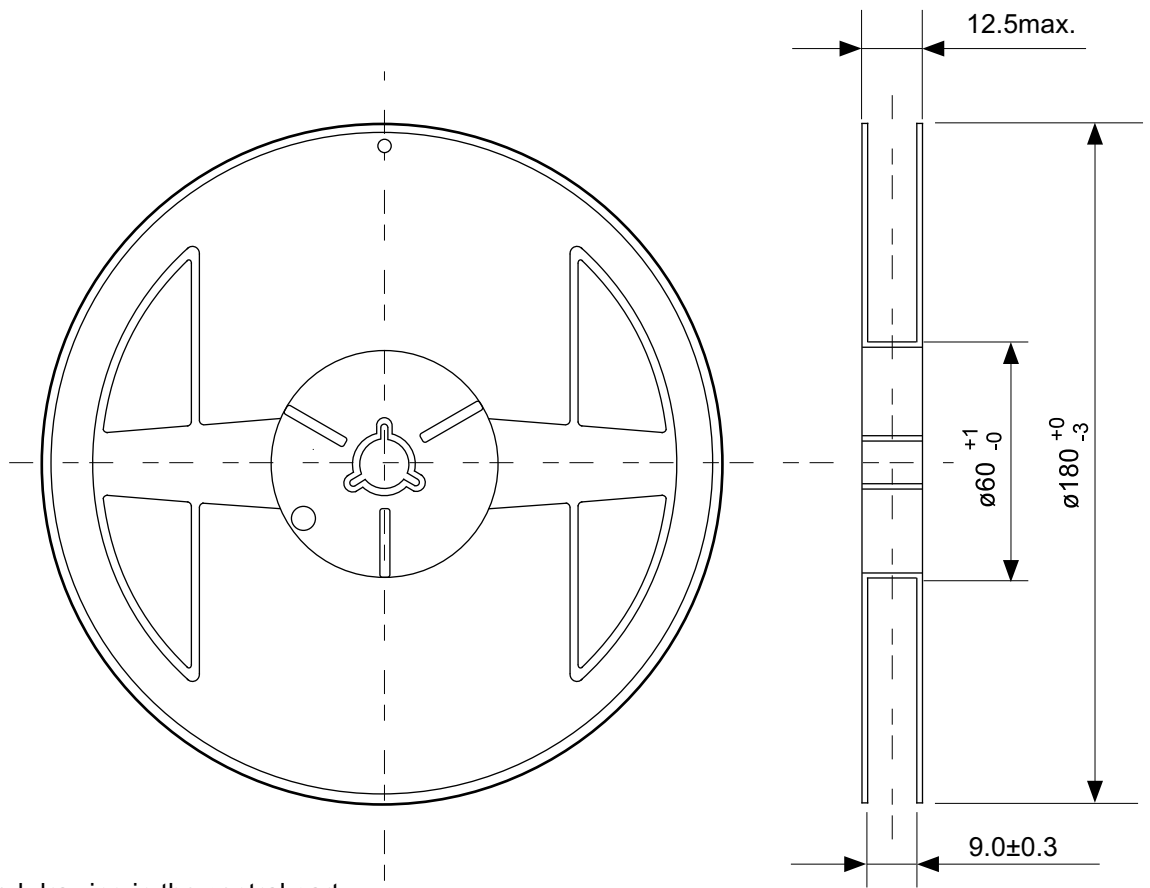




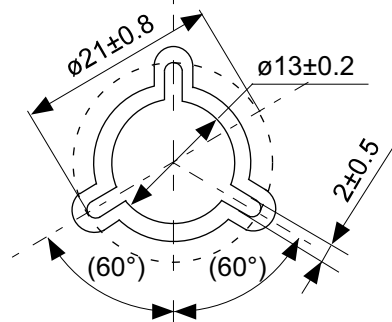
Feed direction

No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

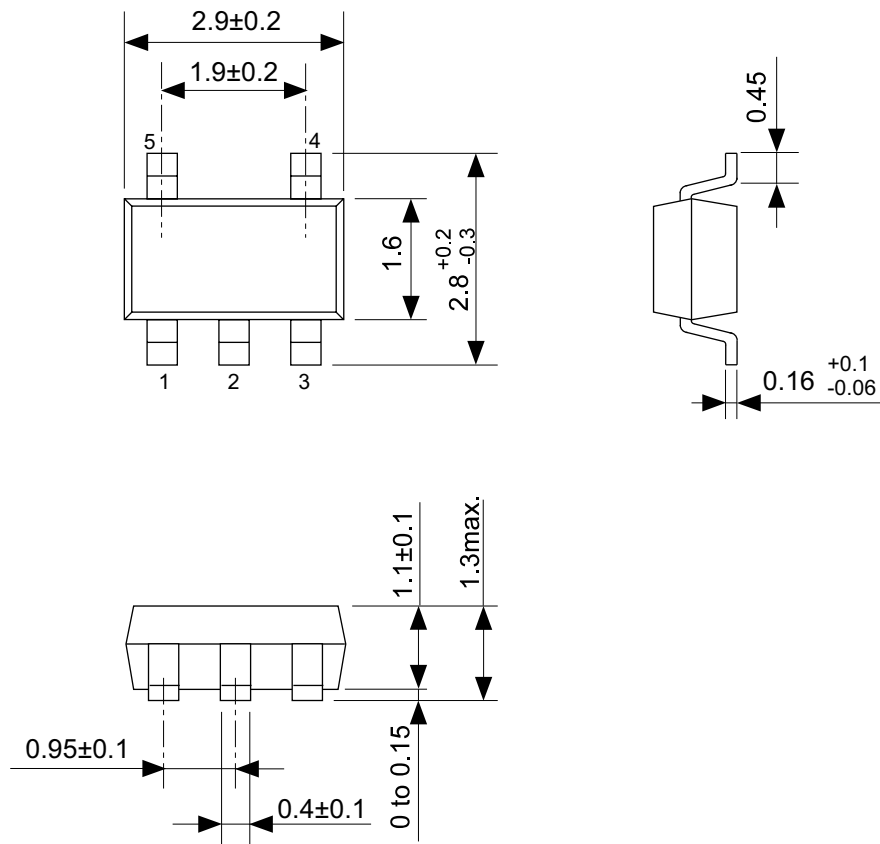


Enlarged drawing in the central part



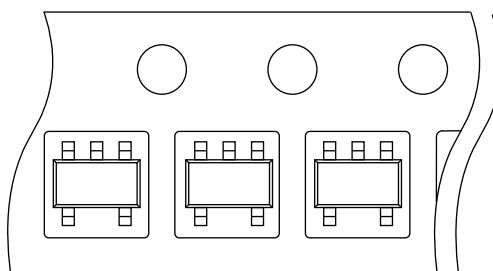
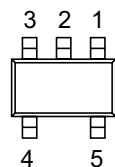
No. NP004-A-R-SD-1.1

TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm
ABLIC Inc.	



Feed direction →

No. MP005-A-C-SD-2.1

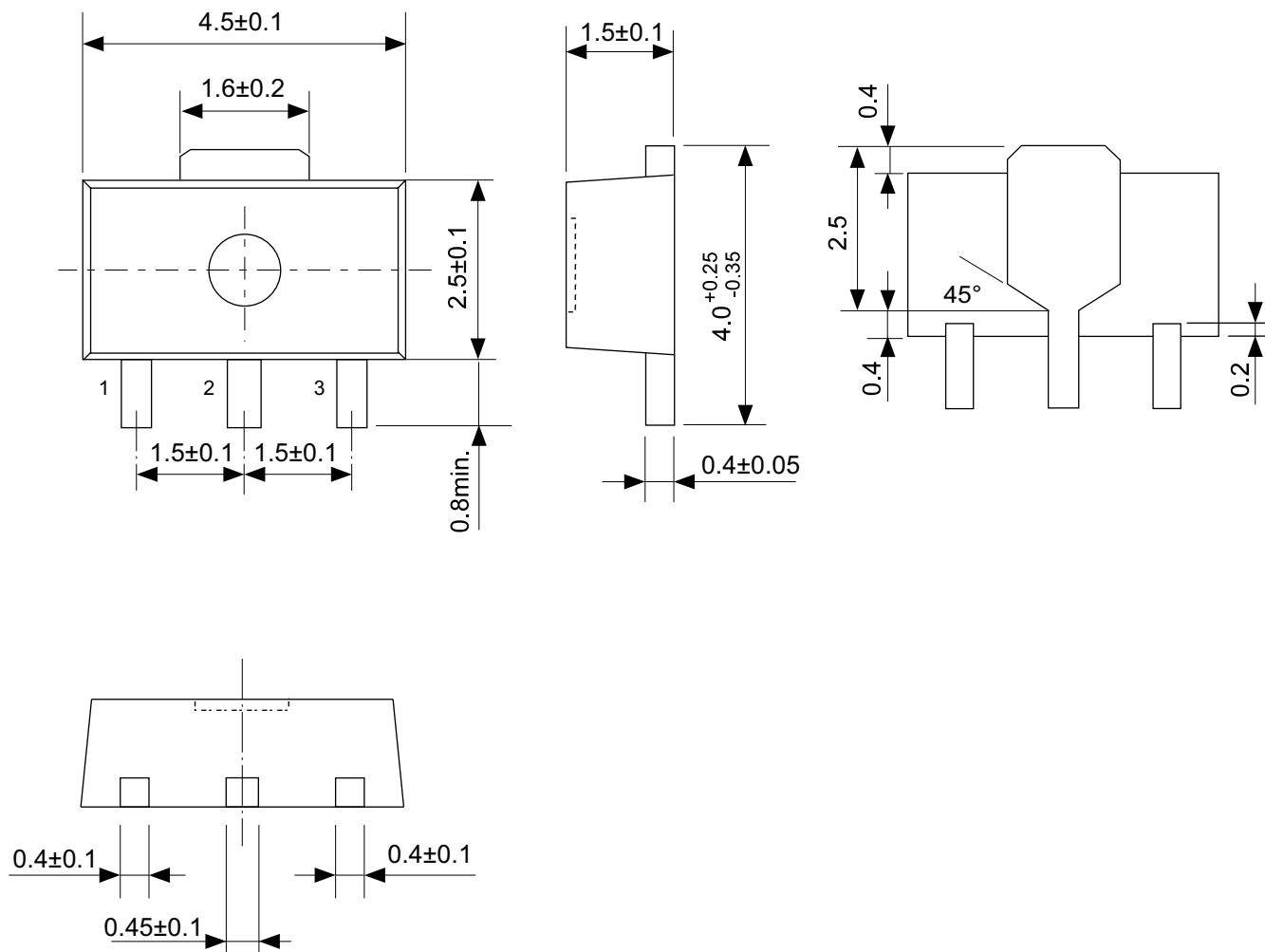
TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part

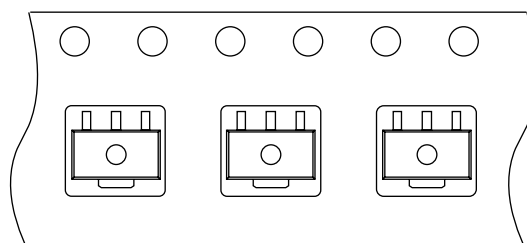
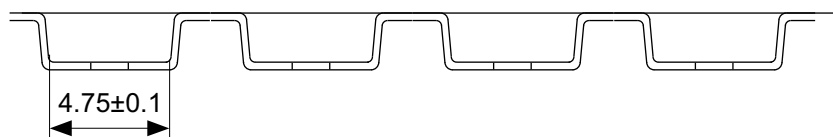
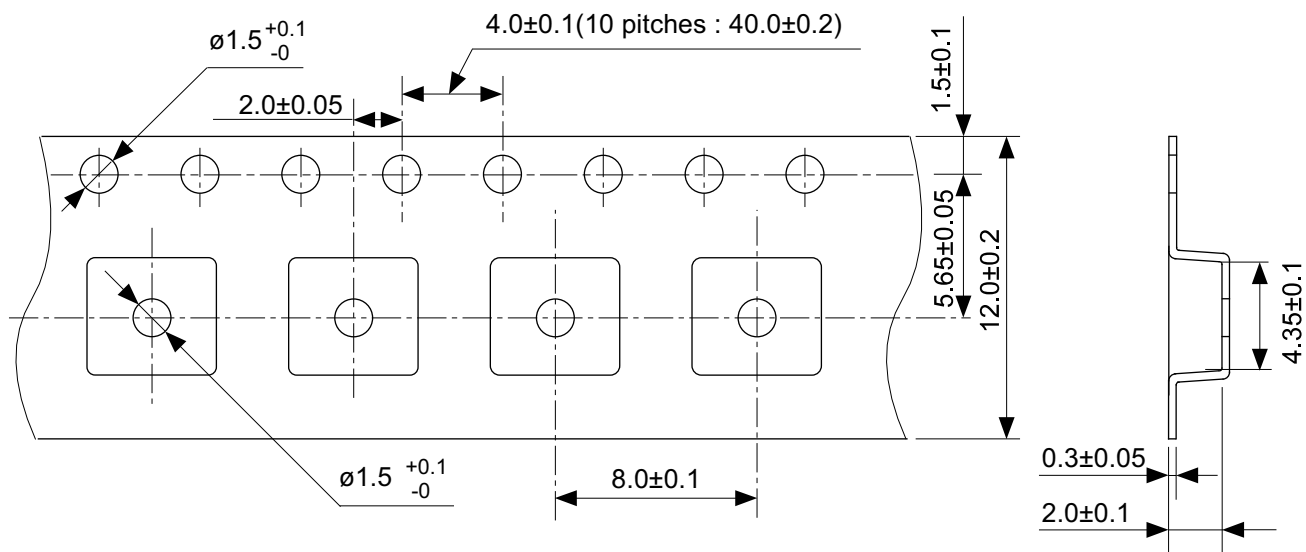
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



No. UP003-A-P-SD-2.0

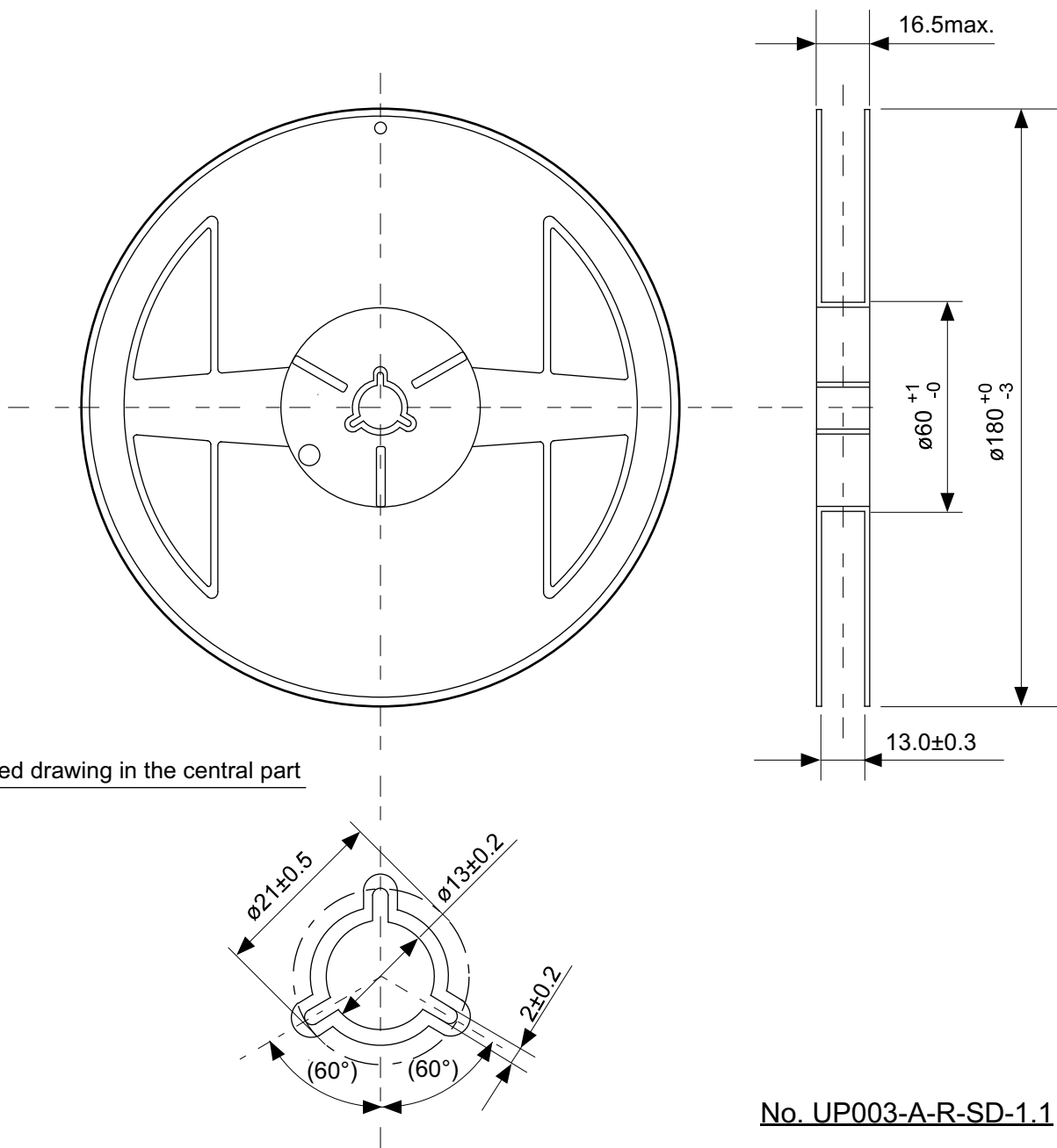
TITLE	SOT893-A-PKG Dimensions
No.	UP003-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



→
Feed direction

No. UP003-A-C-SD-2.0

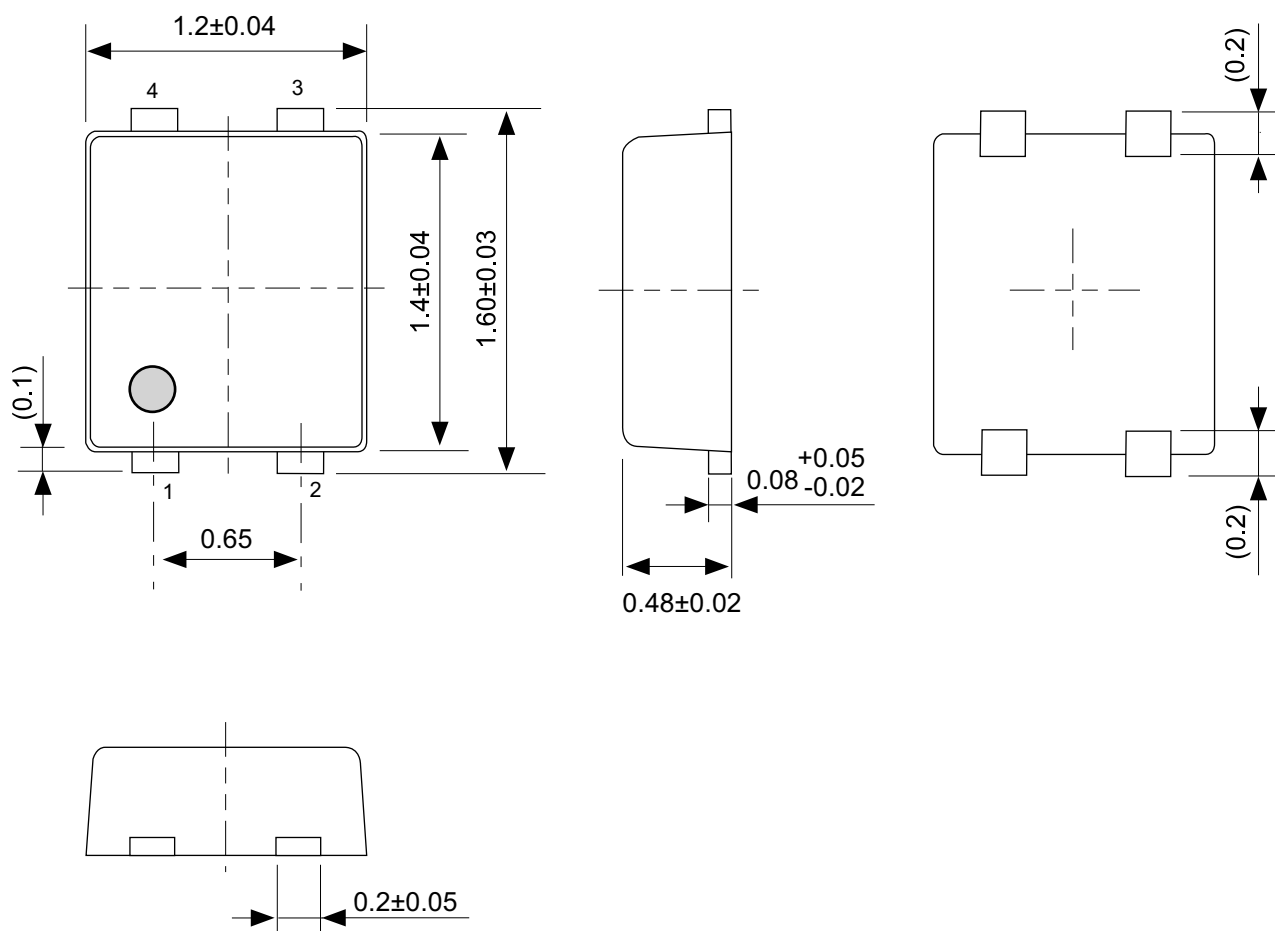
TITLE	SOT893-A-Carrier Tape
No.	UP003-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part

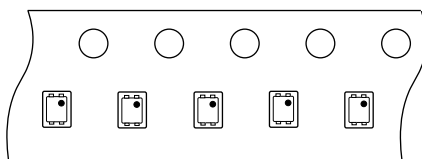
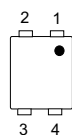
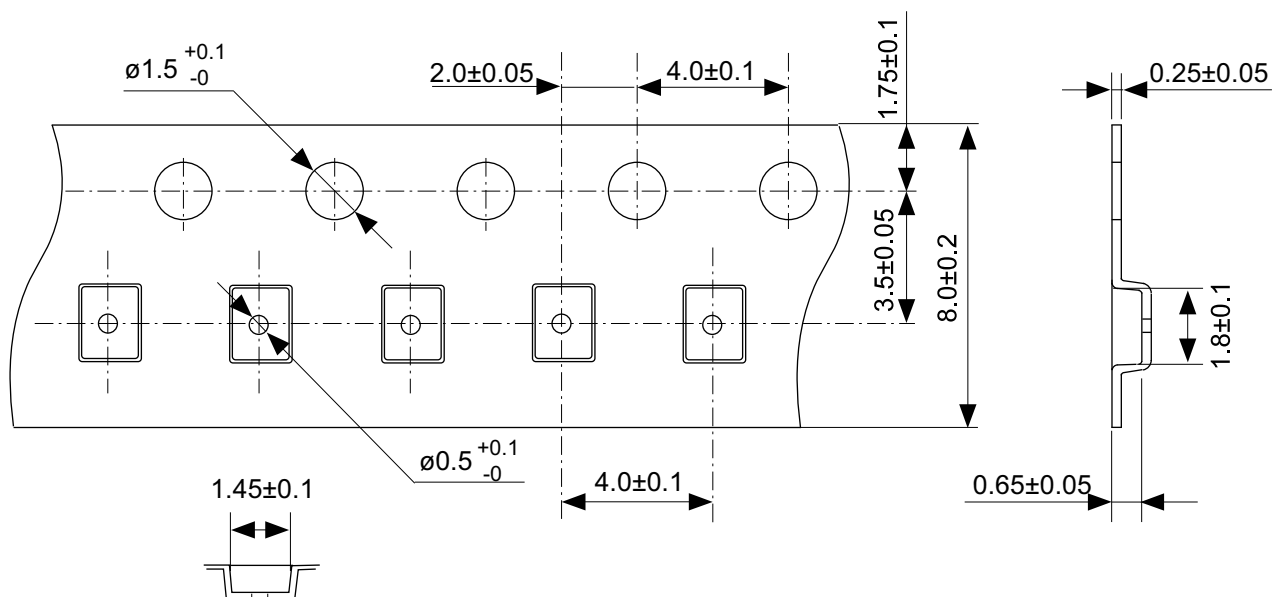
No. UP003-A-R-SD-1.1

TITLE	SOT893-A-Reel		
No.	UP003-A-R-SD-1.1		
ANGLE		QTY.	1,000
UNIT	mm		
ABLIC Inc.			



No. PF004-A-P-SD-6.0

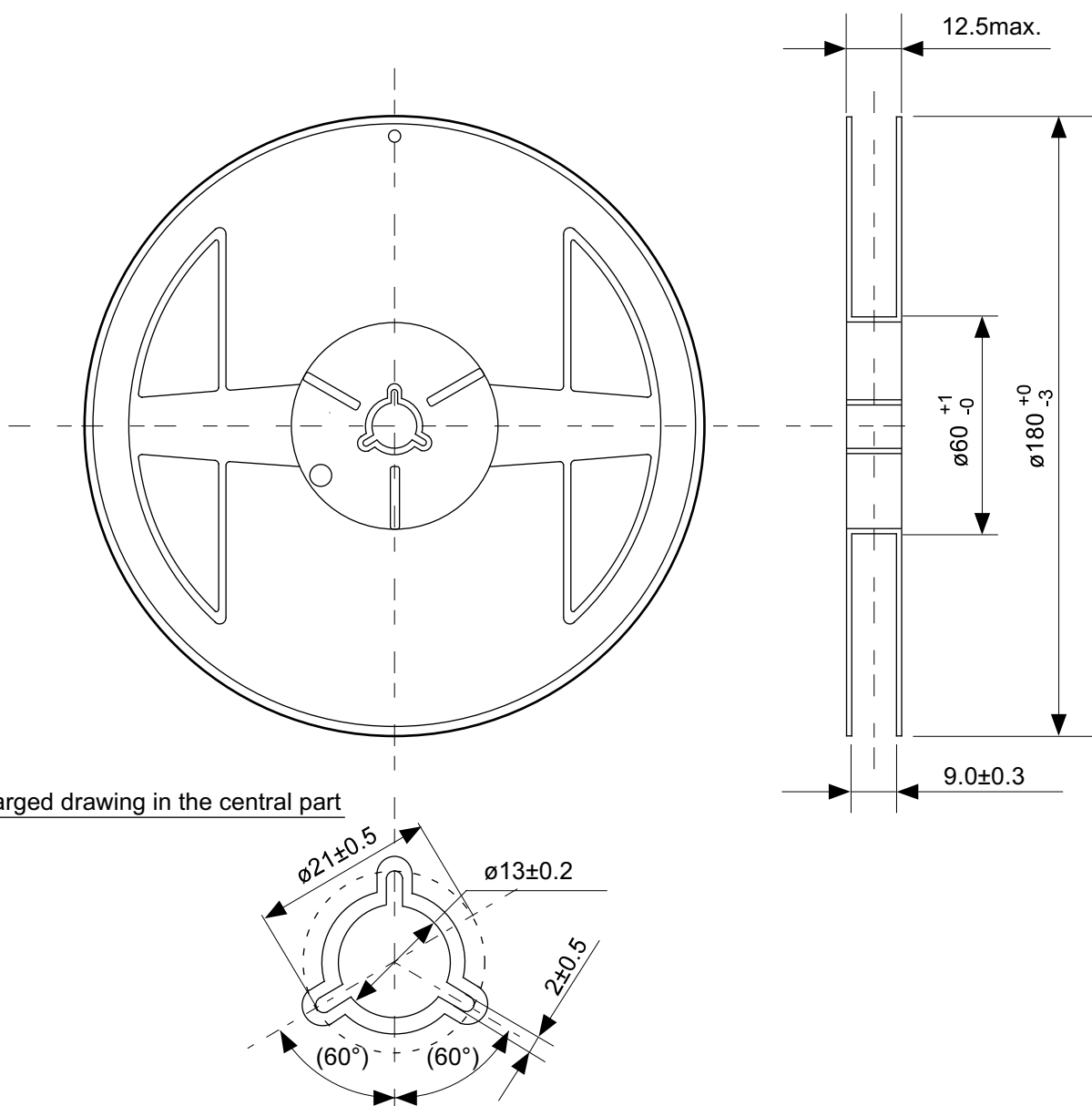
TITLE	SNT-4A-A-PKG Dimensions
No.	PF004-A-P-SD-6.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Feed direction

No. PF004-A-C-SD-2.0

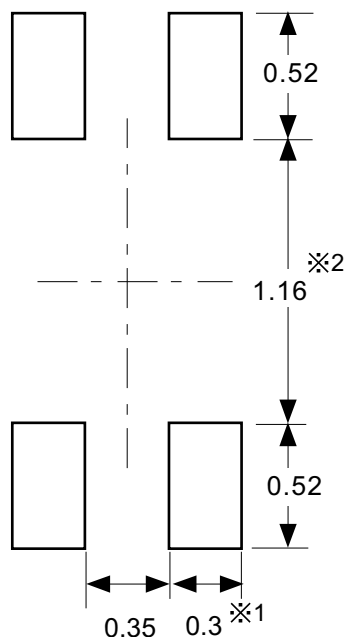
TITLE	SNT-4A-A-Carrier Tape
No.	PF004-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part

No. PF004-A-R-SD-1.0

TITLE	SNT-4A-A-Reel		
No.	PF004-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.).

※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

- 注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
 2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
 3. マスク開口サイズと開口位置はランドパターンと合わせてください。
 4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).

※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.

2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.

3. Match the mask aperture size and aperture position with the land pattern.

4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.).

※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。

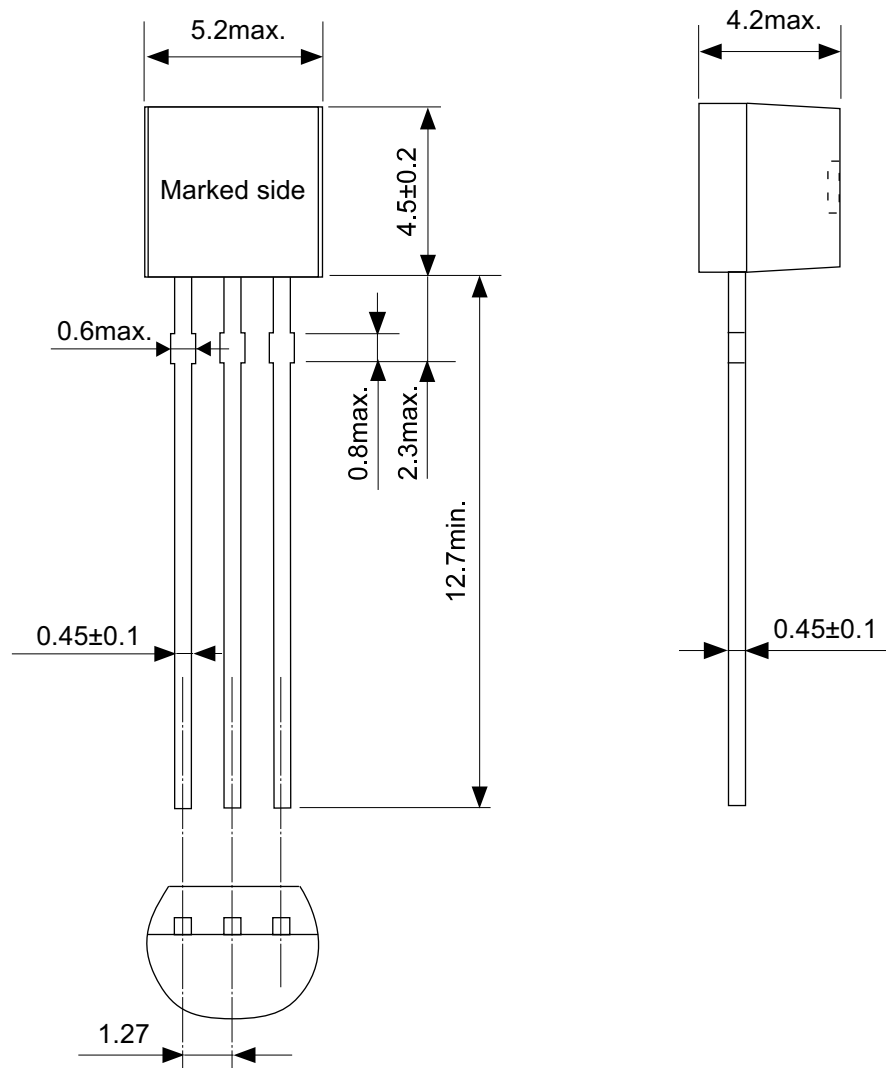
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。

3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。

4. 详细内容请参阅 "SNT 封装的应用指南"。

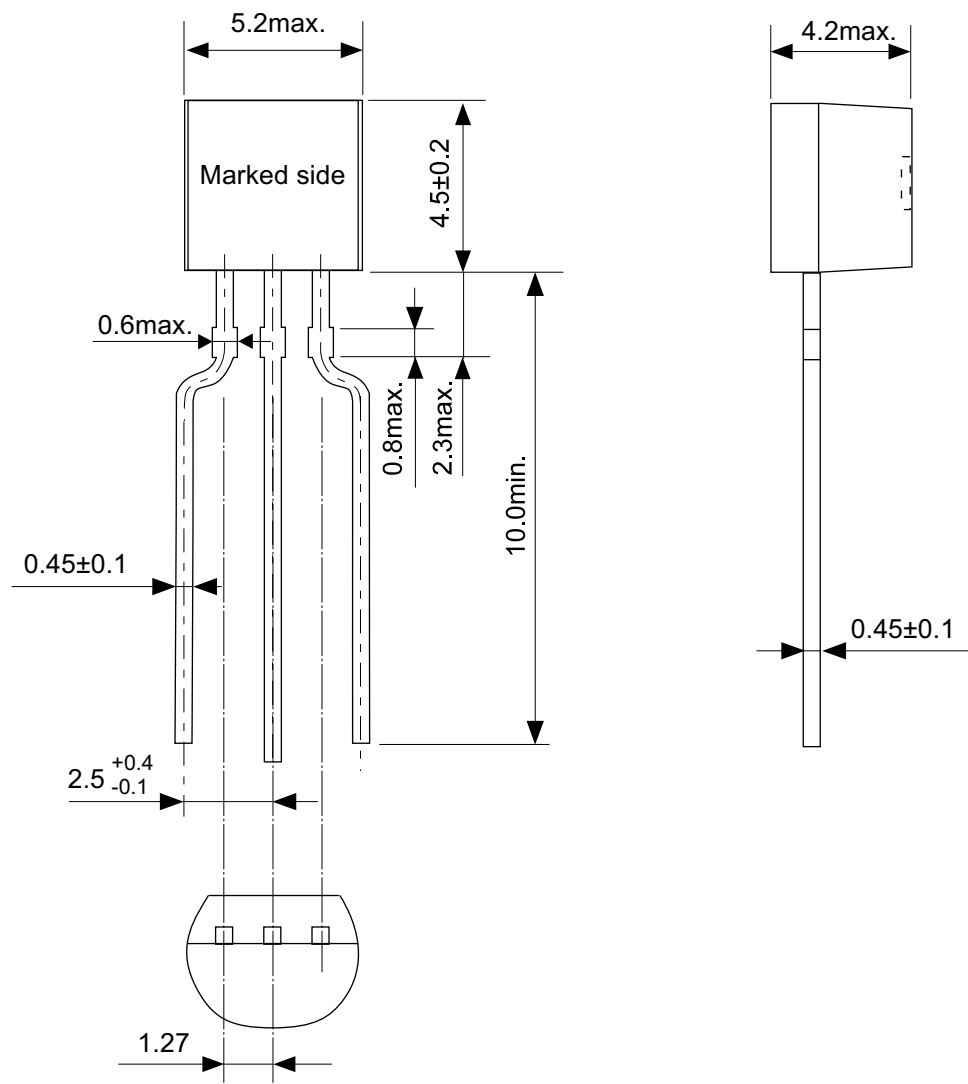
No. PF004-A-L-SD-4.1

TITLE	SNT-4A-A -Land Recommendation
No.	PF004-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	



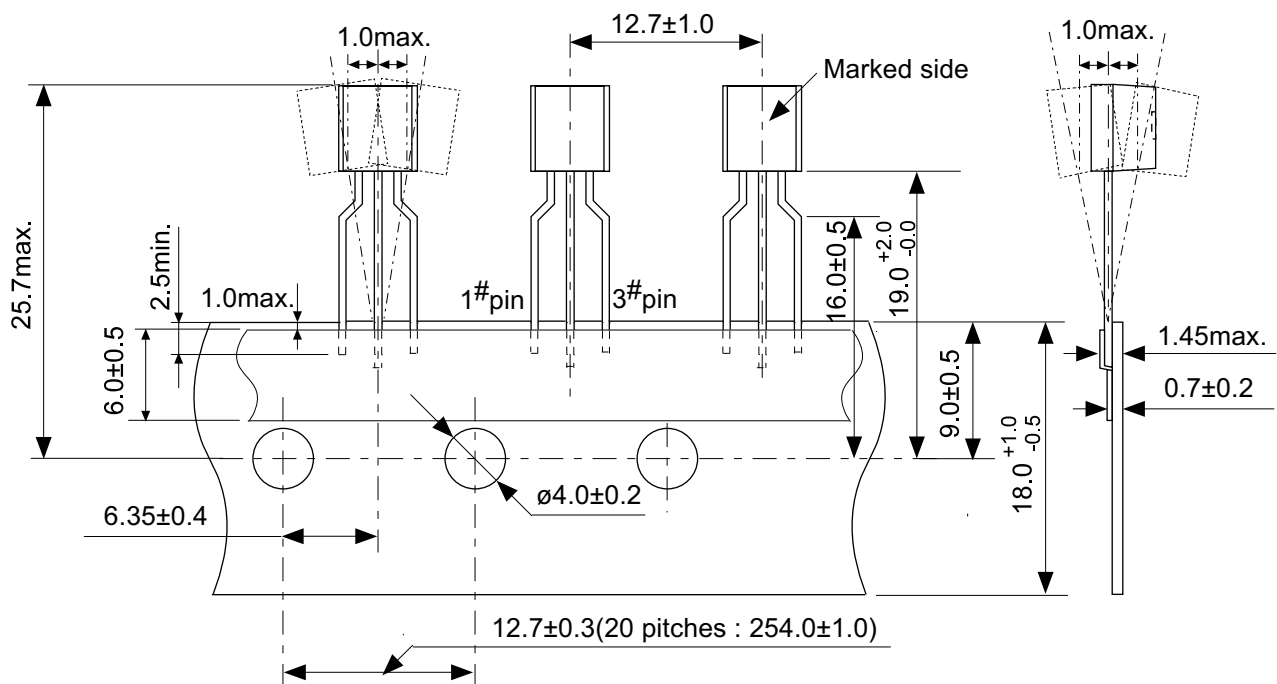
No. YS003-D-P-SD-2.1

TITLE	TO92-D-PKG Dimensions
No.	YS003-D-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

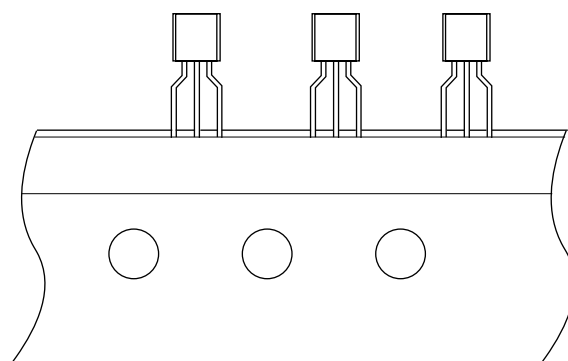


No. YZ003-E-P-SD-2.1

TITLE	TO92-E-PKG Dimensions
No.	YZ003-E-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



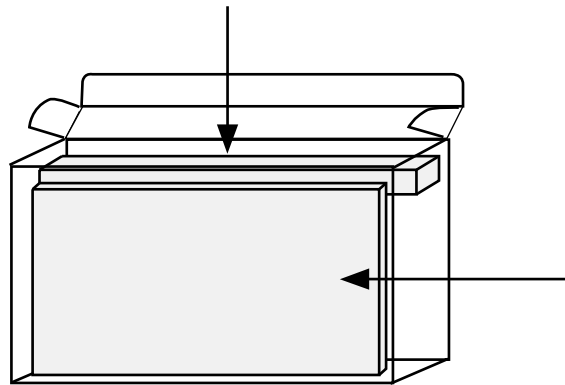
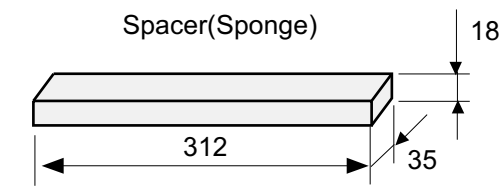
Z type



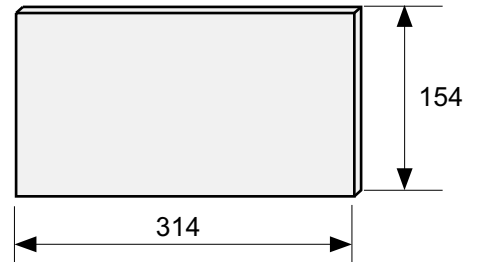
→
Feed direction

No. YZ003-E-C-SD-1.1

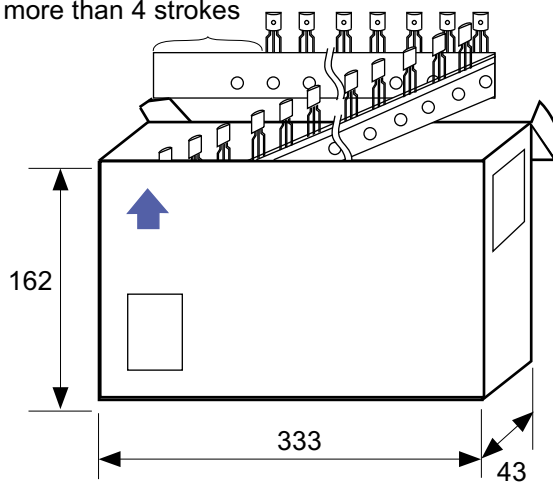
TITLE	TO92-E-Radial Tape
No.	YZ003-E-C-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Side spacer placed in front side



Space more than 4 strokes



No. YZ003-E-Z-SD-2.0

TITLE	TO92-E-Ammo Packing		
No.	YZ003-E-Z-SD-2.0		
ANGLE		QTY.	2,000
UNIT	mm		
ABLIC Inc.			

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The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
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