■ Block Diagram

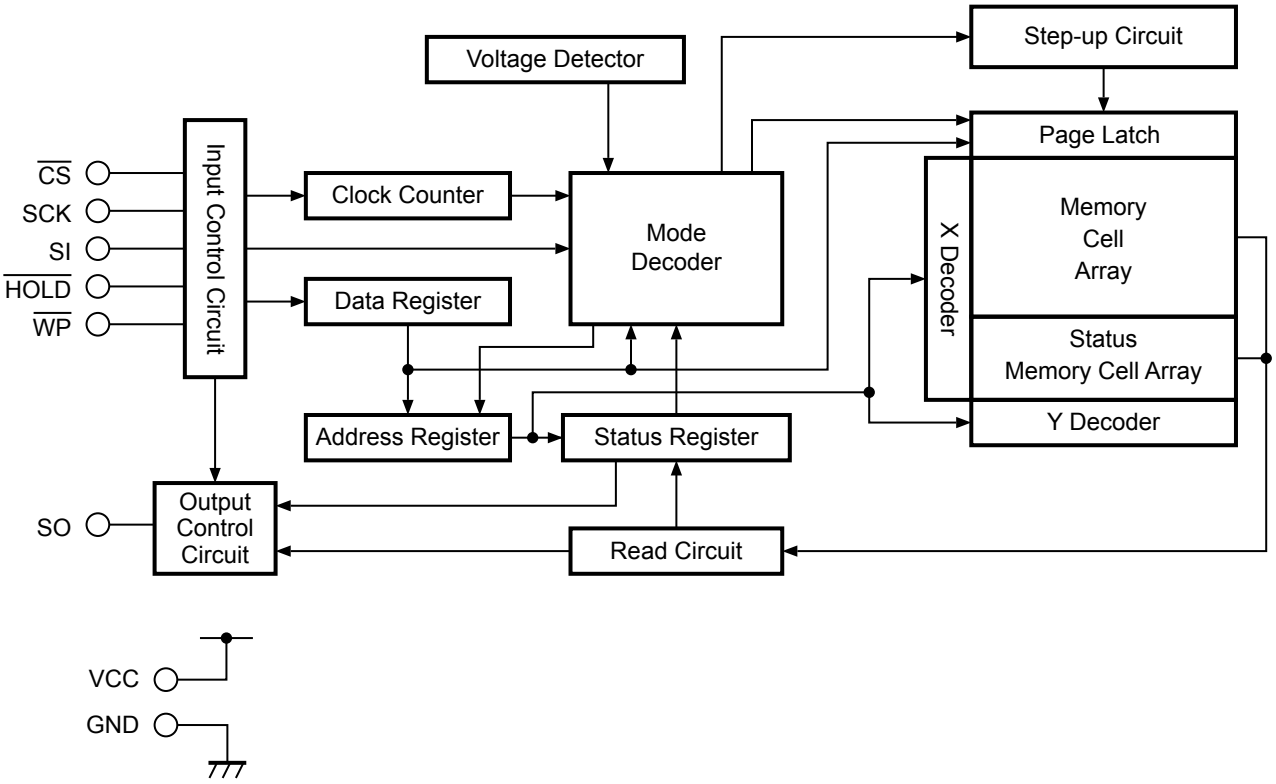


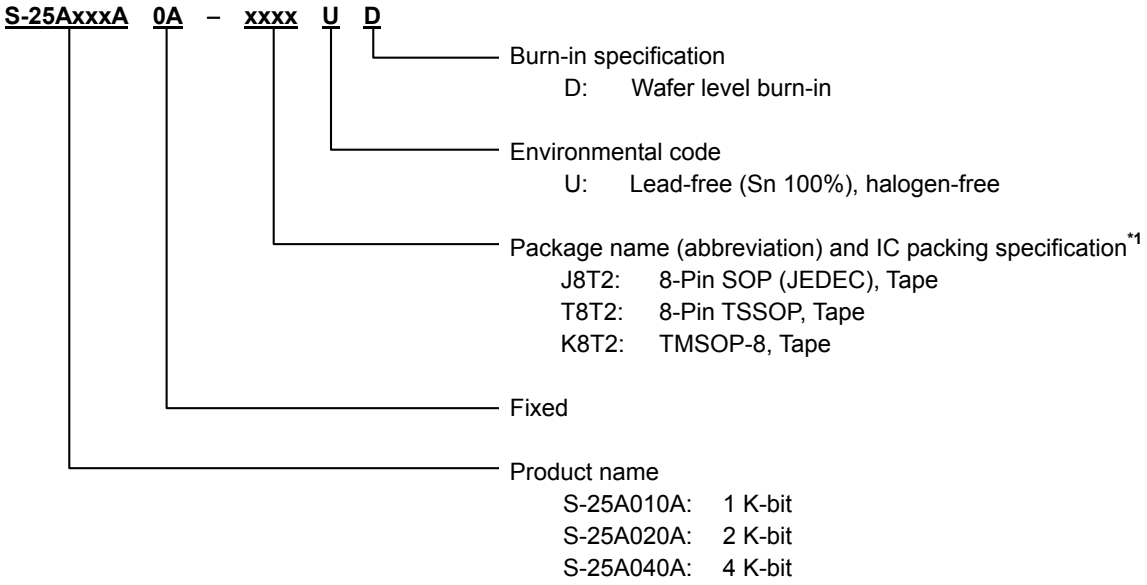
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-SD
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

3. Product name list

Table 2

Product Name	Capacity	Package	Quantity
S-25A010A0A-J8T2UD	1 K bit	8-Pin SOP (JEDEC)	2000 pcs / reel
S-25A010A0A-T8T2UD	1 K bit	8-Pin TSSOP	3000 pcs / reel
S-25A010A0A-K8T2UD	1 K bit	TMSOP-8	4000 pcs / reel
S-25A020A0A-J8T2UD	2 K bit	8-Pin SOP (JEDEC)	2000 pcs / reel
S-25A020A0A-T8T2UD	2 K bit	8-Pin TSSOP	3000 pcs / reel
S-25A020A0A-K8T2UD	2 K bit	TMSOP-8	4000 pcs / reel
S-25A040A0A-J8T2UD	4 K bit	8-Pin SOP (JEDEC)	2000 pcs / reel
S-25A040A0A-T8T2UD	4 K bit	8-Pin TSSOP	3000 pcs / reel
S-25A040A0A-K8T2UD	4 K bit	TMSOP-8	4000 pcs / reel

Remark **1.** Please contact our sales office for products with product name structure other than those specified above.
2. This IC is wafer level burn-in specification.

■ Pin Configurations

1. 8-Pin SOP (JEDEC)

Top view

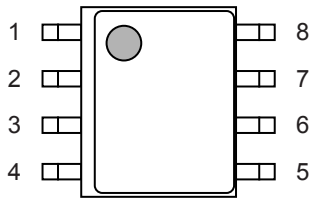


Figure 2

Table 3

Pin No.	Symbol	Description
1	$\overline{CS}$ *1	Chip select input
2	SO	Serial data output
3	$\overline{WP}$ *1	Write protect input
4	GND	Ground
5	SI*1	Serial data input
6	SCK*1	Serial clock input
7	$\overline{HOLD}$ *1	Hold input
8	VCC	Power supply

2. 8-Pin TSSOP

Top view

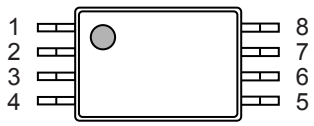


Figure 3

Table 4

Pin No.	Symbol	Description
1	$\overline{CS}$ *1	Chip select input
2	SO	Serial data output
3	$\overline{WP}$ *1	Write protect input
4	GND	Ground
5	SI*1	Serial data input
6	SCK*1	Serial clock input
7	$\overline{HOLD}$ *1	Hold input
8	VCC	Power supply

3. TMSOP-8

Top view

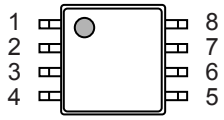


Figure 4

Table 5

Pin No.	Symbol	Description
1	$\overline{CS}$ *1	Chip select input
2	SO	Serial data output
3	$\overline{WP}$ *1	Write protect input
4	GND	Ground
5	SI*1	Serial data input
6	SCK*1	Serial clock input
7	$\overline{HOLD}$ *1	Hold input
8	VCC	Power supply

***1.** Do not use it in "High-Z".

■ Absolute Maximum Ratings

Table 6

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to +7.0	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 7

Item	Symbol	Condition	Ta = −40°C to +125°C		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	Read	2.5	5.5	V
		Write	2.5	5.5	V
High level input voltage	V_{IH}	V_{CC} = 2.5 V to 5.5 V	0.7 × V_{CC}	V_{CC} + 1.0	V
Low level input voltage	V_{IL}	V_{CC} = 2.5 V to 5.5 V	−0.3	0.3 × V_{CC}	V

■ Pin Capacitance

Table 8

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	−	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V (SO)	−	10	pF

■ Endurance

Table9

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	Ta = −40°C to +85°C	10^6	−	cycle / word*1
		Ta = −40°C to +105°C	8×10^5	−	cycle / word*1
		Ta = −40°C to +125°C	5×10^5	−	cycle / word*1

***1.** For each address (Word: 8-bit)

■ Data Retention

Table 10

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	Ta = +25°C	100	−	year
		Ta = −40°C to +125°C	50	−	year

■ DC Electrical Characteristics

Table 11

Item	Symbol	Condition	Ta = −40°C to +125°C						Unit
			V_{CC} = 2.5 V to 3.0 V f_{SCK} = 3.5 MHz		V_{CC} = 3.0 V to 4.5 V f_{SCK} = 5.0 MHz		V_{CC} = 4.5 V to 5.5 V f_{SCK} = 6.5 MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (read)	I_{CC1}	No load at SO pin	−	1.5	−	2.0	−	2.5	mA

Table 12

Item	Symbol	Condition	Ta = −40°C to +125°C						Unit
			V_{CC} = 2.5 V to 3.0 V f_{SCK} = 3.5 MHz		V_{CC} = 3.0 V to 4.5 V f_{SCK} = 5.0 MHz		V_{CC} = 4.5 V to 5.5 V f_{SCK} = 6.5 MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (write)	I_{CC2}	No load at SO pin	−	2.0	−	2.5	−	3.0	mA

Table 13

Item	Symbol	Condition	Ta = −40°C to +85°C				Ta = +85°C to +125°C				Unit
			V_{CC} = 2.5 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	$\overline{CS}$ = V_{CC}, SO = Open Other inputs are V_{CC} or GND	−	2.0	−	3.0	−	8.0	−	10.0	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−	1.0	−	1.0	−	2.0	−	2.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	−	1.0	−	1.0	−	2.0	−	2.0	μA
Low level output voltage	V_{OL1}	I_{OL} = 2.0 mA	−	−	−	0.4	−	−	−	0.4	V
	V_{OL2}	I_{OL} = 1.5 mA	−	0.4	−	0.4	−	0.4	−	0.4	V
High level output voltage	V_{OH1}	I_{OH} = −2.0 mA	−	−	0.8 × V_{CC}	−	−	−	0.8 × V_{CC}	−	V
	V_{OH2}	I_{OH} = −0.4 mA	0.8 × V_{CC}	−	0.8 × V_{CC}	−	0.8 × V_{CC}	−	0.8 × V_{CC}	−	V

■ AC Electrical Characteristics

Table 14 Measurement Conditions

Input pulse voltage	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100 pF

Table 15

Item	Symbol	Ta = −40°C to +125°C						Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 3.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	−	3.5	−	5.0	−	6.5	MHz
$\overline{CS}$ setup time during $\overline{CS}$ falling	$t_{CSS.CL}$	90	−	90	−	65	−	ns
$\overline{CS}$ setup time during $\overline{CS}$ rising	$t_{CSS.CH}$	90	−	90	−	65	−	ns
$\overline{CS}$ deselect time	t_{CDS}	160	−	140	−	110	−	ns
$\overline{CS}$ hold time during $\overline{CS}$ falling	$t_{CSH.CL}$	90	−	90	−	65	−	ns
$\overline{CS}$ hold time during $\overline{CS}$ rising	$t_{CSH.CH}$	90	−	90	−	65	−	ns
SCK clock time "H"*1	t_{HIGH}	125	−	95	−	65	−	ns
SCK clock time "L"*1	t_{LOW}	125	−	95	−	65	−	ns
Rising time of SCK clock*2	t_{RSK}	−	1	−	1	−	1	µs
Falling time of SCK clock*2	t_{FSK}	−	1	−	1	−	1	µs
SI data input setup time	t_{DS}	20	−	20	−	20	−	ns
SI data input hold time	t_{DH}	30	−	30	−	30	−	ns
SCK "L" hold time during $\overline{HOLD}$ rising	$t_{SKH.HH}$	70	−	70	−	45	−	ns
SCK "L" hold time during $\overline{HOLD}$ falling	$t_{SKH.HL}$	40	−	40	−	30	−	ns
SCK "L" setup time during $\overline{HOLD}$ falling	$t_{SKS.HL}$	0	−	0	−	0	−	ns
SCK "L" setup time during $\overline{HOLD}$ rising	$t_{SKS.HH}$	0	−	0	−	0	−	ns
Disable time of SO output*2	t_{OZ}	−	100	−	100	−	75	ns
Delay time of SO output	t_{OD}	−	120	−	90	−	60	ns
Hold time of SO output	t_{OH}	0	−	0	−	0	−	ns
Rising time of SO output*2	t_{RO}	−	80	−	80	−	50	ns
Falling time of SO output*2	t_{FO}	−	80	−	80	−	50	ns
Disable time of SO output during $\overline{HOLD}$ falling*2	$t_{OZ.HL}$	−	100	−	100	−	75	ns
Delay time of SO output during $\overline{HOLD}$ rising*2	$t_{OD.HH}$	−	80	−	80	−	60	ns
$\overline{WP}$ setup time	t_{WS1}	0	−	0	−	0	−	ns
$\overline{WP}$ hold time	t_{WH1}	0	−	0	−	0	−	ns
$\overline{WP}$ release / setup time	t_{WS2}	0	−	0	−	0	−	ns
$\overline{WP}$ release / hold time	t_{WH2}	150	−	150	−	100	−	ns

***1.** The clock cycle of the SCK clock (frequency f_{SCK}) is 1 / f_{SCK} µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as (1 / f_{SCK}) = t_{LOW} (min.) + t_{HIGH} (min.) by minimizing the SCK clock cycle time.

***2.** These are values of sample and not 100% tested.

Table 16

Item	Symbol	Ta = −40°C to +105°C						Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 3.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	−	3.5	−	5.0	−	6.5	MHz
$\overline{CS}$ setup time during $\overline{CS}$ falling	$t_{CSS.CL}$	90	−	90	−	65	−	ns
$\overline{CS}$ setup time during $\overline{CS}$ rising	$t_{CSS.CH}$	90	−	90	−	65	−	ns
$\overline{CS}$ deselect time	t_{CDS}	160	−	140	−	110	−	ns
$\overline{CS}$ hold time during $\overline{CS}$ falling	$t_{CSH.CL}$	90	−	90	−	65	−	ns
$\overline{CS}$ hold time during $\overline{CS}$ rising	$t_{CSH.CH}$	90	−	90	−	65	−	ns
SCK clock time "H"*1	t_{HIGH}	125	−	95	−	65	−	ns
SCK clock time "L"*1	t_{LOW}	125	−	95	−	65	−	ns
Rising time of SCK clock*2	t_{RSK}	−	1	−	1	−	1	µs
Falling time of SCK clock*2	t_{FSK}	−	1	−	1	−	1	µs
SI data input setup time	t_{DS}	20	−	20	−	20	−	ns
SI data input hold time	t_{DH}	30	−	30	−	30	−	ns
SCK "L" hold time during $\overline{HOLD}$ rising	$t_{SKH.HH}$	70	−	70	−	45	−	ns
SCK "L" hold time during $\overline{HOLD}$ falling	$t_{SKH.HL}$	40	−	40	−	30	−	ns
SCK "L" setup time during $\overline{HOLD}$ falling	$t_{SKS.HL}$	0	−	0	−	0	−	ns
SCK "L" setup time during $\overline{HOLD}$ rising	$t_{SKS.HH}$	0	−	0	−	0	−	ns
Disable time of SO output*2	t_{OZ}	−	100	−	100	−	75	ns
Delay time of SO output	t_{OD}	−	120	−	90	−	60	ns
Hold time of SO output	t_{OH}	0	−	0	−	0	−	ns
Rising time of SO output*2	t_{RO}	−	80	−	70	−	50	ns
Falling time of SO output*2	t_{FO}	−	80	−	70	−	50	ns
Disable time of SO output during $\overline{HOLD}$ falling*2	$t_{OZ.HL}$	−	100	−	100	−	75	ns
Delay time of SO output during $\overline{HOLD}$ rising*2	$t_{OD.HH}$	−	80	−	80	−	60	ns
$\overline{WP}$ setup time	t_{WS1}	0	−	0	−	0	−	ns
$\overline{WP}$ hold time	t_{WH1}	0	−	0	−	0	−	ns
$\overline{WP}$ release / setup time	t_{WS2}	0	−	0	−	0	−	ns
$\overline{WP}$ release / hold time	t_{WH2}	150	−	150	−	100	−	ns

***1.** The clock cycle of the SCK clock (frequency f_{SCK}) is 1 / f_{SCK} µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as (1 / f_{SCK}) = t_{LOW} (min.) + t_{HIGH} (min.) by minimizing the SCK clock cycle time.

***2.** These are values of sample and not 100% tested.

Table 17

Item	Symbol	Ta = −40°C to +85°C						Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 3.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	−	4.0	−	5.0	−	7.0	MHz
$\overline{CS}$ setup time during $\overline{CS}$ falling	$t_{CSS.CL}$	90	−	80	−	60	−	ns
$\overline{CS}$ setup time during $\overline{CS}$ rising	$t_{CSS.CH}$	90	−	80	−	60	−	ns
$\overline{CS}$ deselect time	t_{CDS}	150	−	120	−	100	−	ns
$\overline{CS}$ hold time during $\overline{CS}$ falling	$t_{CSH.CL}$	90	−	80	−	60	−	ns
$\overline{CS}$ hold time during $\overline{CS}$ rising	$t_{CSH.CH}$	90	−	80	−	60	−	ns
SCK clock time "H"*1	t_{HIGH}	115	−	90	−	60	−	ns
SCK clock time "L"*1	t_{LOW}	115	−	90	−	60	−	ns
Rising time of SCK clock*2	t_{RSK}	−	1	−	1	−	1	µs
Falling time of SCK clock*2	t_{FSK}	−	1	−	1	−	1	µs
SI data input setup time	t_{DS}	20	−	20	−	20	−	ns
SI data input hold time	t_{DH}	30	−	30	−	30	−	ns
SCK "L" hold time during $\overline{HOLD}$ rising	$t_{SKH.HH}$	70	−	60	−	40	−	ns
SCK "L" hold time during $\overline{HOLD}$ falling	$t_{SKH.HL}$	40	−	40	−	30	−	ns
SCK "L" setup time during $\overline{HOLD}$ falling	$t_{SKS.HL}$	0	−	0	−	0	−	ns
SCK "L" setup time during $\overline{HOLD}$ rising	$t_{SKS.HH}$	0	−	0	−	0	−	ns
Disable time of SO output*2	t_{OZ}	−	100	−	100	−	70	ns
Delay time of SO output	t_{OD}	−	110	−	85	−	55	ns
Hold time of SO output	t_{OH}	0	−	0	−	0	−	ns
Rising time of SO output*2	t_{RO}	−	80	−	50	−	40	ns
Falling time of SO output*2	t_{FO}	−	80	−	50	−	40	ns
Disable time of SO output during $\overline{HOLD}$ falling*2	$t_{OZ.HL}$	−	100	−	100	−	70	ns
Delay time of SO output during $\overline{HOLD}$ rising*2	$t_{OD.HH}$	−	80	−	75	−	55	ns
$\overline{WP}$ setup time	t_{WS1}	0	−	0	−	0	−	ns
$\overline{WP}$ hold time	t_{WH1}	0	−	0	−	0	−	ns
$\overline{WP}$ release / setup time	t_{WS2}	0	−	0	−	0	−	ns
$\overline{WP}$ release / hold time	t_{WH2}	150	−	150	−	100	−	ns

***1.** The clock cycle of the SCK clock (frequency f_{SCK}) is 1 / f_{SCK} µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as (1 / f_{SCK}) = t_{LOW} (min.) + t_{HIGH} (min.) by minimizing the SCK clock cycle time.

***2.** These are values of sample and not 100% tested.

Table 18

Item	Symbol	Ta = −40°C to +125°C V_{CC} = 2.5 V to 5.5 V		Unit
		Min.	Max.	
Write time	t_{PR}	—	4.0	ms

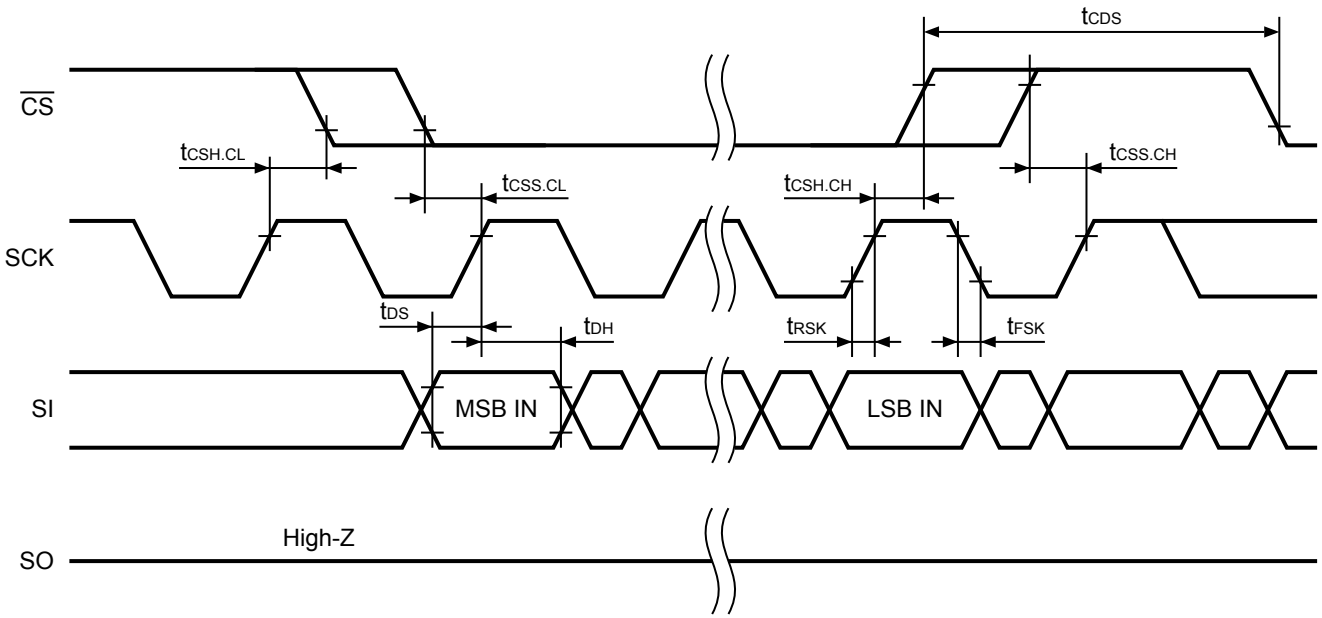


Figure 5 Serial Input Timing

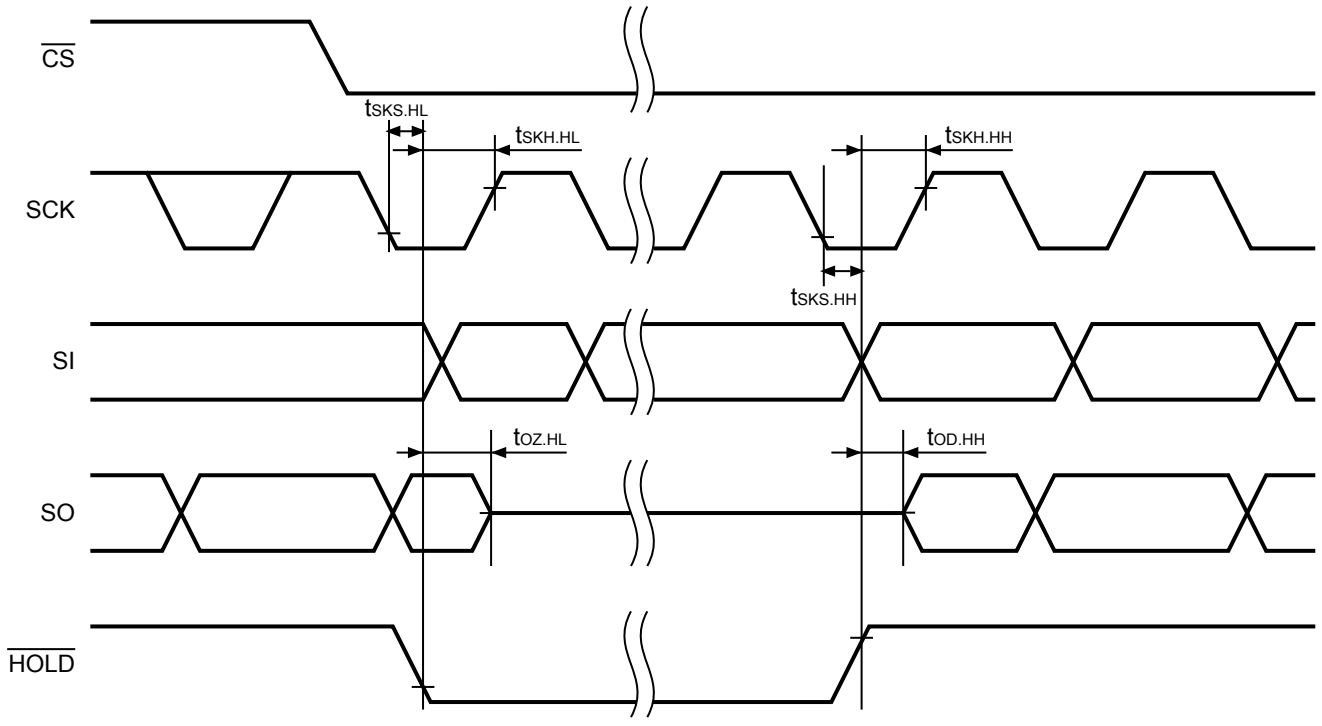


Figure 6 Hold Timing

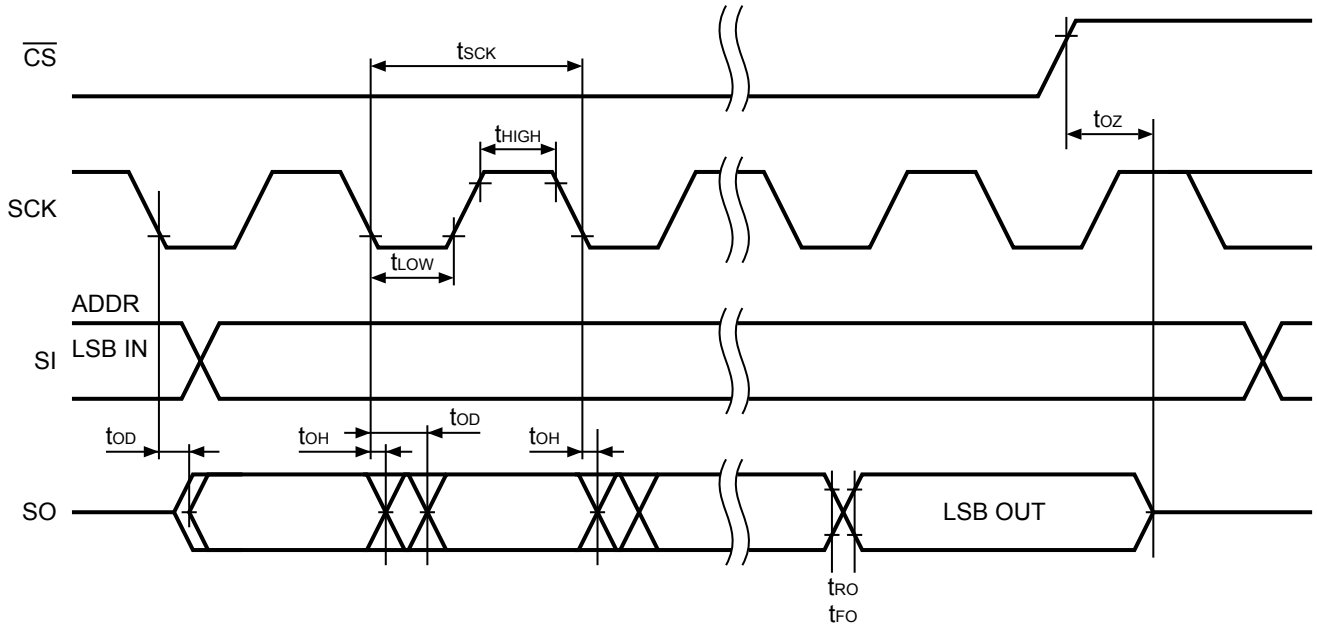


Figure 7 Serial Output Timing

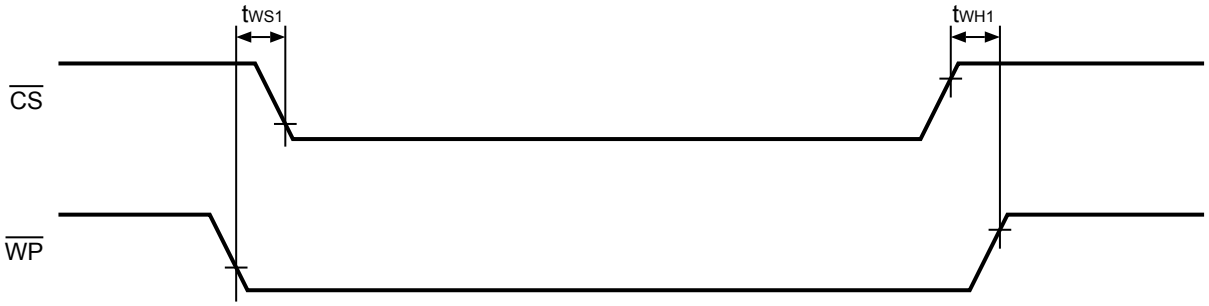


Figure 8 Valid Timing in Write Protect

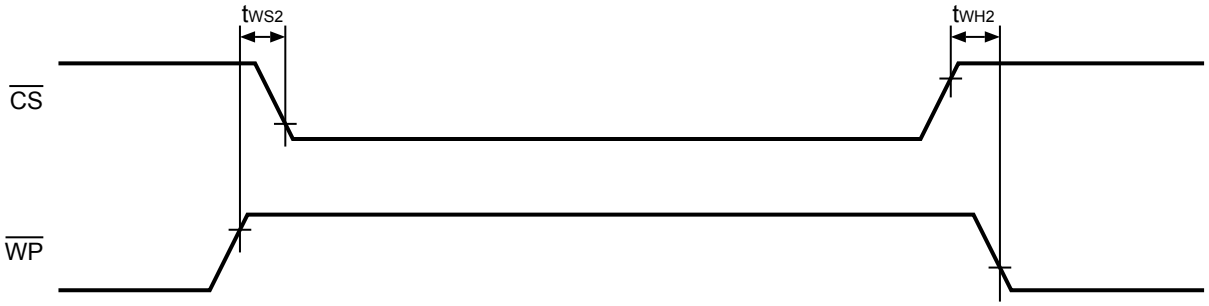


Figure 9 Invalid Timing in Write Protect

■ Pin Functions

1. $\overline{CS}$ (chip select input) pin

This is an input pin to set a chip in the select status. In the "H" input level, this IC is in the non-select status and its output is "High-Z". This IC is in standby as long as it is not in write inside. This IC goes in active by setting the chip select to "L". Input any instruction code after power-on and a falling of chip select.

2. SI (serial data input) pin

This pin is to input serial data. This pin receives an instruction code, an address and write data. This pin latches data at rising edge of serial clock.

3. SO (serial data output) pin

This pin is to output serial data. The data output changes at falling edge of serial clock.

4. SCK (serial clock input) pin

This is a clock input pin to set the timing of serial data. An instruction code, an address and write data are received at a rising edge of clock. Data is output during falling edge of clock.

5. $\overline{WP}$ (write protect input) pin

This is an input pin to protect memory data when write instruction (WRITE, WRSR) is being input. By setting this pin to "L", the WEL bit in the status register is set to "L". Therefore this IC does not write to the E^{2}PROM, however, it accepts other instructions. Fix this pin "H" or "L" not to set it in the floating state.
Refer to "■ **Protect Operation**" for details.

6. $\overline{HOLD}$ (hold input) pin

This pin is used to pause serial communications without setting this IC in the non-select status.
In the hold status, the serial output goes in "High-Z", the serial input and the serial clock go in "Don't care". During the hold operation, be sure to set this IC in active by setting the chip select ($\overline{CS}$ pin) to "L".
Refer to "■ **Hold Operation**" for details.

■ Initial Delivery State

Initial delivery state of all addresses is "FFh".
Moreover, initial delivery state of the status register nonvolatile memory is as follows.

- BP1 = 0
- BP0 = 0

■ Instruction Sets

Table 19 and **Table 20** are the list of instruction for this IC. The instruction is able to be input by changing the $\overline{CS}$ "H" to "L". Input the instruction in the MSB first. Each instruction code is organized with 1-byte as shown below. If this IC receives any invalid instruction code, this IC goes in the non-select status.

1. S-25A010A/020A

Table 19 Instruction Set

Instruction	Operation	Instruction Code	Address	Data
		SCK Input Clock 1 to 8	SCK Input Clock 9 to 16	SCK Input Clock 17 to 24
WREN	Write enable	0000 X110	—	—
WRDI	Write disable	0000 X100	—	—
RDSR	Read the status register	0000 X101	b7 to b0 output*1	—
WRSR	Write in the status register	0000 X001	b7 to b0 input	—
READ	Read memory data	0000 X011	A7*2 to A0	D7 to D0 output*3
WRITE	Write memory data	0000 X010	A7*2 to A0	D7 to D0 input

***1.** Sequential data reading is possible.
***2.** In the S-25A010A, A7 = Don't care because the address range is A6 to A0.
***3.** After outputting data in the specified address, data in the following address is output.

Remark X = Don't care.

2. S-25A040A

Table 20 Instruction Set

Instruction	Operation	Instruction Code	Address	Data
		SCK Input Clock 1 to 8	SCK Input Clock 9 to 16	SCK Input Clock 17 to 24
WREN	Write enable	0000 X110	—	—
WRDI	Write disable	0000 X100	—	—
RDSR	Read the status register	0000 X101	b7 to b0 output*1	—
WRSR	Write in the status register	0000 X001	b7 to b0 input	—
READ	Read memory data	0000 [A8*2]011	A7 to A0	D7 to D0 output*3
WRITE	Write memory data	0000 [A8*2]010	A7 to A0	D7 to D0 input

***1.** Sequential data reading is possible.
***2.** In the S-25A040A, assign bit A8 in the address into the fifth bit in an instruction code.
***3.** After outputting data in the specified address, data in the following address is output.

Remark X = Don't care.

■ Operation

1. Status register

The status register's organization is below. The status register can write and read by a specific instruction.

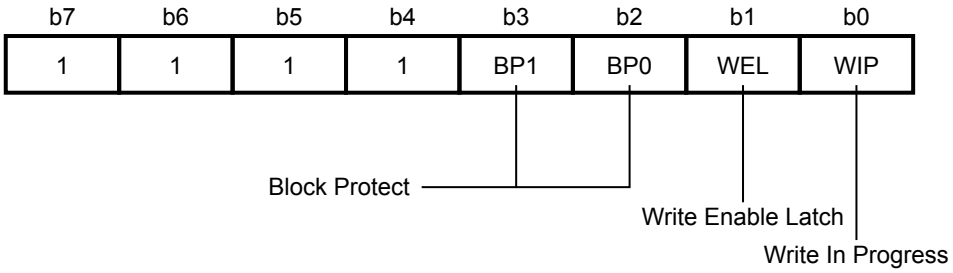


Figure 10 Organization of Status Register

The status / control bits of the status register are as follows.

1. 1 BP1, BP0 (b3, b2) : Block Protect

Bit BP1 and BP0 are composed of the nonvolatile memory. The area size of Software Protect with respect to WRITE instructions is defined by the BP1 and BP0 bits. Rewriting these bits is possible by the WRSR instruction. To protect the memory area against the WRITE instruction, set either or both of bit BP1 and BP0 to "1". Rewriting bit BP1 and BP0 is possible unless they are in Hardware Protect mode. Refer to "**■ Protect Operation**" for details of Block Protect.

1. 2 WEL (b1) : Write Enable Latch

Bit WEL shows the status of internal Write Enable Latch. Bit WEL is set by the WREN instruction only. If bit WEL is "1", this is the status that Write Enable Latch is set. If bit WEL is "0", Write Enable Latch is in reset, so that this IC does not receive the WRITE or WRSR instruction. Bit WEL is reset after these operations;

- The power supply voltage is dropping
- At power-on
- After performing WRDI
- After the completion of write operation by the WRSR instruction
- After the completion of write operation by the WRITE instruction
- After setting $\overline{WP}$ pin to "L"

1. 3 WIP (b0) : Write In Progress

Bit WIP is a read only bit. It indicates whether the internal memory is in the write operation or not by the WRITE or WRSR instruction. Bit WIP is "1" during the write operation but "0" during any other status. **Figure 11** shows the usage example.

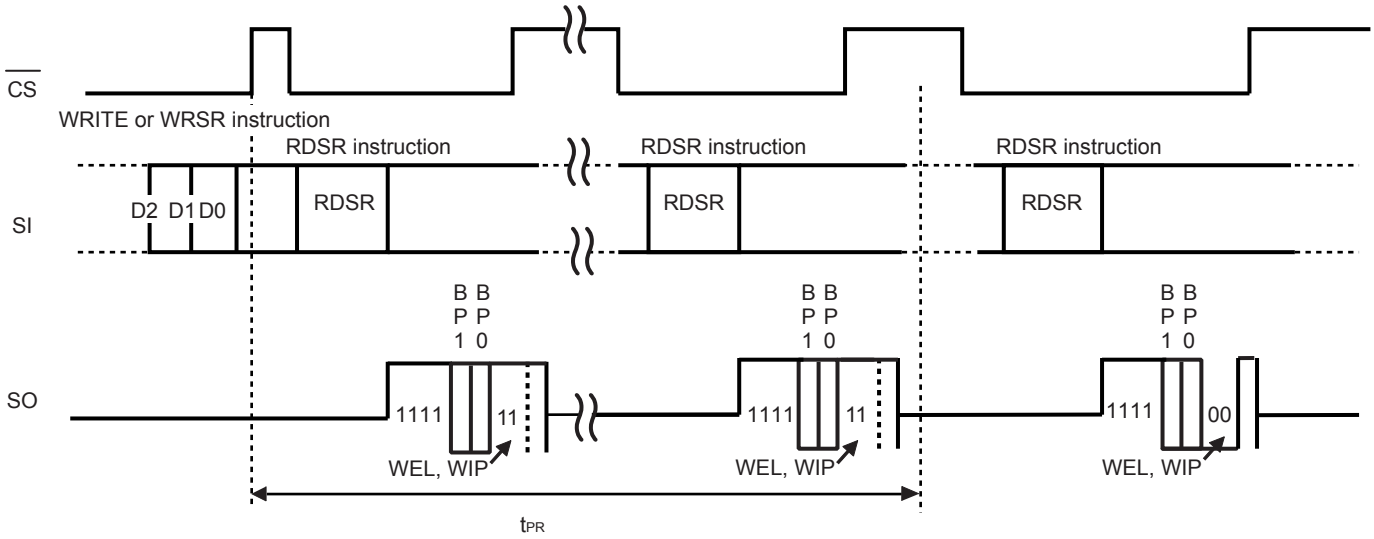
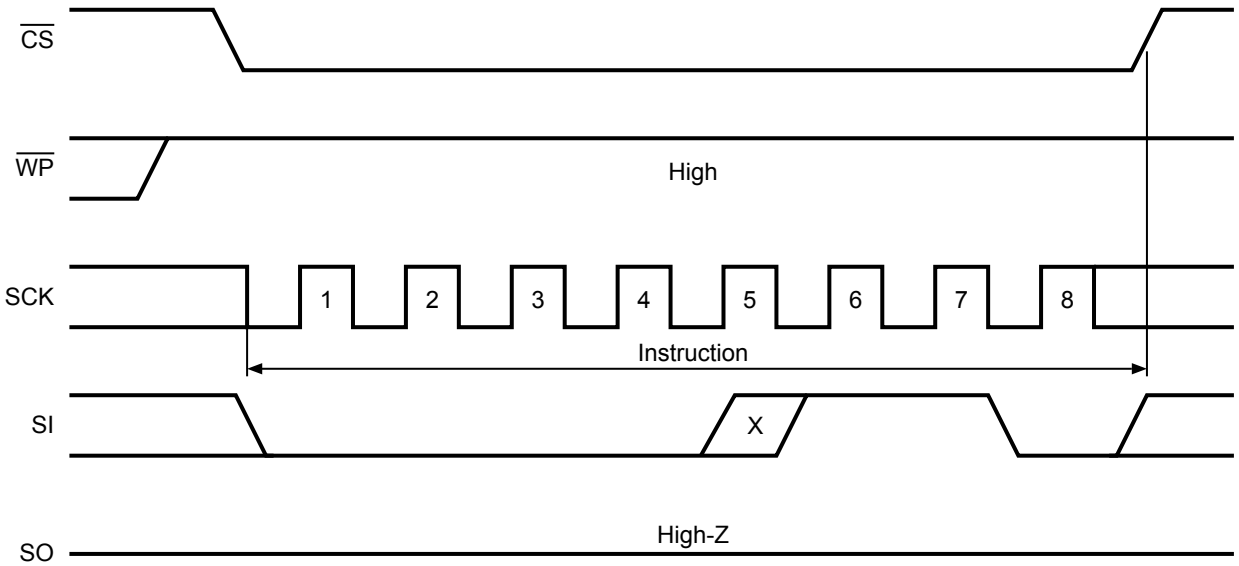


Figure 11 Usage Example of WEL, WIP Bits during Write

2. Write enable (WREN)

Before writing data (WRITE and WRSR), be sure to set bit Write Enable Latch (WEL). This instruction is to set bit WEL. Its operation is below.

After selecting this IC by the chip select ($\overline{CS}$), input the instruction code from serial data input (SI). To set bit WEL, set this IC in the non-select status by $\overline{CS}$ at the 8th clock of the serial clock (SCK). To cancel the WREN instruction, input the clock different from a specified value (n = 8 clock) while $\overline{CS}$ is in "L".



Remark X = Don't care.

Figure 12 WREN Operation

3. Write disable (WRDI)

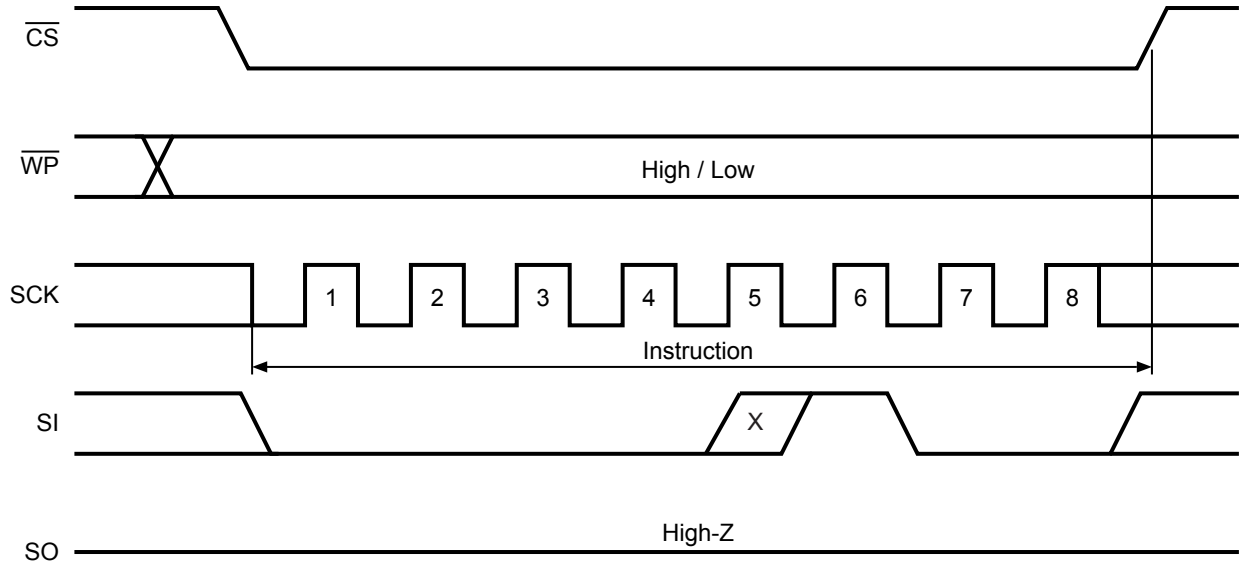
The WRDI instruction is one of ways to reset bit Write Enable Latch (WEL). After selecting this IC by the chip select ($\overline{CS}$), input the instruction code from serial data input (SI).

To reset bit WEL, set this IC in the non-select status by $\overline{CS}$ at the 8th clock of the serial clock.

To cancel the WRDI instruction, input the clock different from a specified value (n = 8 clock) while $\overline{CS}$ is in "L".

Bit WEL is reset after the operations shown below.

- The power supply voltage is dropping
- At power-on
- After performing WRDI
- After the completion of write operation by the WRSR instruction
- After the completion of write operation by the WRITE instruction
- After setting $\overline{WP}$ pin to "L"



Remark X = Don't care.

Figure 13 WRDI Operation

4. Read the status register (RDSR)

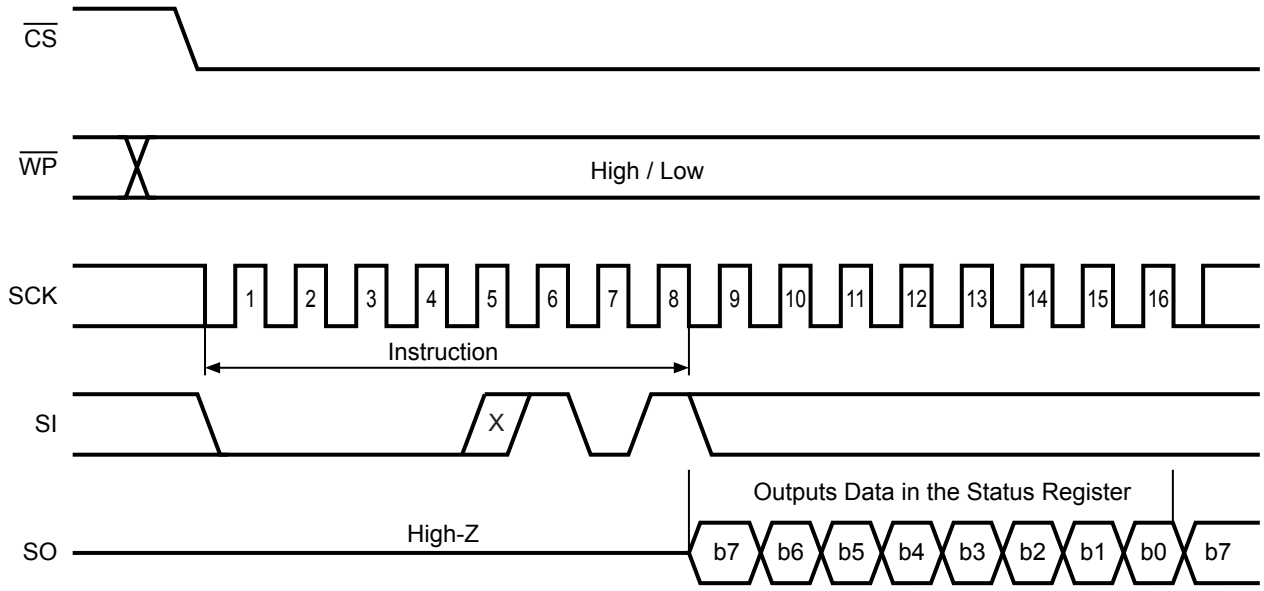
Reading data in the status register is possible by the RDSR instruction. During the write operation, it is possible to confirm the progress by checking bit WIP.

Set the chip select ($\overline{CS}$) "L" first. After that, input the instruction code from serial data input (SI). The status of bit in the status register is output from serial data output (SO). Sequential read is available for the status register. To stop the read cycle, set $\overline{CS}$ to "H".

It is possible to read the status register always. The bits in it are valid and can be read by RDSR even in the write cycle.

The 2 bits WEL and WIP are updated during the write cycle. The updated nonvolatile bits BP1 and BP0 can be acquired by performing a new RDSR instruction after verifying the completion of the write cycle.

b7, b6, b5, and b4 are "1" when they are read by the RDSR instruction.



Remark X = Don't care.

Figure 14 RDSR Operation

5. Write in the status register (WRSR)

The values of status register (BP1, BP0) can be rewritten by inputting the WRSR instruction. But b7, b6, b5, b4, b1, b0 of status register cannot be rewritten. b7 to b4 are always "1" when reading the status register.

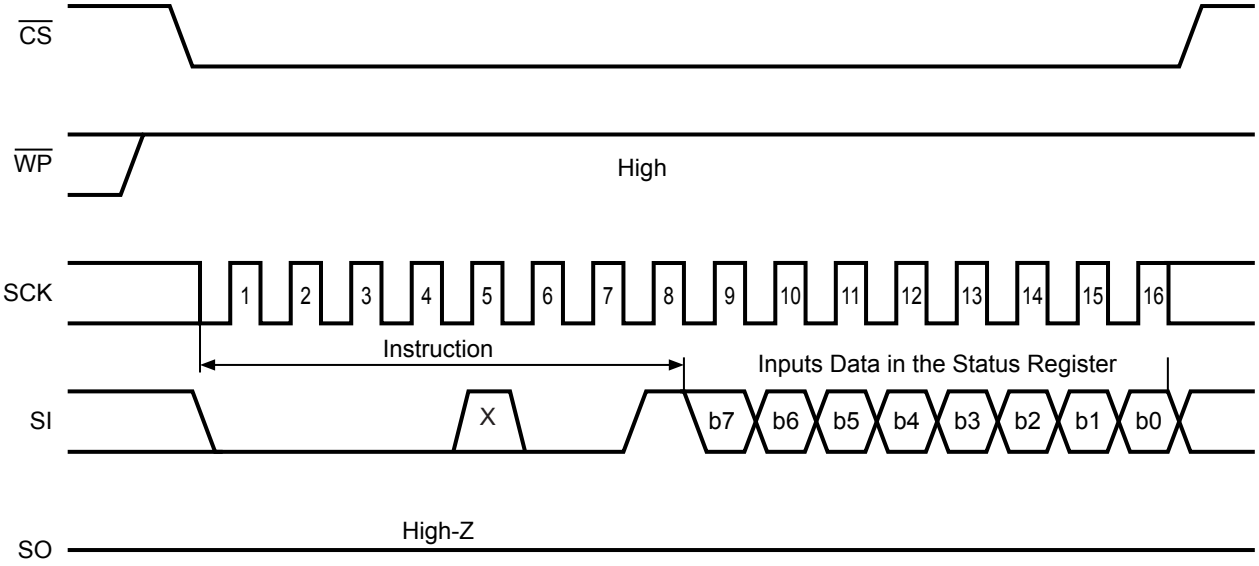
Before inputting the WRSR instruction, set bit WEL by the WREN instruction. The operation of WRSR is shown below.

Set the chip select ($\overline{CS}$) "L" first. After that, input the instruction code and data from serial data input (SI). To start WRSR write (t_{PR}), set the chip select ($\overline{CS}$) to "H" after inputting data or before inputting a rising of the next serial clock. It is possible to confirm the operation status by reading the value of bit WIP during WRSR write. Bit WIP is "1" during write, "0" during any other status. Bit WEL is reset when write is completed.

With the WRSR instruction, the values of BP1 and BP0; which determine the area size the users can handle as the read only memory; can be changed. When $\overline{WP}$ pin is "L", however, the WRSR instruction is not be performed (Refer to "■ **Protect Operation**").

Bits BP1 and BP0 keep the value which is the one prior to the WRSR instruction during the WRSR instruction. The newly updated value is changed when the WRSR instruction has completed.

To cancel the WRSR instruction, input the clock different from a specified value (n = 16 clock) while $\overline{CS}$ is in "L".



Remark X = Don't care.

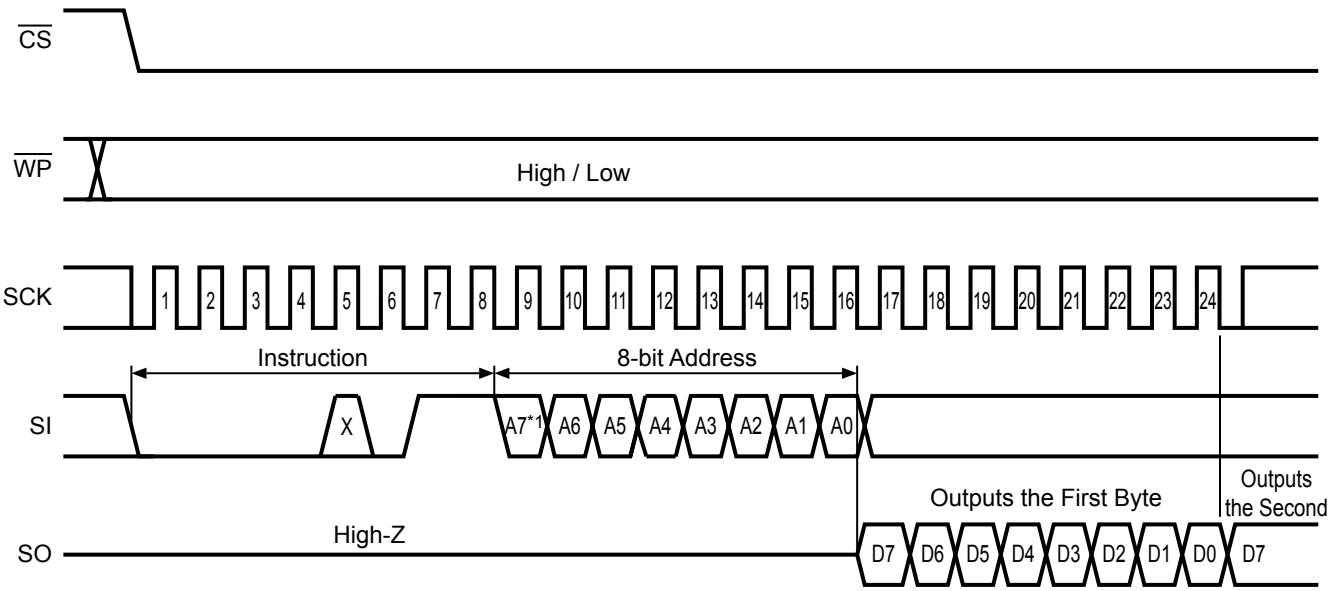
Figure 15 WRSR Operation

6. Read memory data (READ)

The READ operation is shown below. Input the instruction code and the address from serial data input (SI) after inputting "L" to the chip select ($\overline{CS}$). The input address is loaded to the internal address counter, and data in the address is output from the serial data output (SO).

Next, by inputting the serial clock (SCK) keeping the chip select ($\overline{CS}$) in "L", the address is automatically incremented so that data in the following address is sequentially output. The address counter rolls over to the first address by increment in the last address.

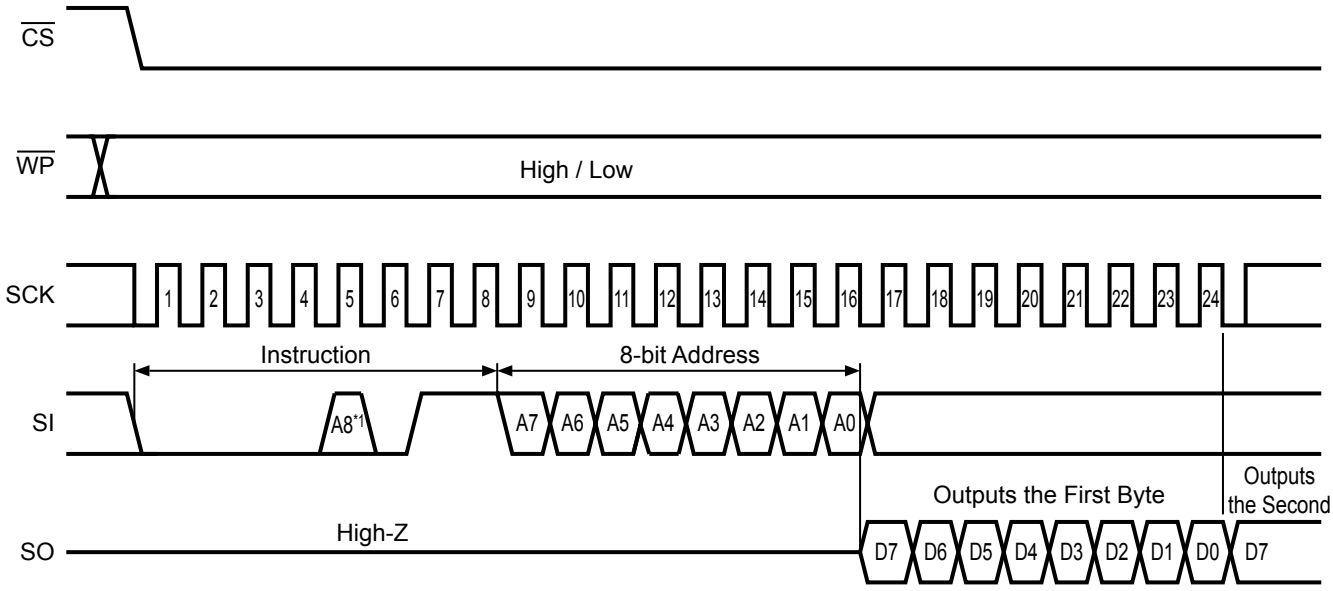
To finish the read cycle, set $\overline{CS}$ to "H". It is possible to raise the chip select always during the cycle. During write, the READ instruction code is not be accepted or operated.



***1** In the S-25A010A, A7 = Don't care because the address range is A6 to A0.

Remark X = Don't care.

Figure 16 READ Operation (S-25A010A/020A)



***1** In the S-25A040A, assign bit A8 in the address into the fifth bit in an instruction code.

Figure 17 READ Operation (S-25A040A)

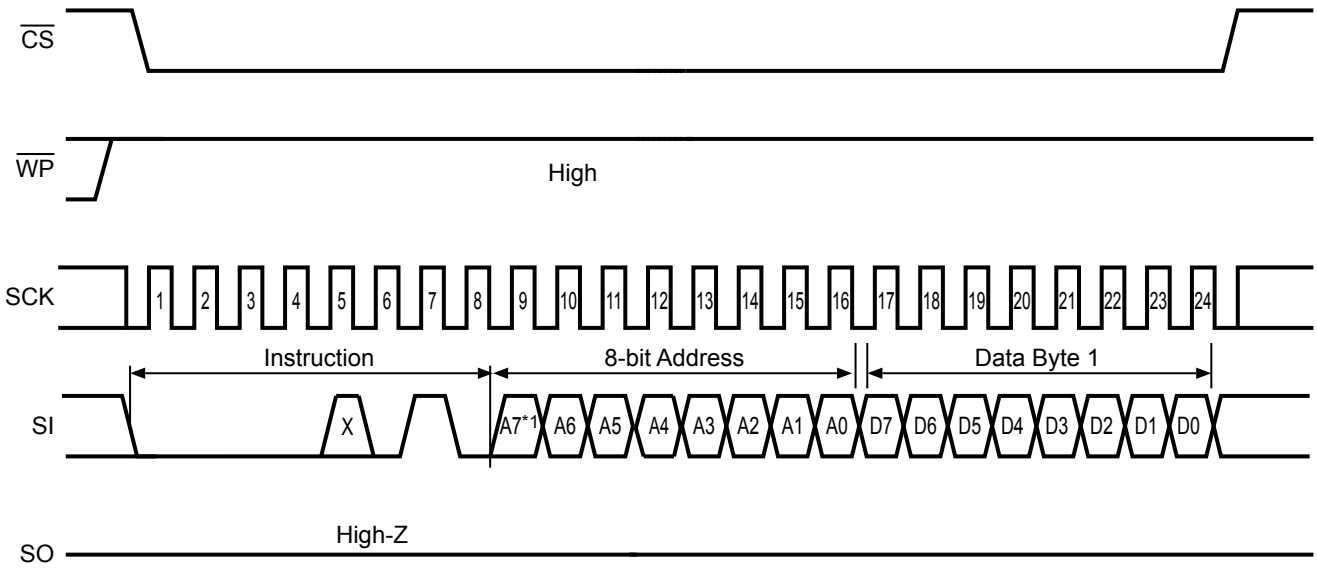
7. Write memory data (WRITE)

Figure 18 and **Figure 19** show the timing chart when inputting 1-byte data. Input the instruction code, the address and data from serial data input (SI) after inputting "L" to the chip select ($\overline{CS}$). To start WRITE (t_{PR}), set the chip select ($\overline{CS}$) to "H" after inputting data or before inputting a rising of the next serial clock. Bit WIP and WEL are reset to "0" when write has completed.
This IC can Page write of 16 bytes. Its function to transmit data is as same as Byte write basically, but it operates Page write by receiving sequential 8-bit write data as much data as page size has. Input the instruction code, the address and data from serial data input (SI) after inputting “L” in $\overline{CS}$, as the WRITE operation (page) shown in **Figure 20** and **Figure 21**. Input the next data while keeping $\overline{CS}$ in “L”. After that, repeat inputting data of 8-bit sequentially. At the end, by setting $\overline{CS}$ to “H”, the WRITE operation starts (t_{PR}).
4 of the lower bits in the address are automatically incremented every time when receiving write data of 8-bit. Thus, even if write data exceeds 16 bytes, the higher bits in the address do not change. And 4 of lower bits in the address roll over so that write data which is previously input is overwritten.

These are cases when the WRITE instruction is not accepted or operated.

- Bit WEL is not set to "1" (not set to "1" beforehand immediately before the WRITE instruction)
- During WRITE operation
- The address to be written is in the protect area by BP1 and BP0
- $\overline{WP}$ pin is set to "L"

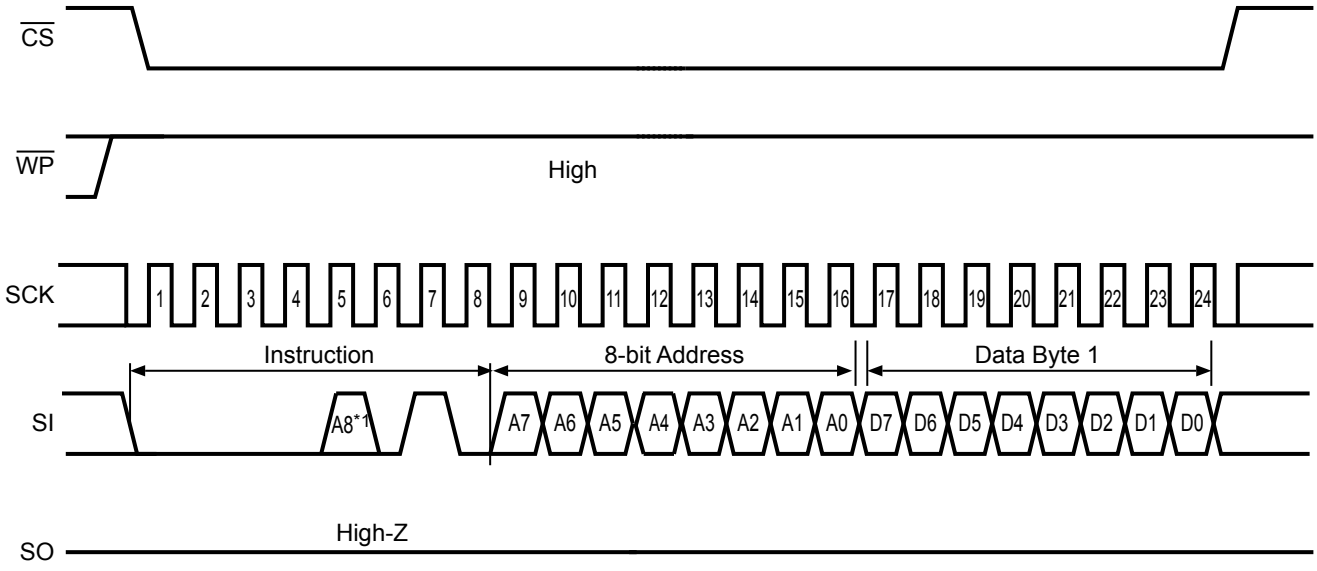
To cancel the WRITE instruction, input the clock different from a specified value (n = 16 + m × 8 clock) while $\overline{CS}$ is in "L".



***1** In the S-25A010A, A7 = Don't care because the address range is A6 to A0.

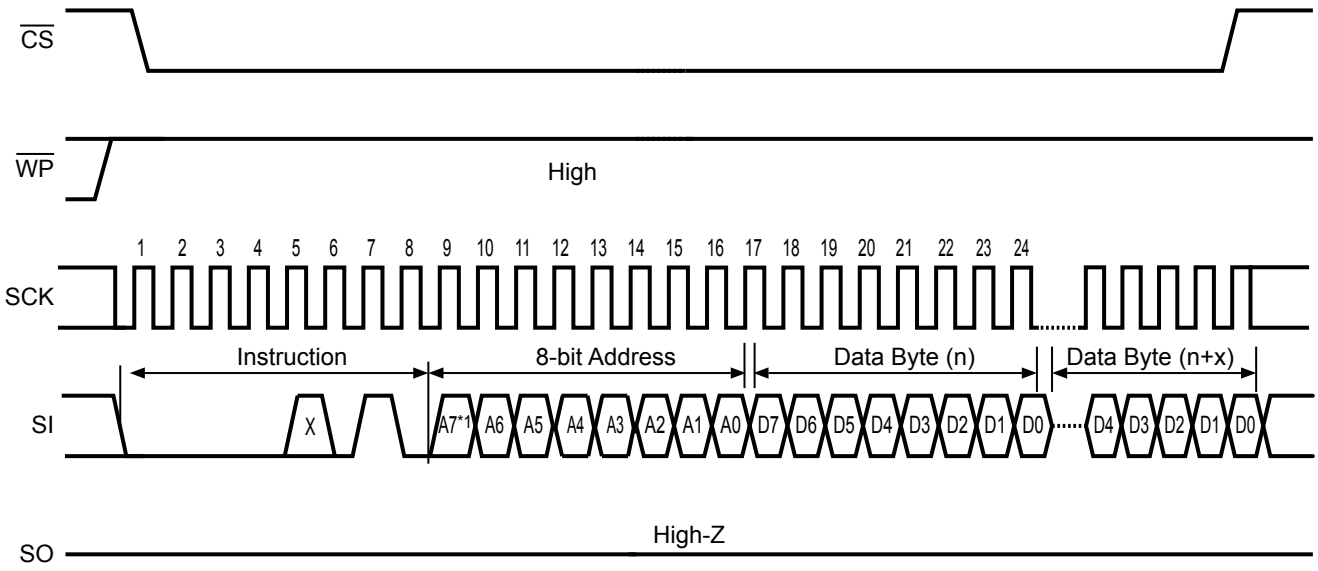
Remark X = Don't care.

Figure 18 WRITE Operation (1 Byte) (S-25A010A/020A)



***1** In the S-25A040A, assign bit A8 in the address into the fifth bit in an instruction code.

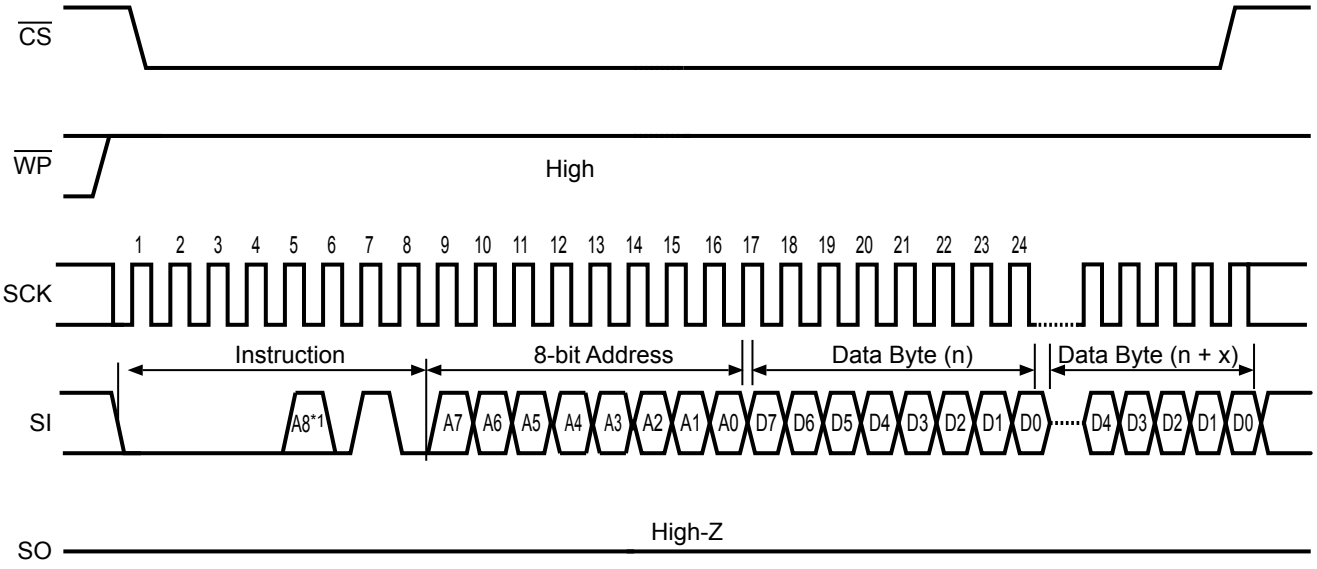
Figure 19 WRITE Operation (1 Byte) (S-25A040A)



***1** In the S-25A010A, A7 = Don't care because the address range is A6 to A0.

Remark X = Don't care.

Figure 20 WRITE Operation (Page) (S-25A010A/020A)



***1** In the S-25A040A, assign bit A8 in the address into the fifth bit in an instruction code.

Figure 21 WRITE Operation (Page) (S-25A040A)

■ Protect Operation

Table 21 shows the block settings of write protect. Setting value in Protect Bits (BP1, BP0) in the status register protect data in the area of all / 50% / 25% of the memory address.

Setting $\overline{WP}$ pin to “L” provides the following settings.

- Write protect for the WRITE, WRSR instructions
- Reset bit WEL

The timing during the cycle write to the status register is showed in "**Figure 8 Valid Timing in Write Protect**" and "**Figure 9 Invalid Timing in Write Protect**".

Table 21 Block Settings of Write Protect

Status Register		Area of Write Protect	Address of Write Protect Block		
BP1	BP0		S-25A010A	S-25A020A	S-25A040A
0	0	0%	None	None	None
0	1	25%	60h to 7Fh	C0h to FFh	180h to 1FFh
1	0	50%	40h to 7Fh	80h to FFh	100h to 1FFh
1	1	100%	00h to 7Fh	00h to FFh	000h to 1FFh

■ Hold Operation

The hold operation is used to pause serial communications without setting this IC in the non-select status. In the hold status, the serial data output goes in "High-Z", and both of the serial data input and the serial clock go in "Don't care". Be sure to set the chip select ($\overline{CS}$) to "L" to set this IC in the select status during the hold status.
Generally, during the hold status, this IC holds the select status. But if setting this IC in the non-select status, the users can finish the operation even in progress. **Figure 22** shows the hold operation.

These are two statuses when the serial clock (SCK) is set to "L".

- If setting hold ($\overline{HOLD}$) to "L", hold ($\overline{HOLD}$) is switched at the same time the hold status starts.
- If setting hold ($\overline{HOLD}$) to "H", hold ($\overline{HOLD}$) is switched at the same time the hold status ends.

These are two statuses when the serial clock (SCK) is set to "H".

- If setting hold ($\overline{HOLD}$) to "L", the hold status starts when the serial clock goes in "L" after hold ($\overline{HOLD}$) is switched.
- If setting hold ($\overline{HOLD}$) to "H", the hold status ends when the serial clock goes in "L" after hold ($\overline{HOLD}$) is switched.

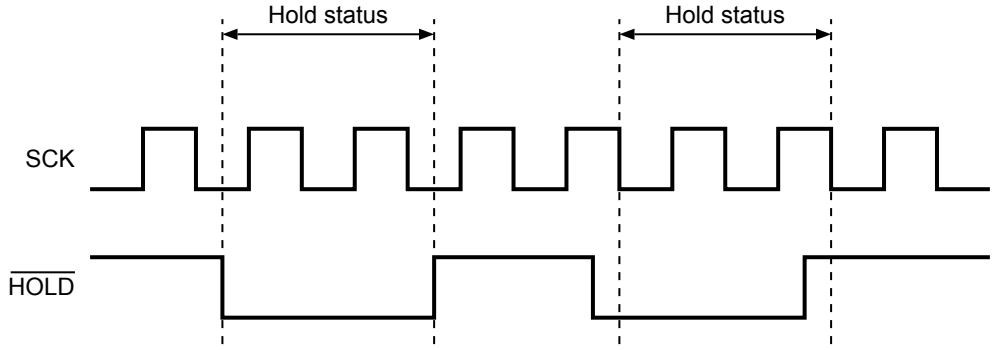


Figure 22 Hold Operation

■ Write Protect Function during the Low Power Supply Voltage

This IC has a built-in detection circuit which operates with the low power supply voltage. This IC cancels the write operation (WRITE, WRSR) when the power supply voltage drops and power-on, at the same time, goes in the write protect status (WRDI) automatically to reset bit WEL. The detection voltage is 1.20 V typ., the release voltage is 1.35 V typ., and its hysteresis is approx. 0.15 V (Refer to **Figure 23**).
To operate write, after the power supply voltage dropped once but rose to the voltage level which allows write again, be sure to set the Write Enable Latch bit (WEL) before operating write (WRITE, WRSR).
In the write operation, data in the address written during the low power supply voltage is not assured.

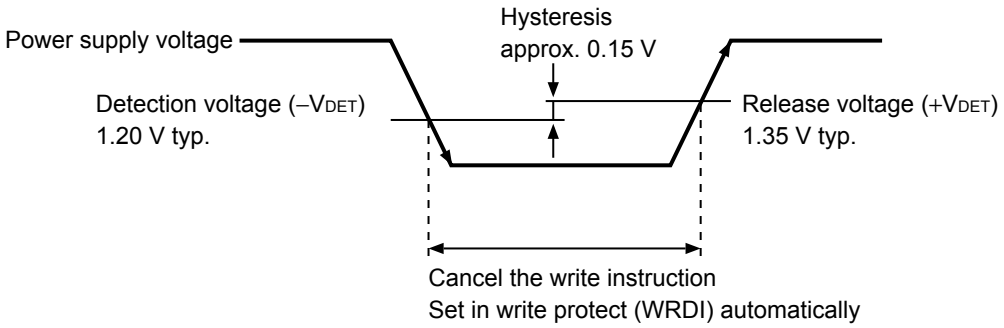


Figure 23 Operation during the Low Power Supply Voltage

■ Input Pin and Output Pin

1. Connection of input pin

All input pins in this IC have the CMOS structure. Do not set these pins in "High-Z" during operation when you design. Especially, set the $\overline{CS}$ input pin in the non-select status "H" during power-on/off and standby. The error write does not occur as long as the $\overline{CS}$ pin is in the non-select status "H". Set the $\overline{CS}$ pin to V_{CC} via a resistor (the pull-up resistor of 10 kΩ to 100 kΩ).
If the $\overline{CS}$ pin and the SCK pin change from "L" to "H" simultaneously, data may be input from the SI pin.
To prevent the error for sure, it is recommended to pull down the SCK pin to GND. In addition, it is recommended to pull up the SI pin, the $\overline{WP}$ pin and the $\overline{HOLD}$ pin to V_{CC}, or pull down these pins to GND, respectively. Connecting the $\overline{WP}$ pin and the $\overline{HOLD}$ pin to V_{CC} directly is also possible when these pins are not in use.

2. Equivalent circuit of input pin and output pin

Figure 24 and **Figure 25** show the equivalent circuits of input pins in this IC. A pull-up and pull-down elements are not included in each input pin, pay attention not to set it in the floating state when you design.
Figure 26 shows the equivalent circuit of the output pin. This pin has the tri-state output of "H" / "L" / "High-Z".

2. 1 Input pin

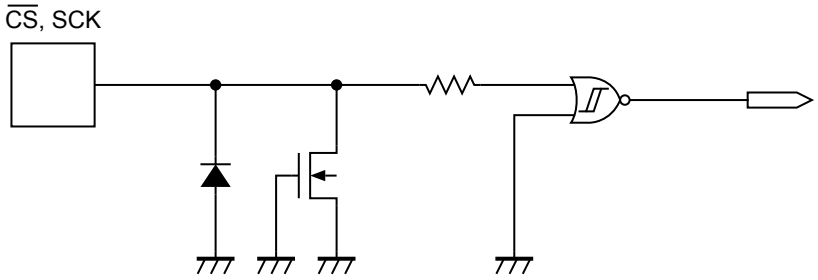


Figure 24 $\overline{CS}$, SCK Pin

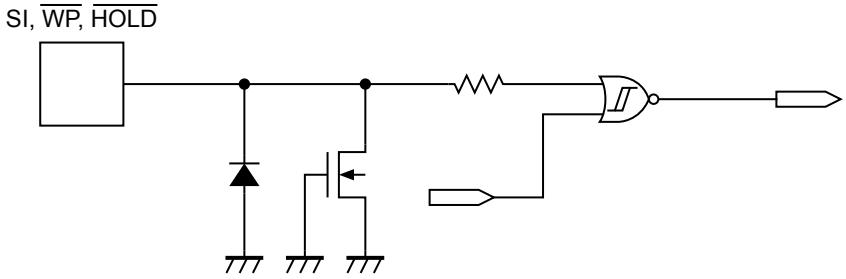


Figure 25 SI, $\overline{WP}$, $\overline{HOLD}$ Pin

2. 2 Output pin

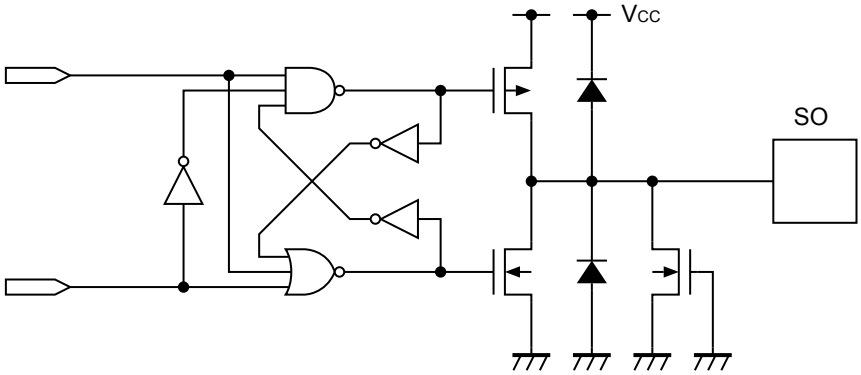


Figure 26 SO Pin

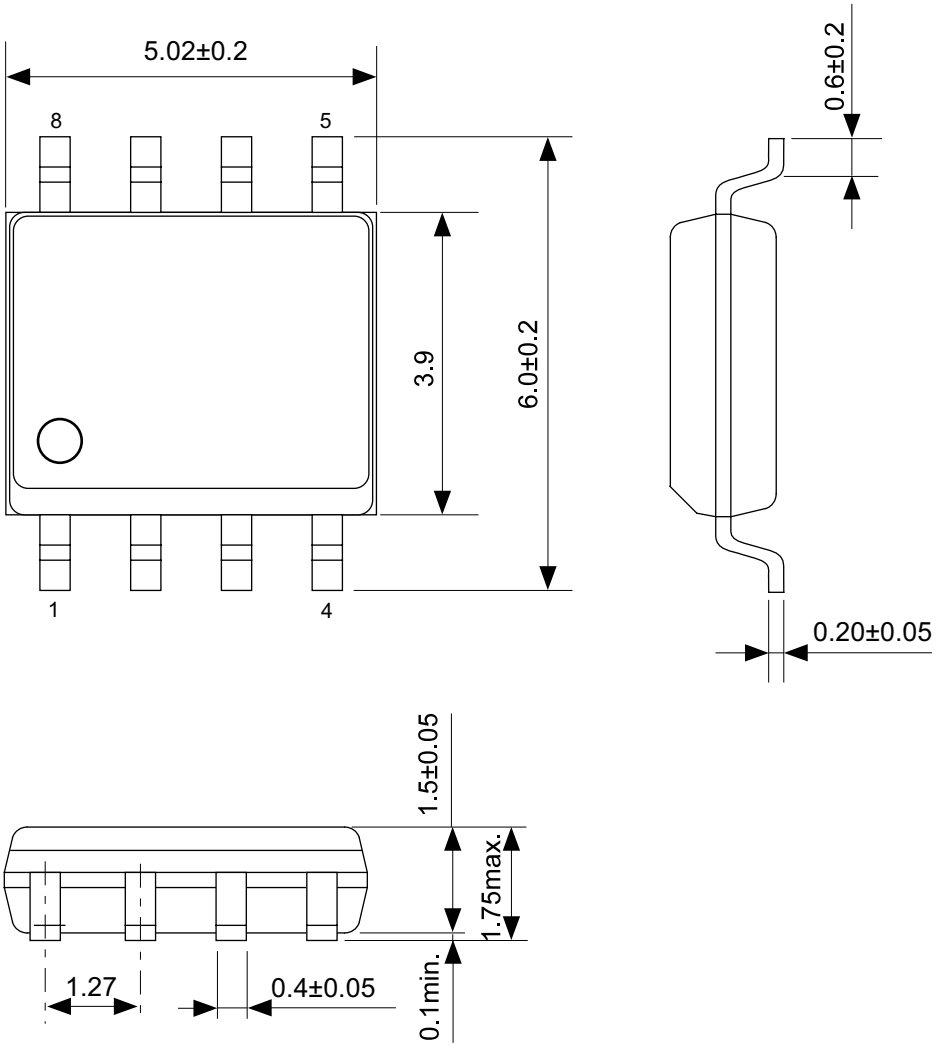
■ Precautions

- Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pins to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

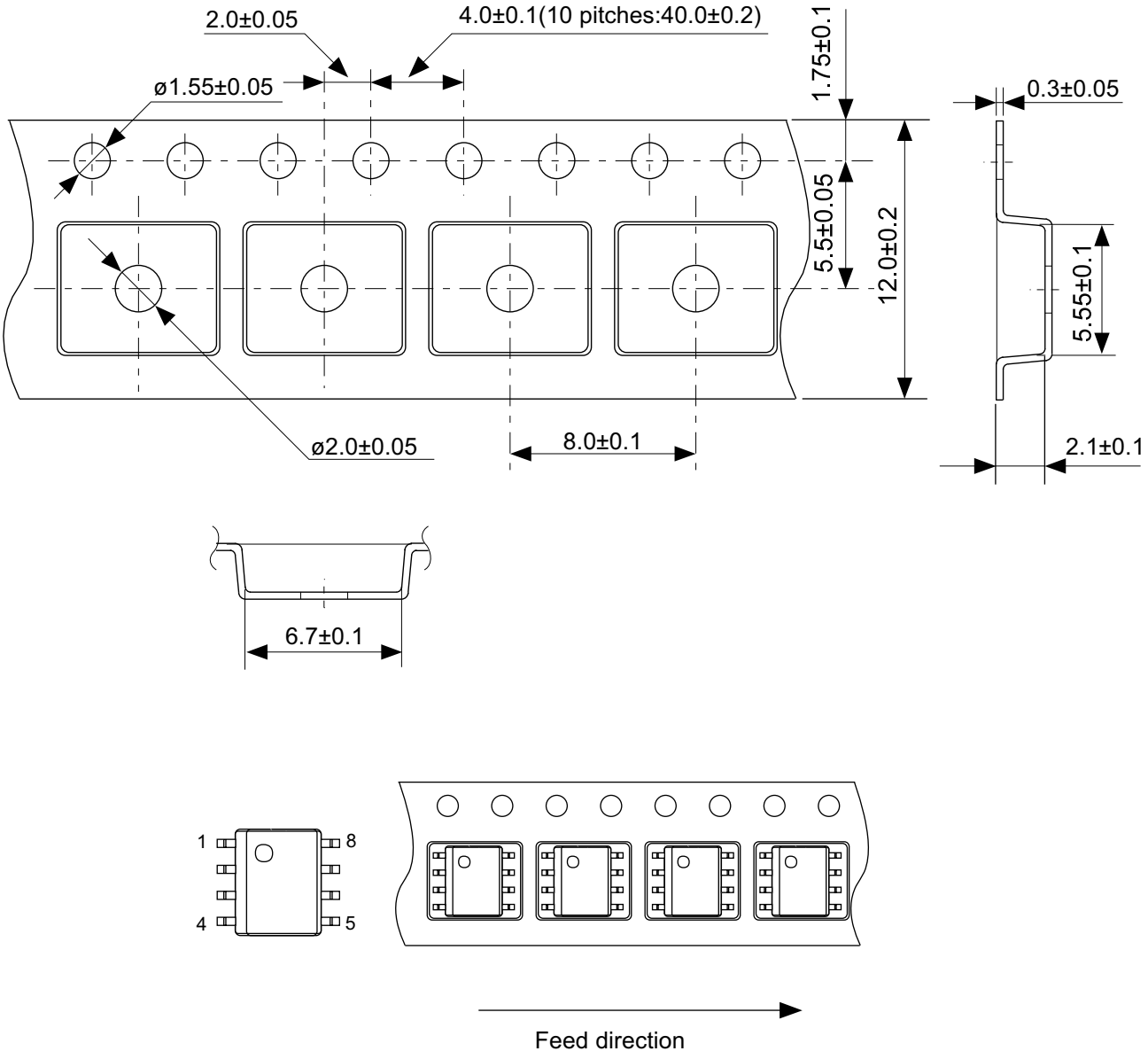
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.



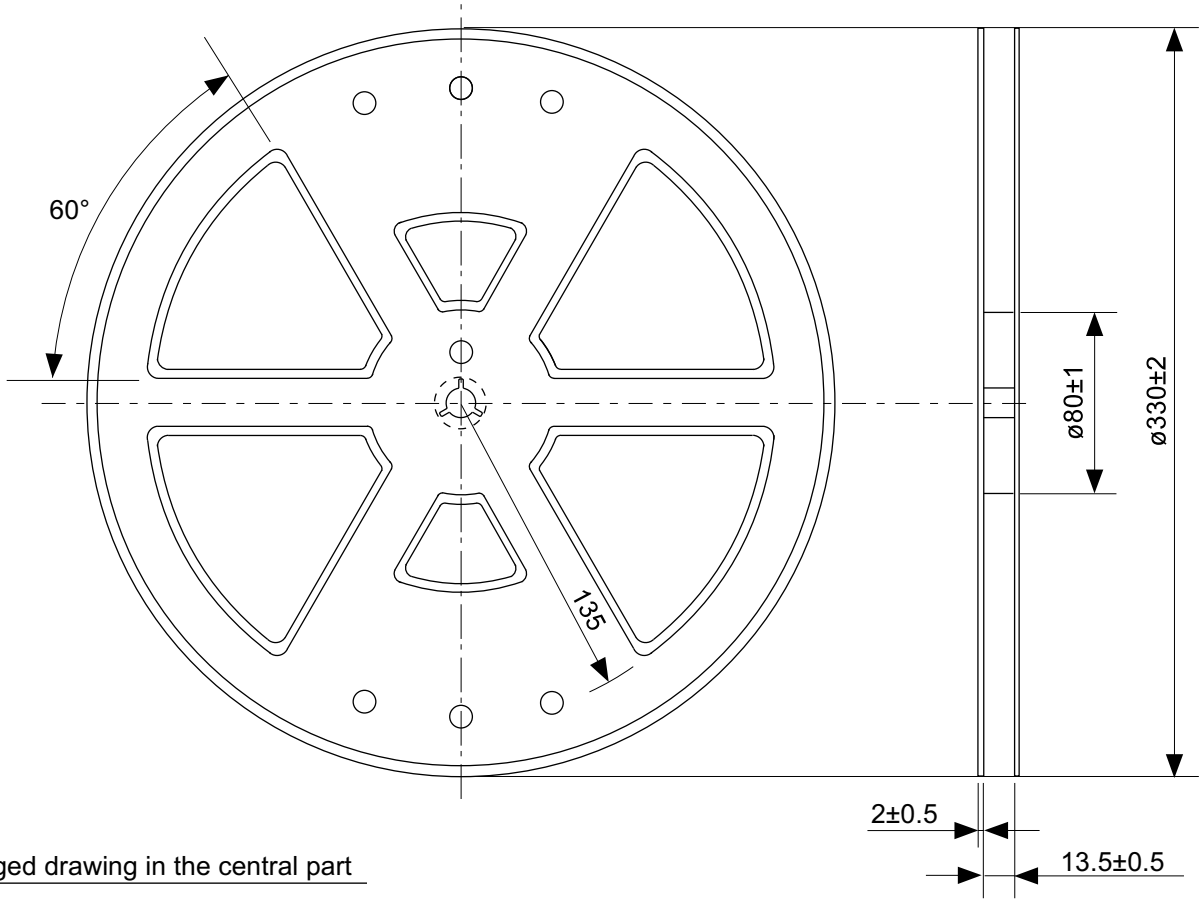
No. FJ008-A-P-SD-2.2

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.2
ANGLE	
UNIT	mm
ABLIC Inc.	

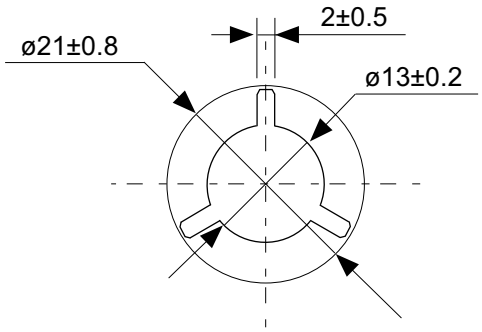


No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FJ008-D-R-SD-1.1

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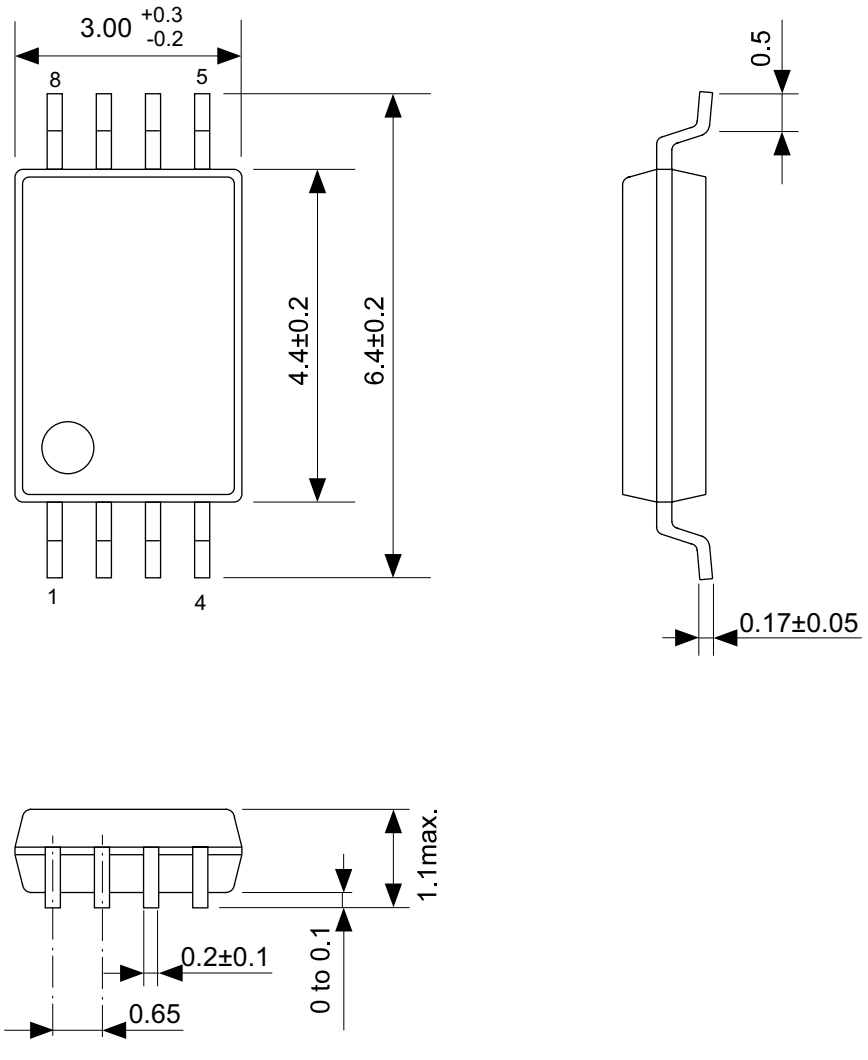
No.	FJ008-D-R-SD-1.1		
ANGLE		QTY.	2,000
UNIT	mm		
	ABLIC Inc.		



No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
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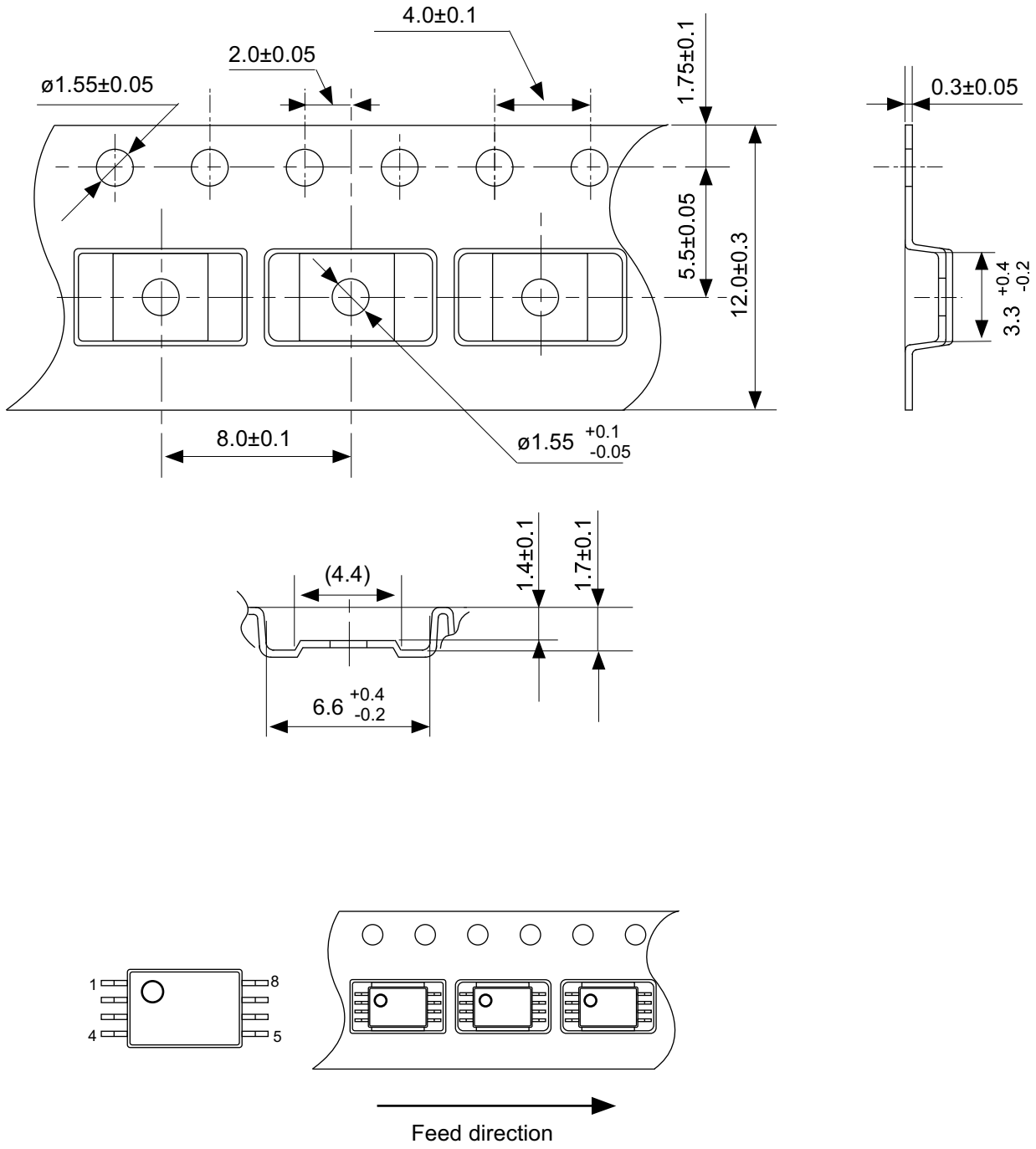
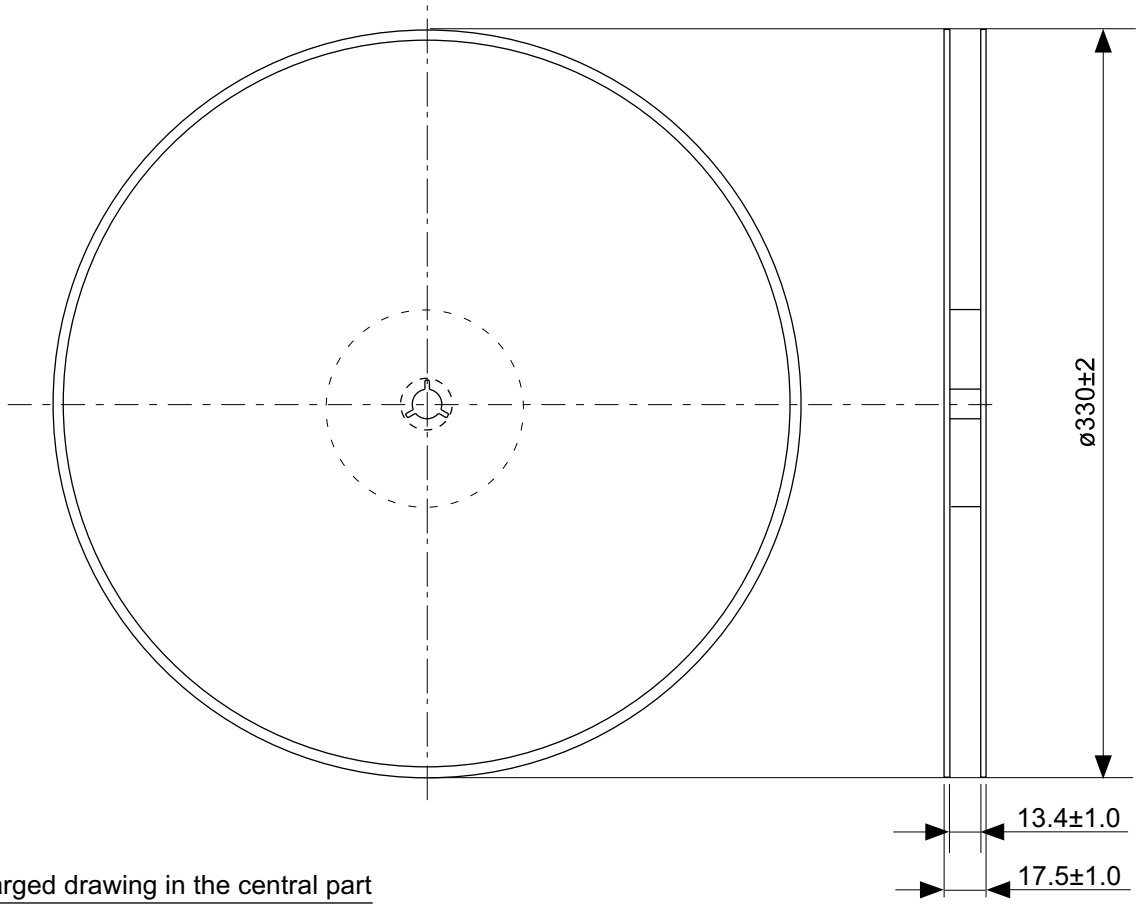
ANGLE	
UNIT	mm

ABLIC Inc.

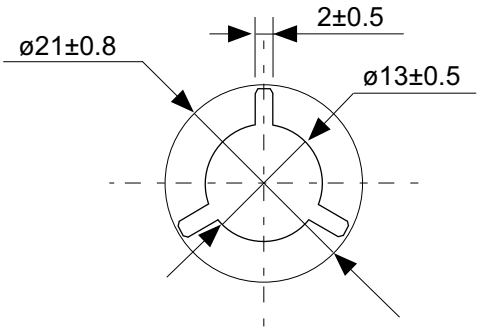


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

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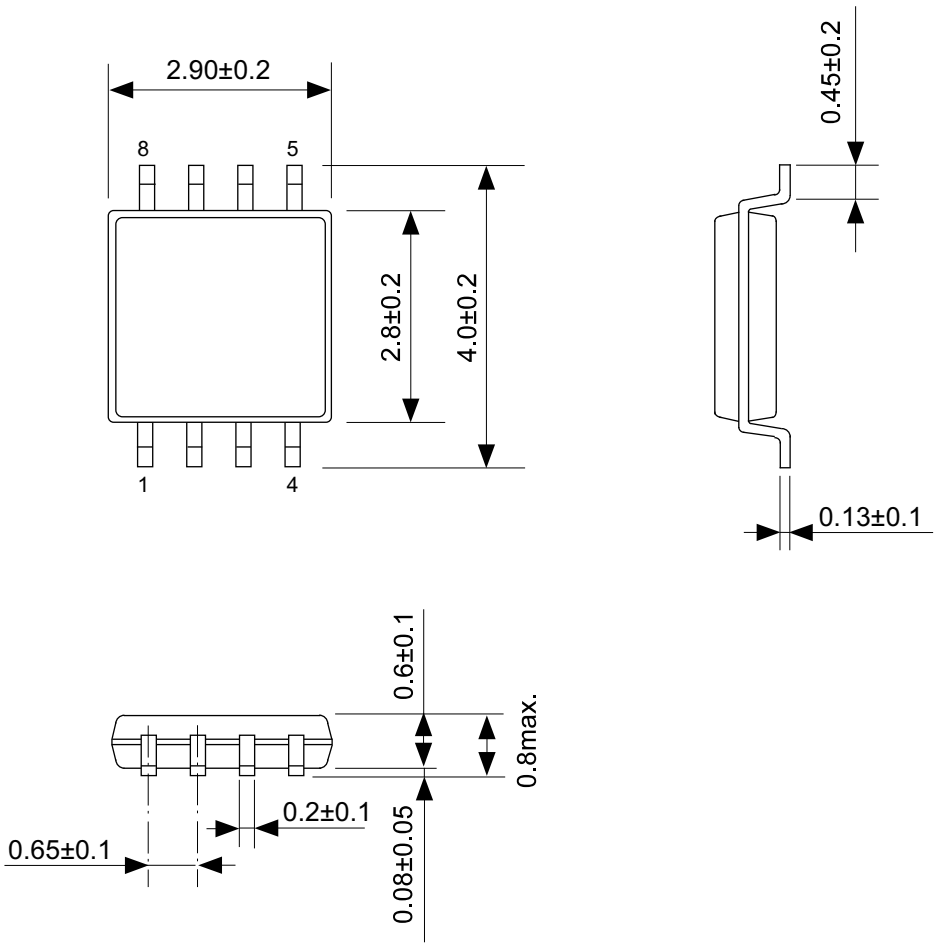
UNIT	mm		
ABLIC Inc.			



No. FM008-A-P-SD-1.2

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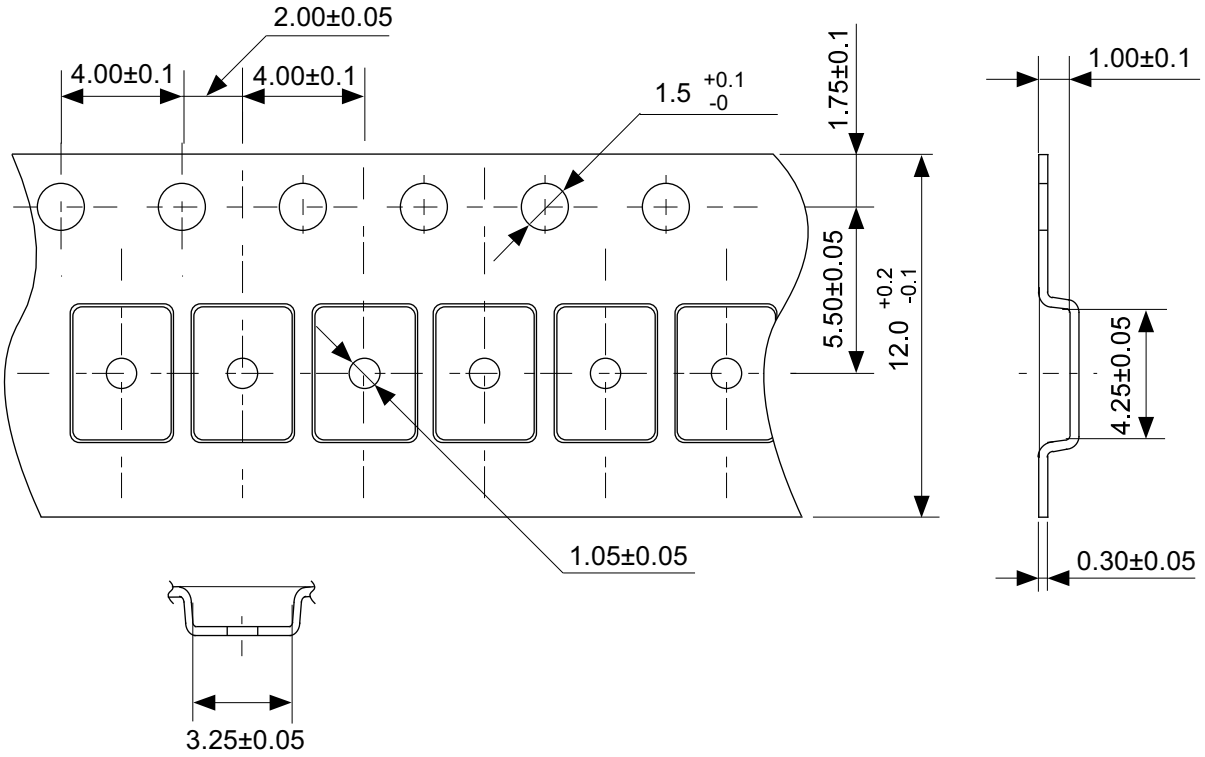
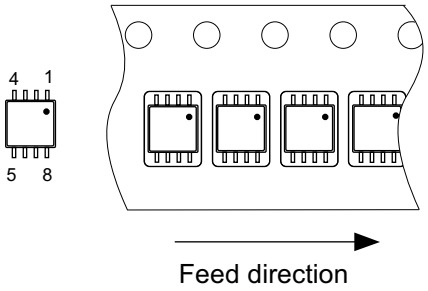
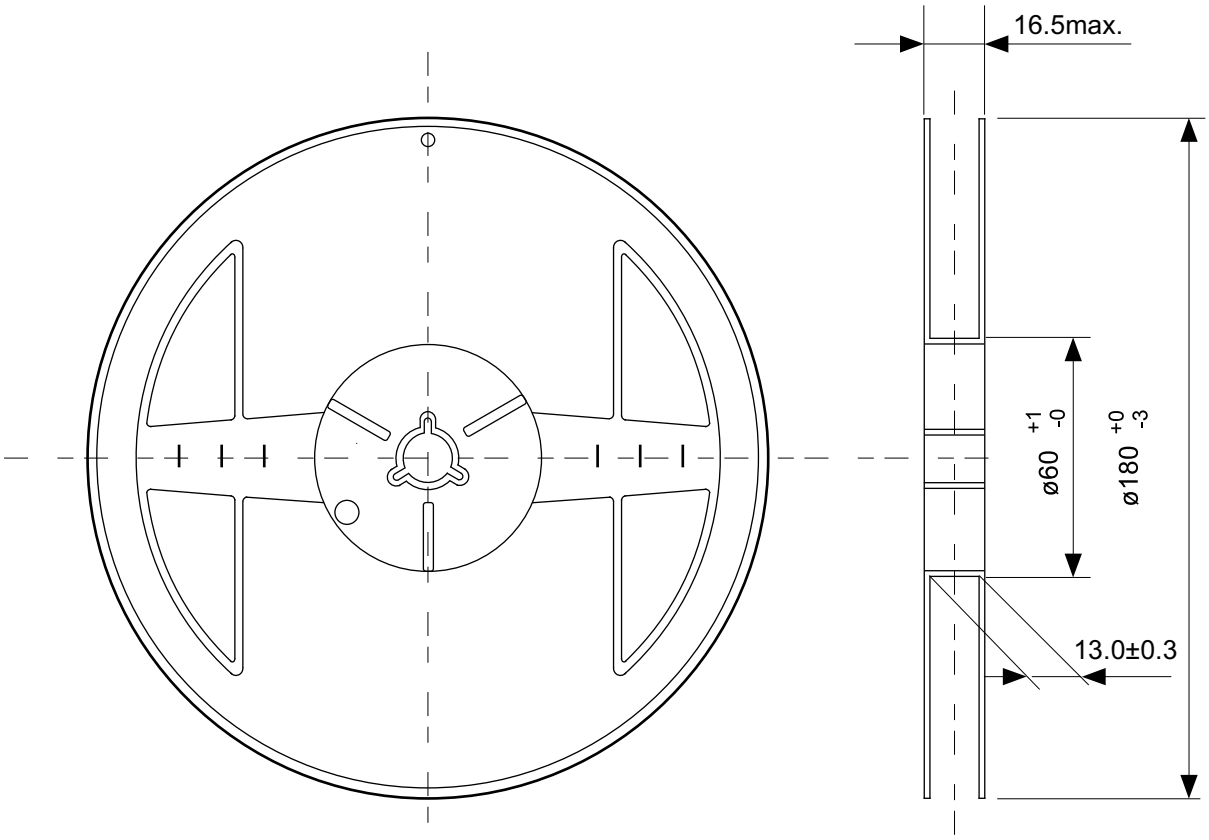
ANGLE	
UNIT	mm
ABLIC Inc.	



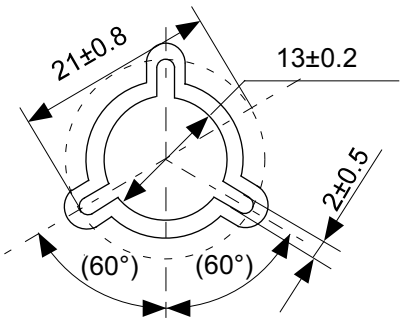


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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2.4-2019.07