## Typical Application Circuit

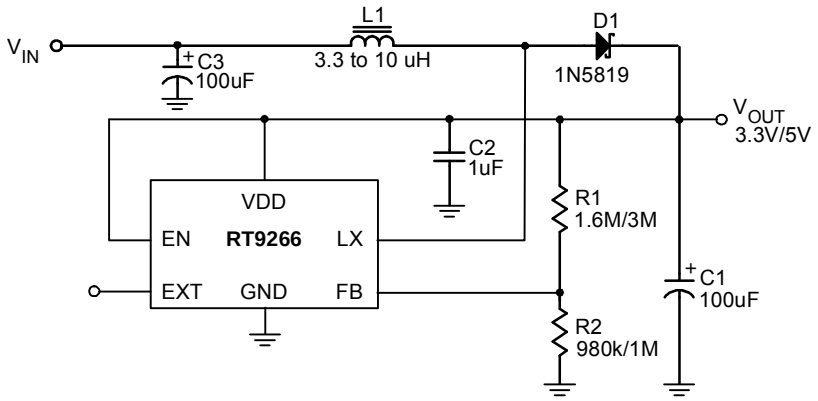



Figure 1. RT9266 Typical Application for Portable Instruments

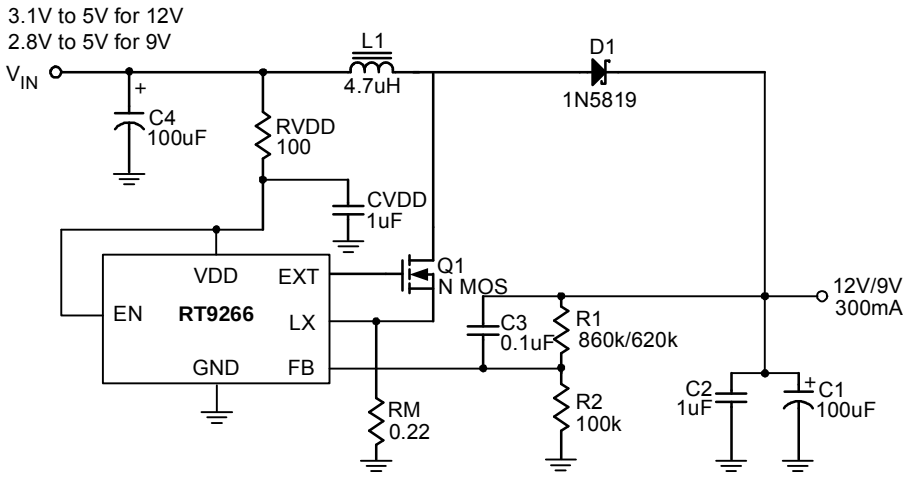



Figure 2. RT9266 High Voltage Applications

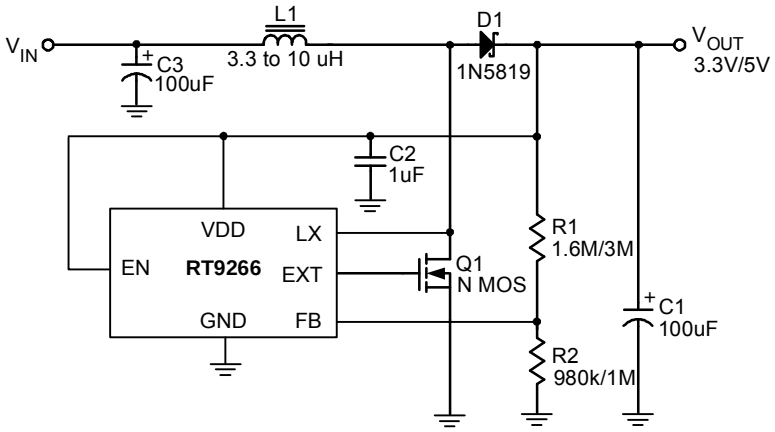



Figure 3. RT9266 for Higher Current Applications

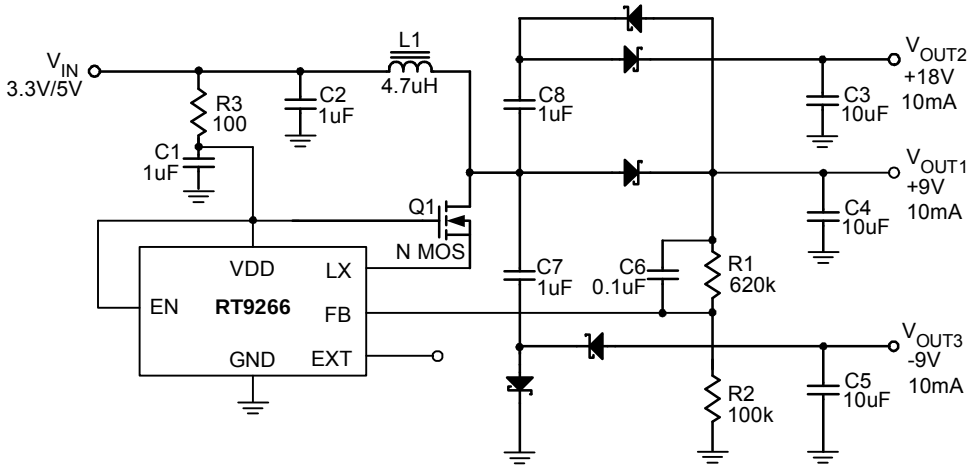
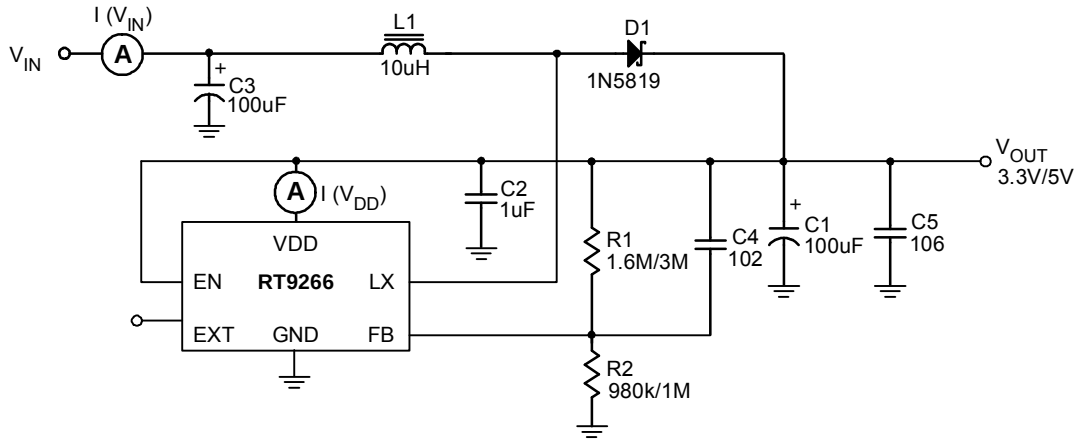



Figure 4. RT9266 for Multi-Output Applications

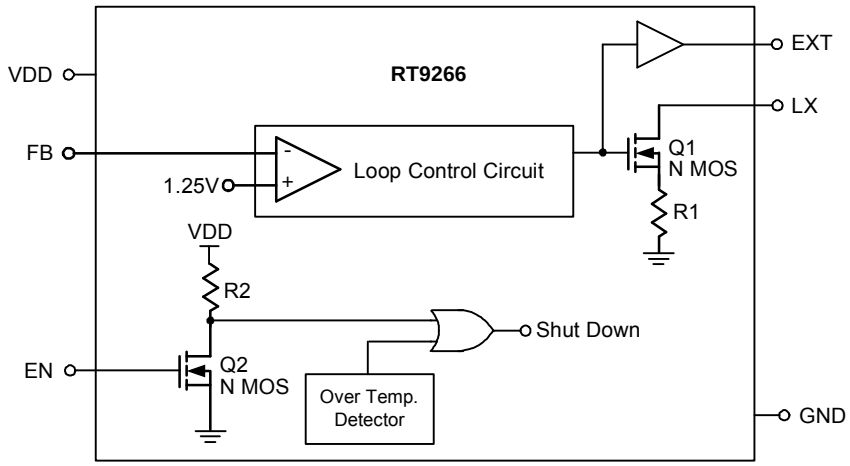
## Test Circuit




## Functional Pin Description

| Pin No. | | Pin Name | Pin Function |
|---|---|---|---|
| SOT-23-6 | SOT-89-5 | | |
| 1 | 1 | EN | Chip Enable (Active High). |
| 2 | – | EXT | Output Pin for Driving External N-MOSFET. |
| 3 | 5 | GND | Ground. |
| 4 | 4 | LX | Pin for Switching. |
| 5 | 2 | VDD | Input Positive Power Pin of RT9266. |
| 6 | 3 | FB | Feedback Input Pin.<br>Internal Reference Voltage for the Error Amplifier is 1.25V. |

## Function Block Diagram



## Absolute Maximum Ratings

- Supply Voltage ---------- –0.3V to 7V
- LX Pin Switch Voltage ---------- –0.3V to 7V
- Other I/O Pin Voltages ---------- –0.3V to ($V_{DD}$ + 0.3V)
- LX Pin Switch Current ---------- 2.5A
- EXT Pin Driver Current ---------- 200mA
- Package Thermal Resistance
  SOT-23-6, $\theta_{JC}$ ---------- 145°C/W
  SOT-89-5, $\theta_{JC}$ ---------- 45°C/W
- Operating Junction Temperature ---------- 125°C
- Storage Temperature Range ---------- –65°C to +150°C

NOTE:
Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits

## Electrical Characteristics

($V_{IN}$ = 1.5V, VDD set to 3.3V, Load Current = 0, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Start-UP Voltage | $V_{ST}$ | $I_L$ = 1mA | -- | 0.98 | 1.05 | V |
| Operating VDD Range | $V_{DD}$ | $V_{DD}$ pin voltage | 2 | -- | 6 | V |
| Shutdown Current I ($V_{IN}$) | $I_{OFF}$ | EN Pin = 0V, $V_{IN}$ = 4.5V | -- | 0.01 | 1 | µA |
| Switch-off Current I (VDD) | $I_{SWITCH\ OFF}$ | $V_{IN}$ = 6V | -- | 17 | 25 | µA |
| Continuous Switching Current | $I_{SWITCH}$ | $V_{IN}$ = EN = 3.3V, $V_{FB}$ = GND | 0.4 | 0.55 | 0.7 | mA |
| No Load Current I ($V_{IN}$) | $I_{NO\ LOAD}$ | $V_{IN}$ = 1.5V, $V_{OUT}$ = 3.3V | -- | 75* | -- | µA |
| Feedback Reference Voltage | $V_{REF}$ | Close Loop, VDD = 3.3V | 1.225 | 1.25 | 1.275 | V |
| Switching Frequency | $F_S$ | $V_{DD}$ = 3.3V | 425 | 500 | 575 | kHz |
| Maximum Duty | $D_{MAX}$ | $V_{DD}$ = 3.3V | 85 | 95 | -- | % |
| LX ON Resistance | | $V_{DD}$ = 3.3V | -- | 0.3 | 1.1 | Ω |
| Current Limit Setting | $I_{LIMIT}$ | $V_{DD}$ = 3.3V | 1.6 | 2 | 2.6** | A |
| EXT ON Resistance to VDD | | $V_{DD}$ = 3.3V | -- | 5 | 8.5 | Ω |
| EXT ON Resistance to GND | | $V_{DD}$ = 3.3V | -- | 5 | 8.5 | Ω |
| Line Regulation | $\Delta V_{LINE}$ | $V_{IN}$ = 3.5 ~ 6V, $I_L$ = 1mA | -- | 1.5 | 10 | mV/V |
| Load Regulation | $\Delta V_{LOAD}$ | $V_{IN}$ = 2.5V, $I_L$ = 1 ~ 100mA | -- | 0.25*** | -- | mV/mA |
| EN Pin Trip Level | | $V_{DD}$ = 3.3V | 0.4 | 0.8 | 1.2 | V |
| Temperature Stability for $V_{OUT}$ | $T_S$ | | -- | 50 | -- | ppm/°C |
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | | -- | 10 | -- | °C |

Note :

* No Load Current is highly dependent on practical system design and component selection that cannot be covered by production testing. Typical No Load Current is verified by typical application circuit with recommended components. No Load Current performance is guaranteed by Switch Off Current and Continuous Switching Current.

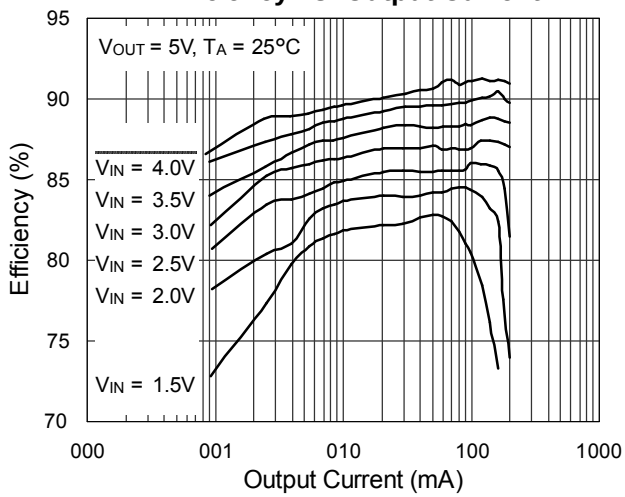
** Current Limit is guaranteed by design at $T_A$ = 25°C.

***Load Regulation is not tested at production due to practical instrument limitation. Load Regulation performance is dominantly dependent on DC loop gain and LX ON Resistance that are guaranteed by "Line Regulation" and "LX ON Resistance" tests in production.

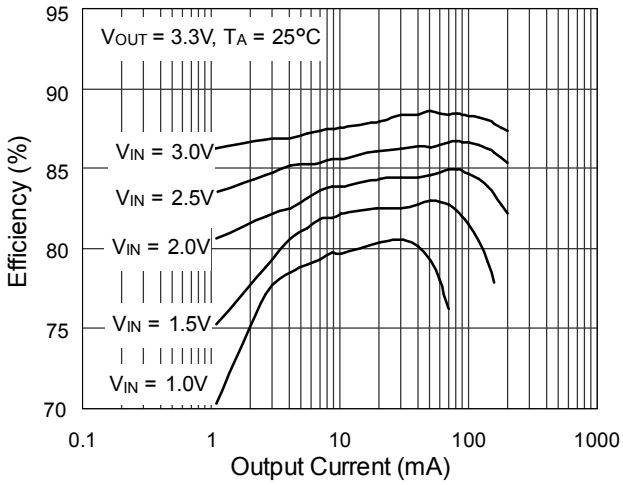
## Typical Operating Characteristics

(Refer to Test Circuit)

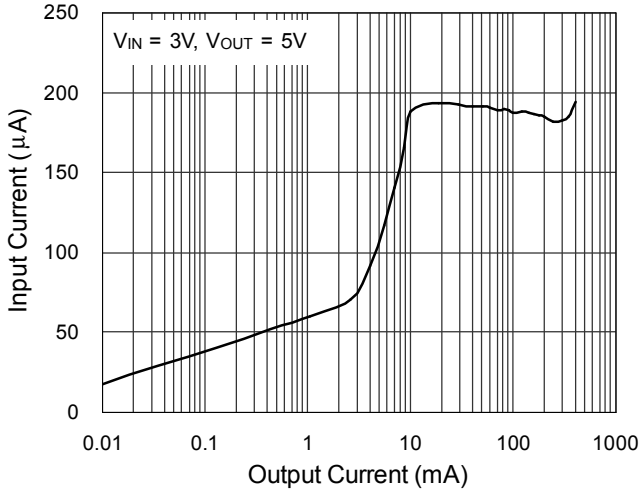
**Efficiency vs. Output Current**



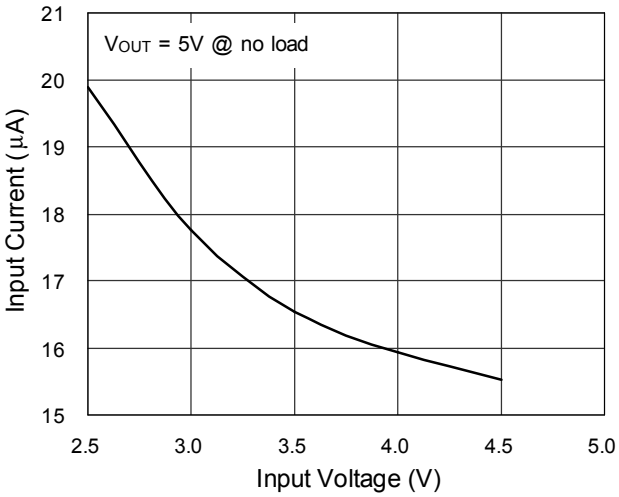

**Efficiency vs. Output Current**



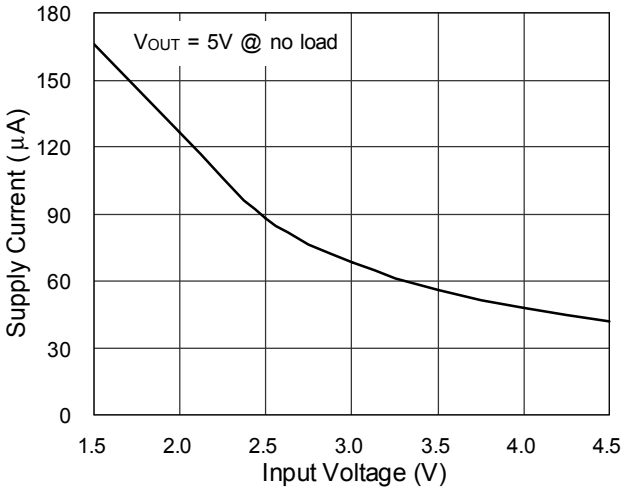

**Input Current $I(V_{DD})$ vs. Output Current**



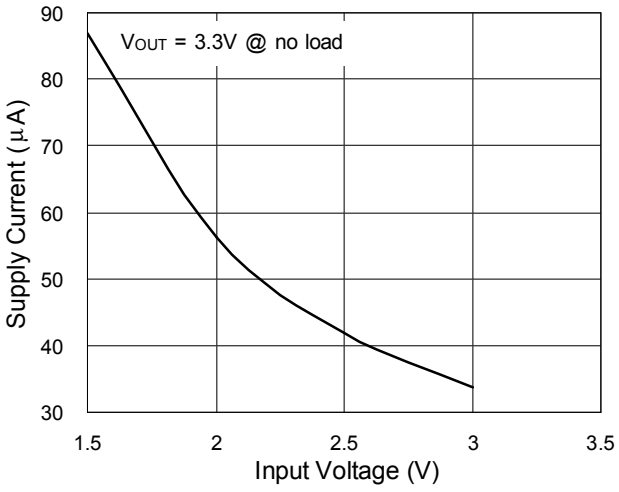

**Input Current $I(V_{DD})$ vs. Input Voltage**



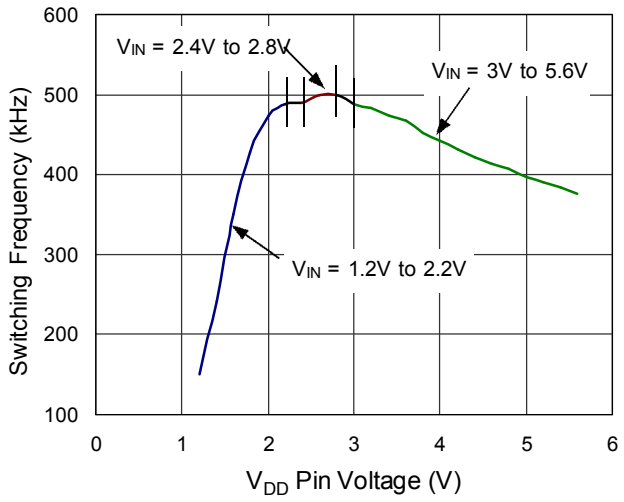

**Supply Current $I(V_{IN})$ vs. Input Voltage**



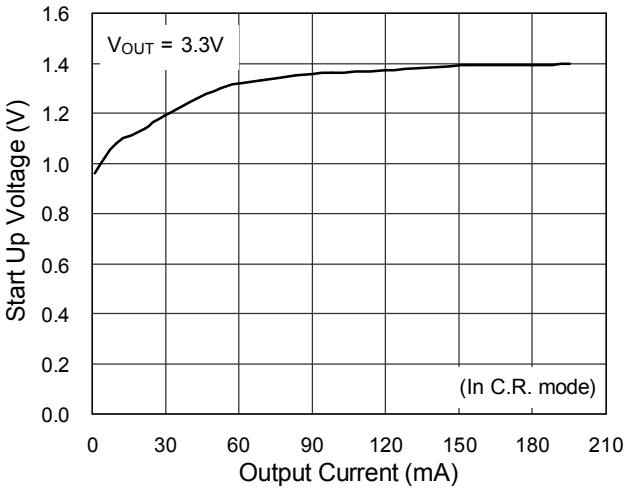

**Supply Current $I(V_{IN})$ vs. Input Voltage**



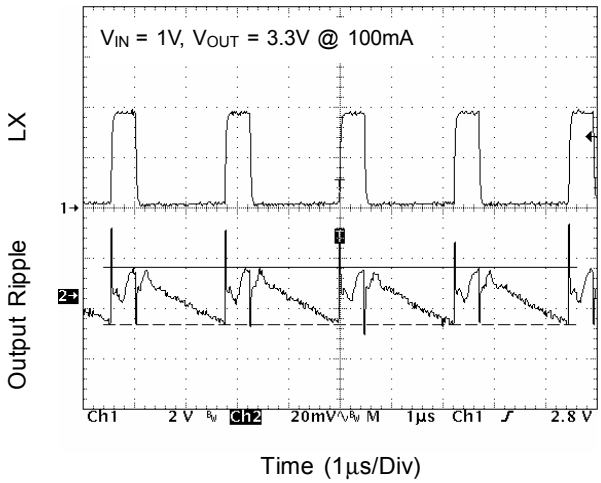
### Switching Frequency vs. VDD Pin Voltage




### Start Up Voltage vs. Output Current

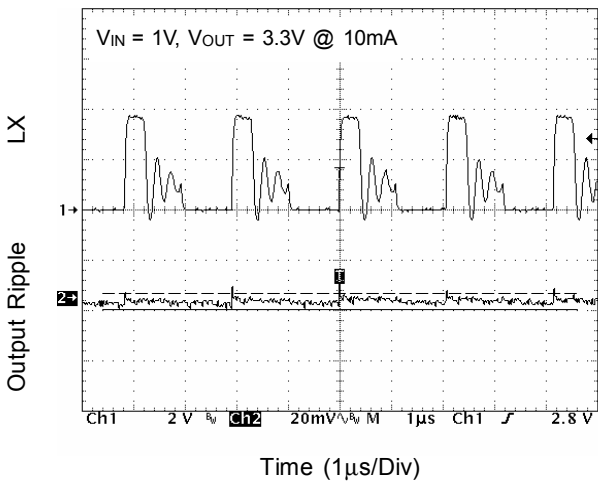



### LX & Output Ripple



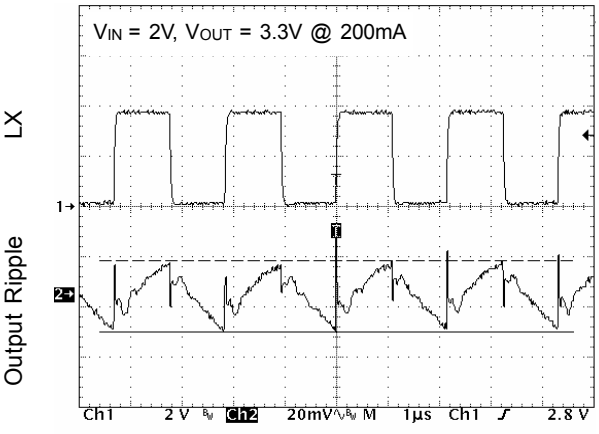

Time (1µs/Div)

### LX & Output Ripple



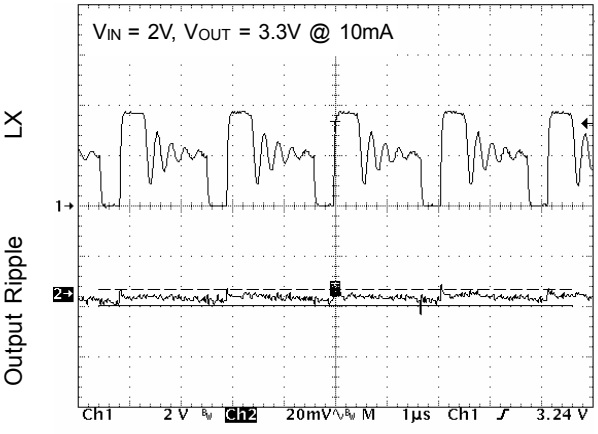

Time (1µs/Div)

### LX & Output Ripple



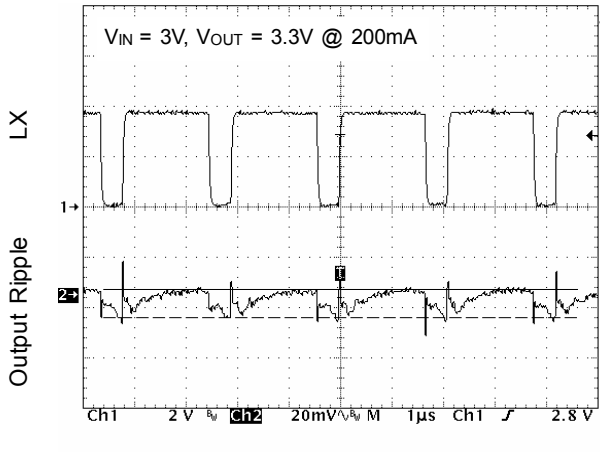

Time (1µs/Div)

### LX & Output Ripple



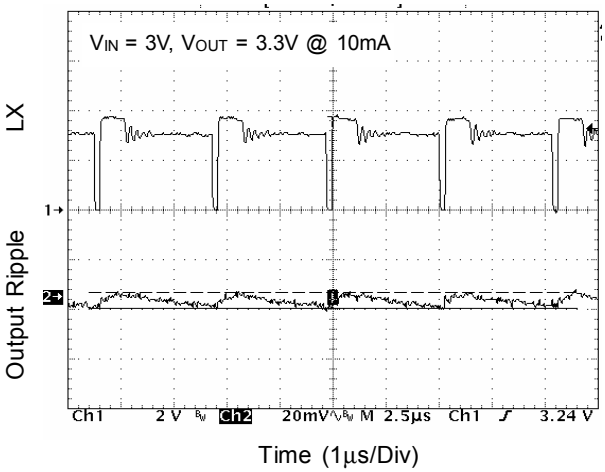

Time (1µs/Div)

**LX & Output Ripple**



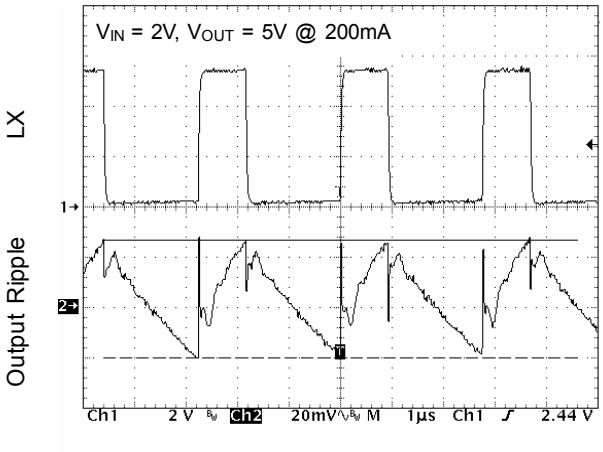

Time (1µs/Div)

**LX & Output Ripple**



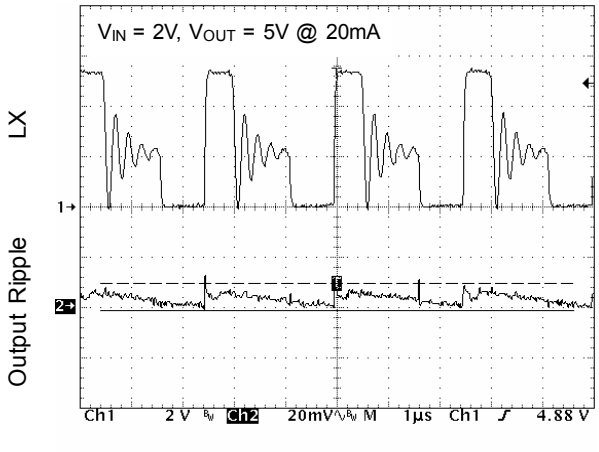

Time (1µs/Div)

**LX & Output Ripple**



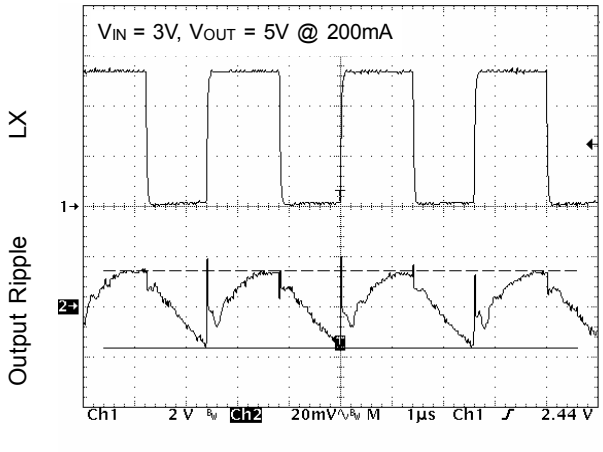

Time (1µs/Div)

**LX & Output Ripple**



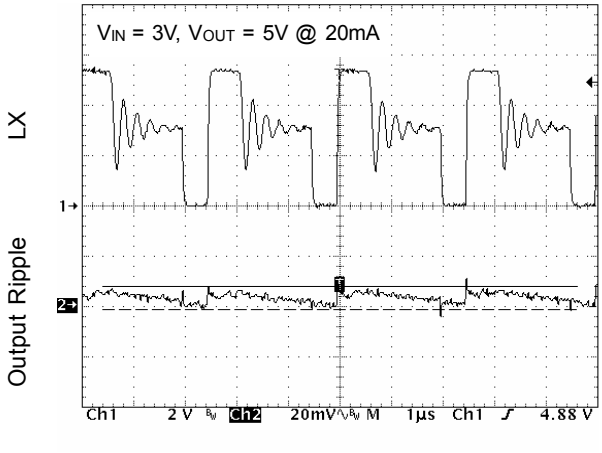

Time (1µs/Div)

**LX & Output Ripple**



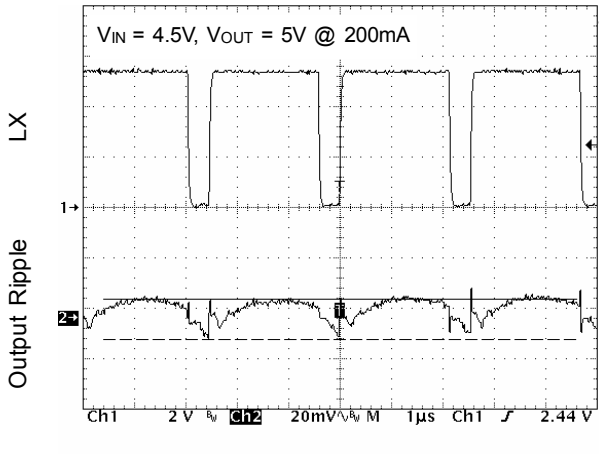

Time (1µs/Div)

**LX & Output Ripple**



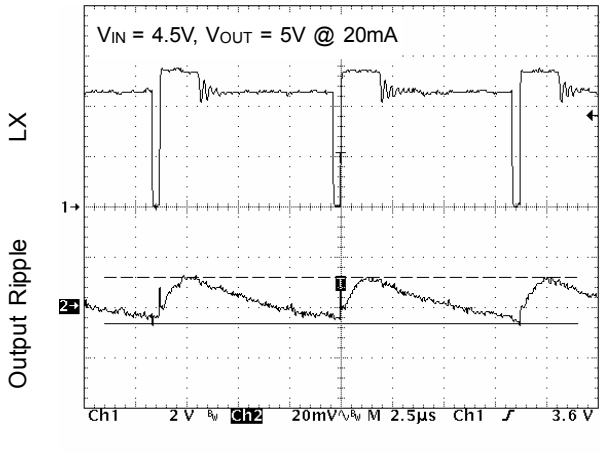

Time (1µs/Div)

### LX & Output Ripple



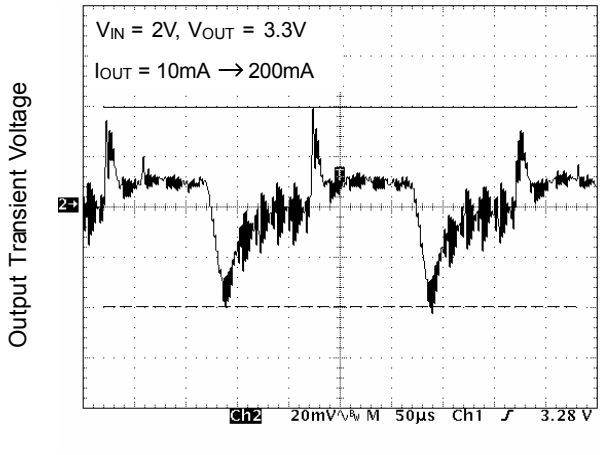

Time (1µs/Div)

### LX & Output Ripple



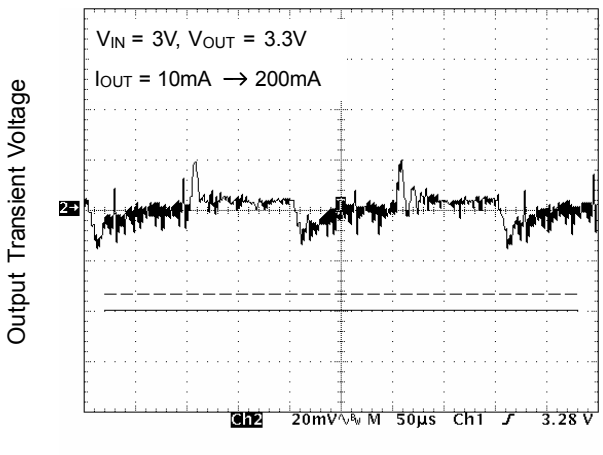

Time (1µs/Div)

### Transient Response



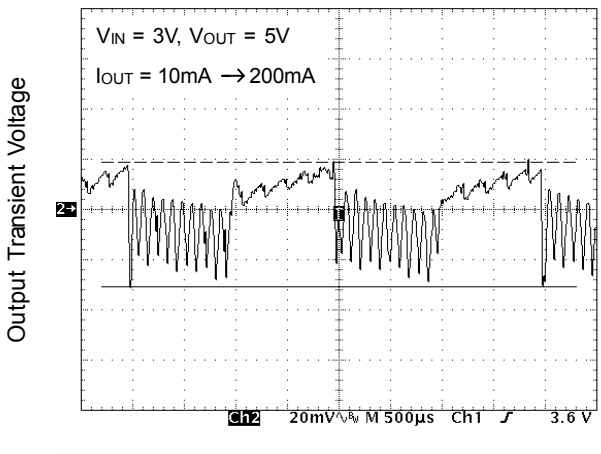

Time (50µs/Div)

### Transient Response



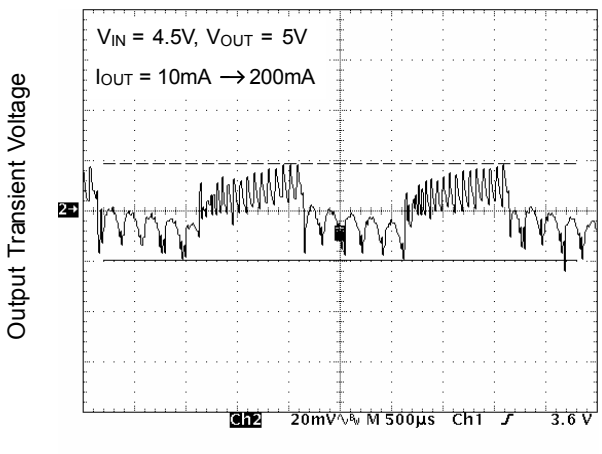

Time (50µs/Div)

### Transient Response

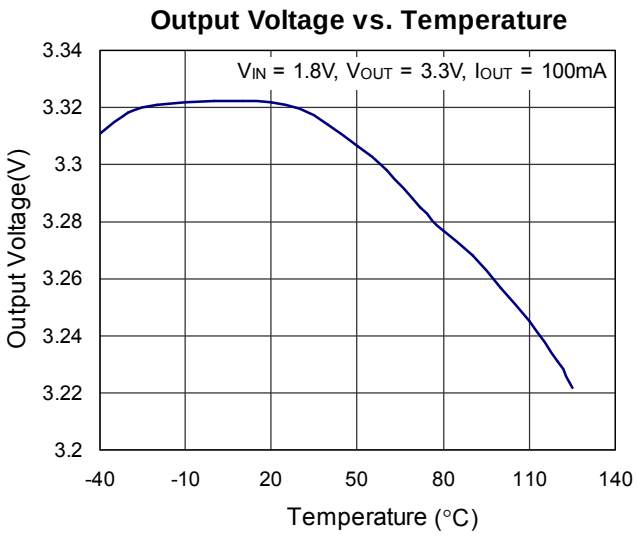


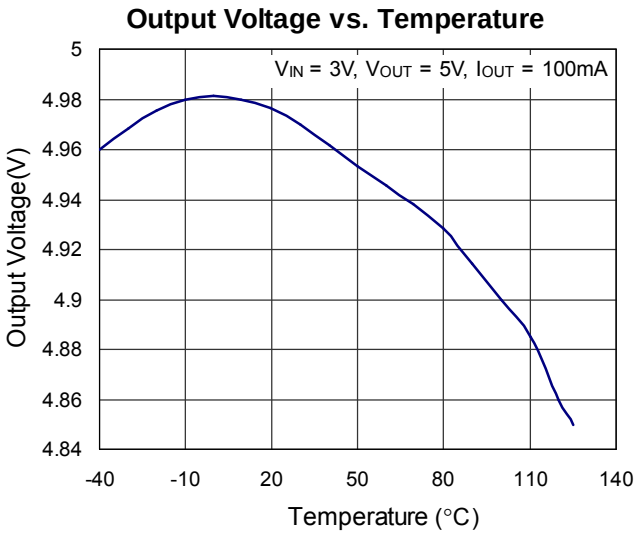

Time (50µs/Div)

### Transient Response




Time (50µs/Div)



## Application Information

### Output Voltage Setting

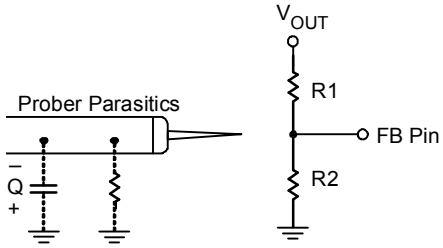
Referring to Typical Application Circuits, the output voltage of the switching regulator ($V_{OUT}$) can be set with Equation (1).

$$V_{OUT} = (1 + \frac{R1}{R2}) \times 1.25V \quad (1)$$

### Feedback Loop Design

Referring to Typical Application Circuits. The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

- Follow Equation (1)
- Higher R reduces the quiescent current (Path current = 1.25V/R2), however resistors beyond 5MΩ are not recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pins.




- A proper value of feed forward capacitor parallel with R1 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is around 0~33pF for feedback resistors of MΩ, and 10nF~0.1μF for feedback resistors of tens to hundreds kΩ.

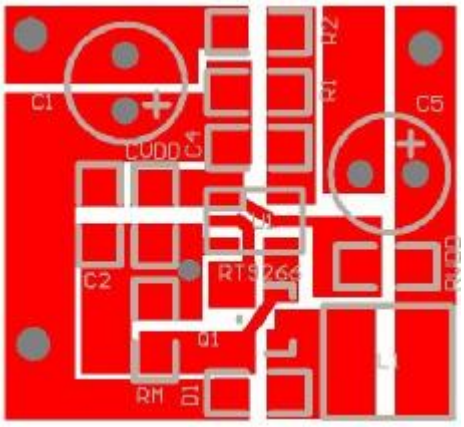
For applications without standby or suspend modes, lower values of R1 and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 and R2 are needed. Such "high impedance feedback loops" are sensitive to any interference, which require careful layout and avoid any interference, e.g. probing to FB pin.

### Layout Guide

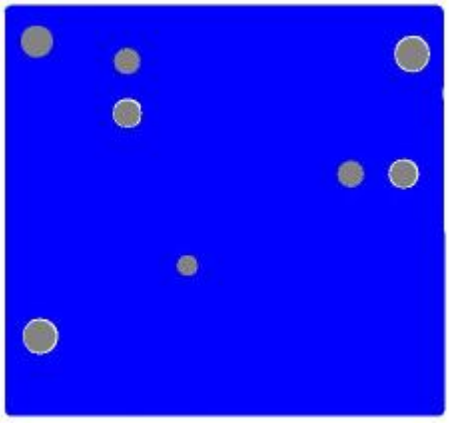
- A full GND plane without gap break.
- $V_{DD}$ to GND noise bypass – Short and wide connection for the 1μF MLCC capacitor between Pin5 and Pin3.
- $V_{IN}$ to GND noise bypass – Add a capacitor close to L1 inductor, when $V_{IN}$ is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.

### Board Layout Example (2-Layer Board)

(Refer to Typical Application Circuits Figure 2 for the board)

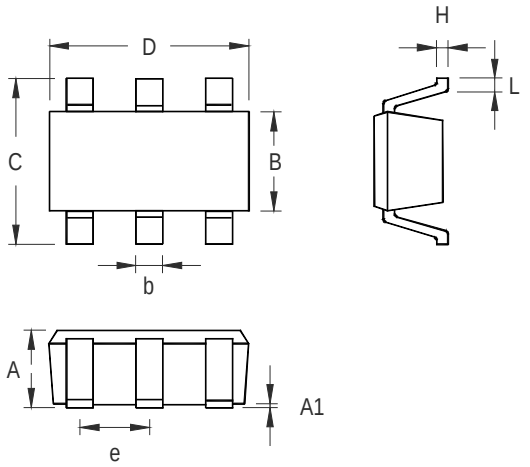



- Top Layer -



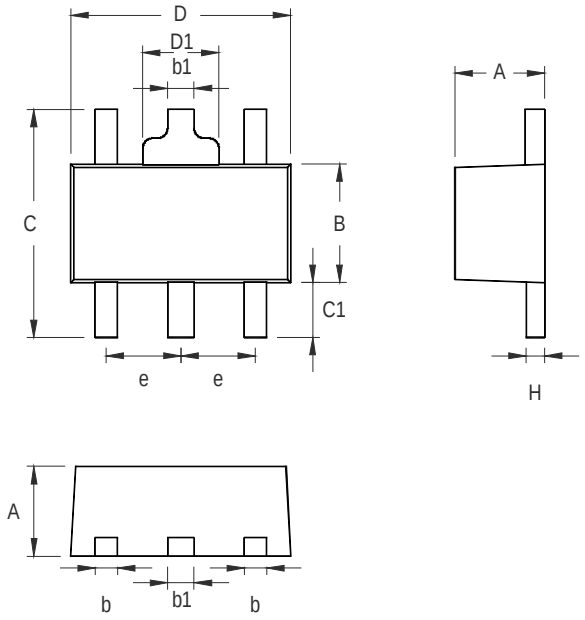
- Bottom Layer -

## Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.889 | 1.295 | 0.031 | 0.051 |
| A1 | 0.000 | 0.152 | 0.000 | 0.006 |
| B | 1.397 | 1.803 | 0.055 | 0.071 |
| b | 0.250 | 0.560 | 0.010 | 0.022 |
| C | 2.591 | 2.997 | 0.102 | 0.118 |
| D | 2.692 | 3.099 | 0.106 | 0.122 |
| e | 0.838 | 1.041 | 0.033 | 0.041 |
| H | 0.080 | 0.254 | 0.003 | 0.010 |
| L | 0.300 | 0.610 | 0.012 | 0.024 |

**SOT-23-6 Surface Mount Package**




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.397 | 1.600 | 0.055 | 0.063 |
| b | 0.356 | 0.508 | 0.014 | 0.020 |
| B | 2.388 | 2.591 | 0.094 | 0.102 |
| b1 | 0.406 | 0.533 | 0.016 | 0.021 |
| C | 3.937 | 4.242 | 0.155 | 0.167 |
| C1 | 0.787 | 1.194 | 0.031 | 0.047 |
| D | 4.394 | 4.597 | 0.173 | 0.181 |
| D1 | 1.397 | 1.702 | 0.055 | 0.067 |
| e | 1.397 | 1.600 | 0.055 | 0.063 |
| H | 0.356 | 0.432 | 0.014 | 0.017 |

**5-Lead SOT-89 Surface Mount Package**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