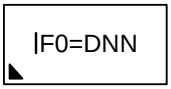
Marking Information

R7732GGE



|F0= : Product Code
DNN : Date Code

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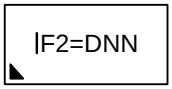

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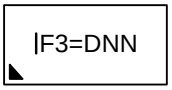

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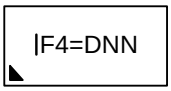

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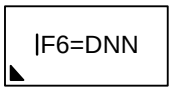
R7732RGE

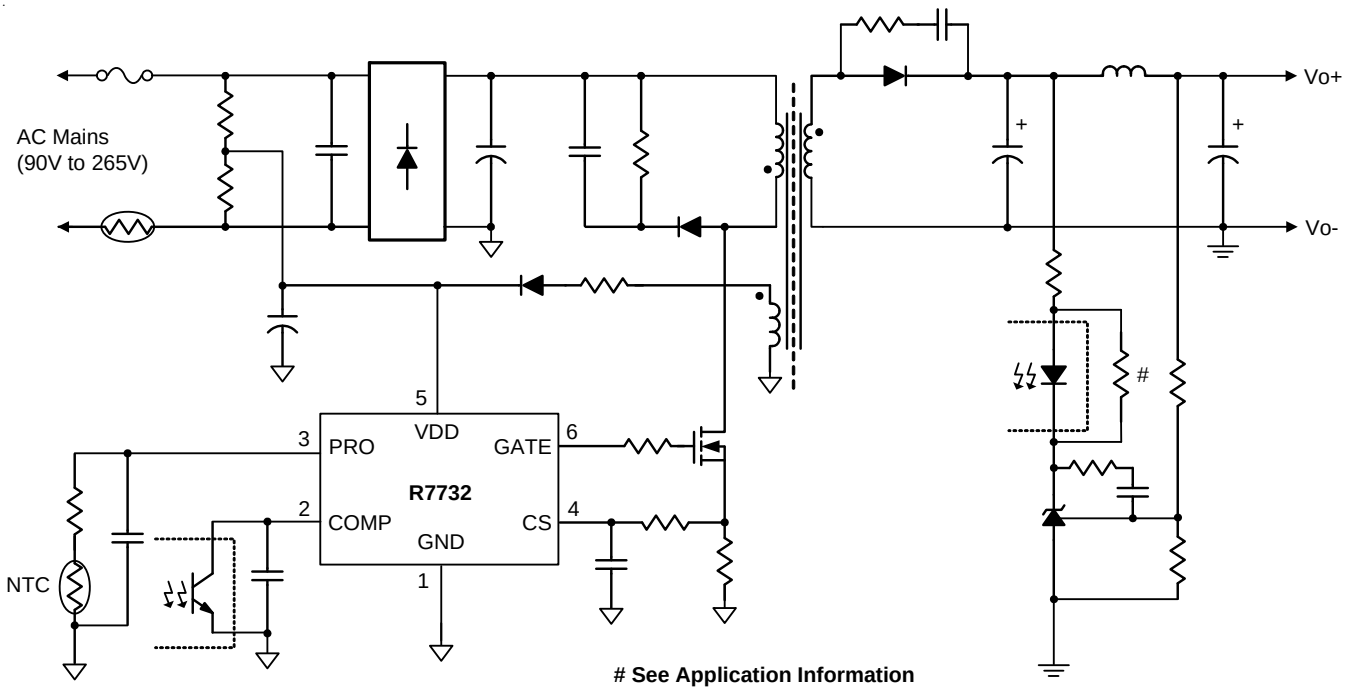


|F6= : Product Code
DNN : Date Code

R7732 Version Table

Version	R7732G	R7732R	R7732L	R7732A	R7732H
Frequency	65kHz	65kHz	65kHz	65kHz	100kHz
OLP Delay Time	56ms	56ms	56ms	28ms	36ms
Internal OVP(27V)	Auto Recovery	Auto Recovery	Latch	Latch	Auto Recovery
OLP & SRSP	Auto Recovery	Auto Recovery	Auto Recovery	Latch	Auto Recovery
PRO Pin High	Latch	Auto Recovery	Latch	Latch	Auto Recovery
PRO Pin Low	Auto Recovery	Latch	Latch	Latch	Latch

Typical Application Circuit

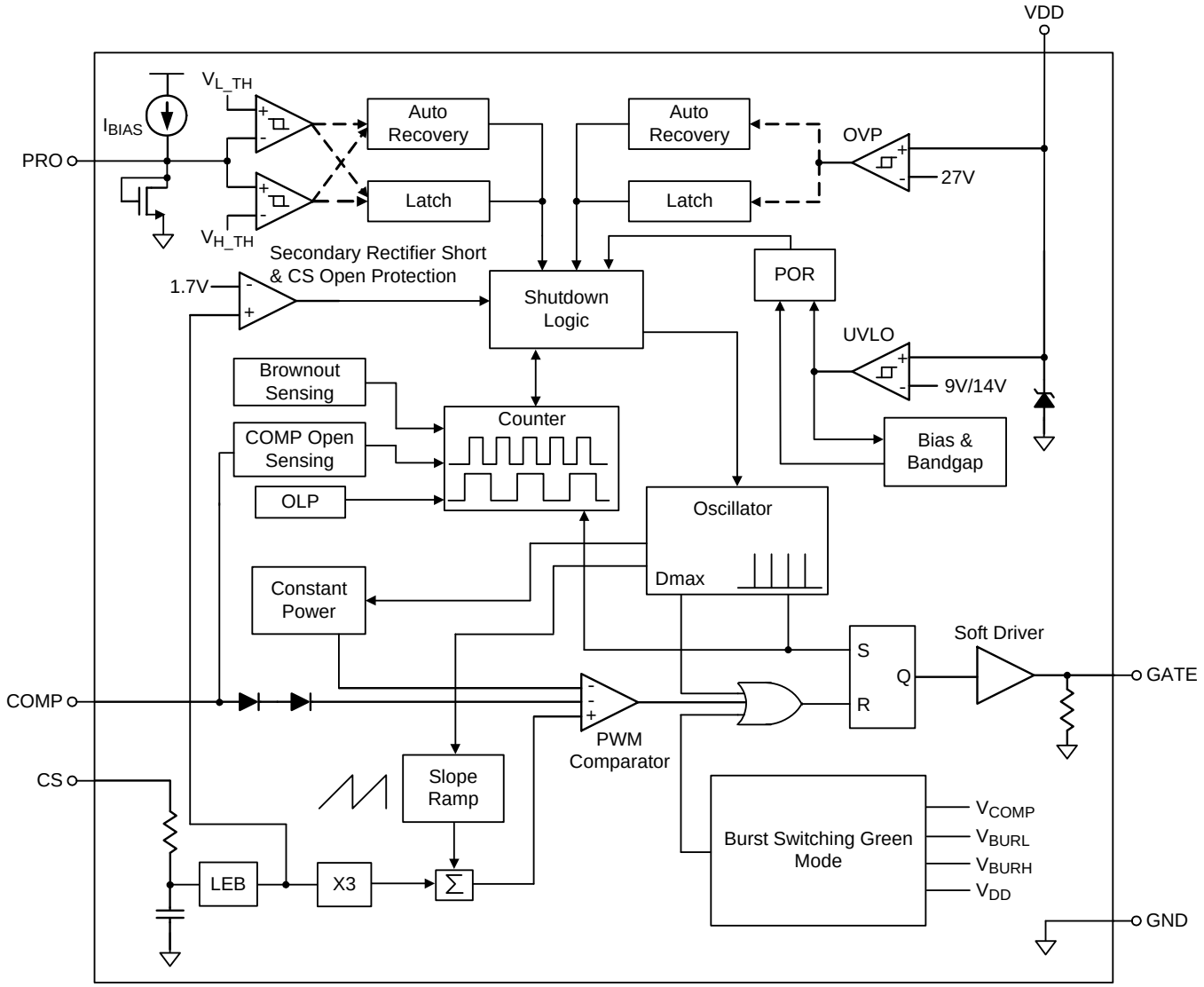


 # See Application Information

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground.
2	COMP	Voltage Feedback Pin. By connecting an opto-coupler to close control loop and achieve the regulation.
3	PRO	For External Arbitrary OVP or OTP.
4	CS	Primary Current Sense Pin.
5	VDD	Power Supply Pin.
6	GATE	Gate Drive Output to drive the external MOSFET.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{DD} ---------- –0.3V to 30V
- GATE Pin ---------- –0.3V to 16.5V
- PRO, COMP, CS Pin ---------- –0.3V to 6.5V
- I_{DD} ---------- 10mA
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.4W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 250°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 3kV
  MM (Machine Mode) ---------- 250V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{DD} ---------- 12V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section						
V_{DD} Over Voltage Protection Level	V_{OVP}		26	27	28	V
V_{DD} Zener Clamp	V_Z		29	--	--	V
On Threshold Voltage	V_{TH_ON}		13	14	15	V
Off Threshold Voltage	V_{TH_OFF}		8.5	9	9.5	V
VDD Holdup Mode Entry Point	V_{DD_LOW}	V_{COMP} <1.6V	--	10	--	V
VDD Holdup Mode Ending Point	V_{DD_HIGH}	V_{COMP} <1.6V	--	10.5	--	V
Latch-off Voltage	V_{LH}		--	14	--	V
Latched Reset Voltage	V_{LH_RST}		--	9	--	V
Start-up Current	I_{DD_ST}	V_{DD} = V_{TH_ON} – 0.2V, T_A= –40°C to 100°C (Note 5)	--	20	35	μA
Operating Supply Current	I_{DD_OP}	V_{DD}= 15V, V_{COMP} = 2.5V, GATE pin open	--	1.3	2.2	mA
Latch-off Operating Current	I_{DD_LH}	T_A= –40°C to 100°C (Note 5)	--	--	40	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Section						
Normal PWM Frequency	f_{OSC}	R7732G/R/L/A	60	65	70	kHz
		R7732H	92	100	108	kHz
Minimum Burst Switching Green Mode Frequency	f_{BS_MIN}	R7732G/R/L/A	18	22	--	kHz
		R7732H	--	25	--	kHz
Maximum Duty Cycle	DCY_{MAX}		70	75	80	%
PWM Frequency Jitter Range	△f		--	±6	--	%
PWM Frequency Jitter Period	T_{JIT}	For 65kHz	--	4	--	ms
Frequency Variation Versus V_{DD} Deviation	f_{DV}	V_{DD} = 12V to 25V	--	--	2	%
Frequency Variation Versus Temperature Deviation	f_{DT}	T_A= −30°C to 105°C (Note 5)	--	--	5	%
COMP Input Section						
Open-Loop Voltage	V_{COMP_OP}	COMP pin open	5.5	5.75	6	V
COMP Open-Loop Protection Delay Time	T_{OLP}	R7732G/R/L	--	56	--	ms
		R7732A	--	28	--	ms
		R7732H	--	36	--	ms
Short Circuit Current	I_{ZERO}	V_{COMP} = 0V	--	1.2	2.2	mA
Burst Switching Green Mode Entry Voltage	V_{BS_ET}		--	3	--	V
Burst Switching Green Mode Ending Voltage	V_{BS_ED}	R7732G/R/L/A	--	2.9	--	V
		R7732H	--	2.8	--	
Current-Sense Section						
Initial Peak Current Limitation Offset	V_{CS_TH}	(Note 5)	0.68	0.7	0.72	V
Leading Edge Blanking Time	T_{LEB}	(Note 6)	150	250	350	ns
Internal Propagation Delay Time	T_{PD}	(Note 6)	--	100	--	ns
Minimum On Time	T_{ON_MIN}		250	350	450	ns
GATE Section						
Rising Time	T_R	V_{DD} = 15V, C_L = 1nF	--	125	--	ns
Falling Time	T_F	V_{DD} = 15V, C_L = 1nF	--	40	--	ns
GATE Output Clamping Voltage	V_{CLAMP}	V_{DD} = 25V	--	14	--	V
PRO Interface Section						
Pull Low Threshold	V_{L_TH}		0.47	0.5	0.53	V
Pull High Threshold	V_{H_TH}		3.5	3.8	4.1	V
Internal Bias Current	I_{BIAS}		90	100	110	μA
Pull High Sinking Current	I_{SINK}	(Note 7)	--	--	1.2	mA

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

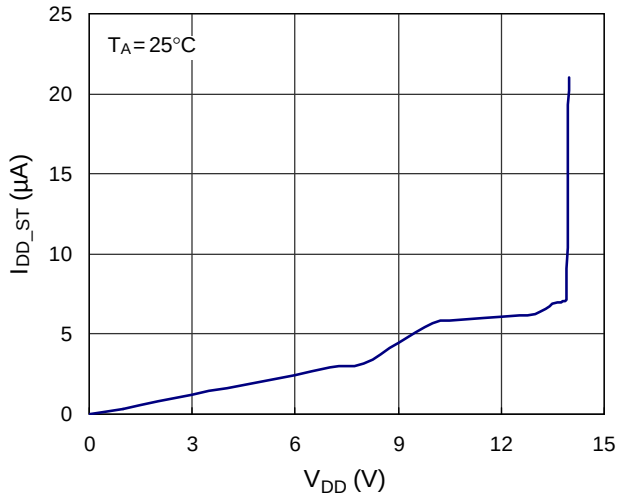
Note 5. Guaranteed by design.

Note 6. Leading edge blanking time and internal propagation delay time are guaranteed by design.

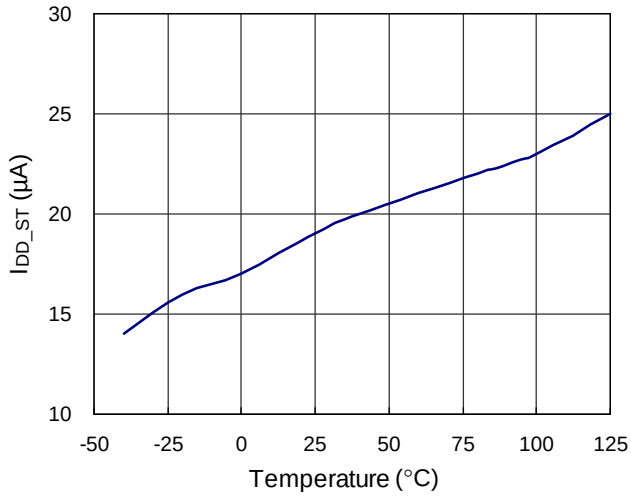
Note 7. The sourcing current of PRO pin must be limited below 5mA. Otherwise it may cause permanent damage to the device.

Typical Operating Characteristics

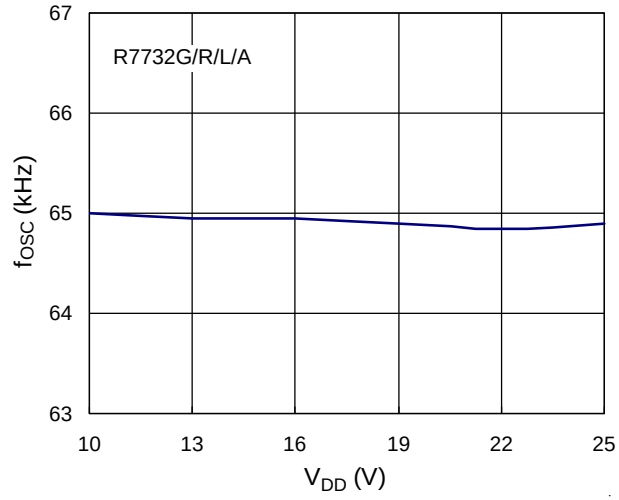
I_{DD_ST} vs. V_{DD}



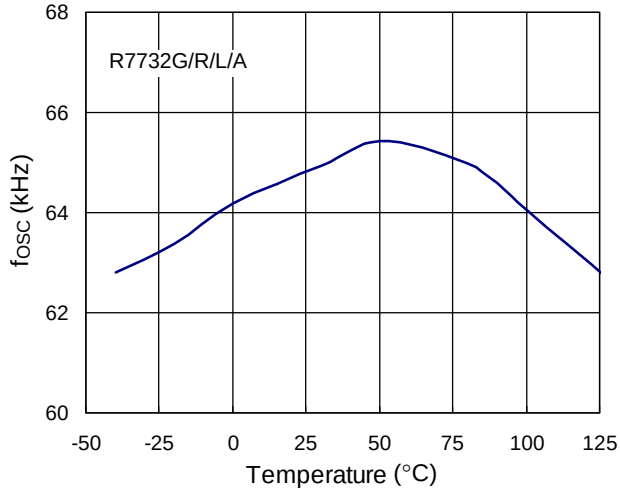
I_{DD_ST} vs. Temperature



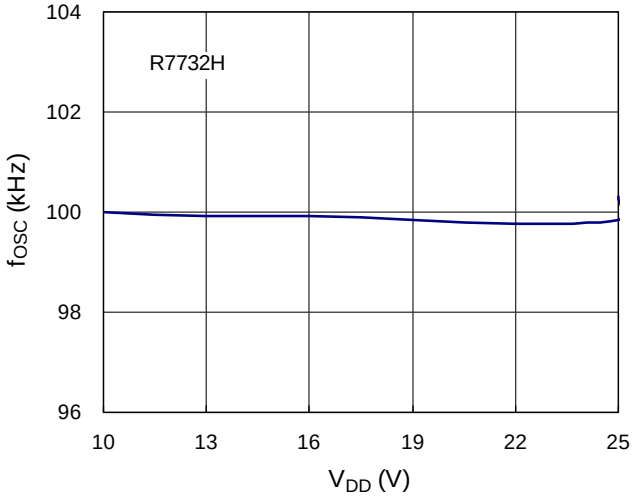
f_{OSC} vs. V_{DD}



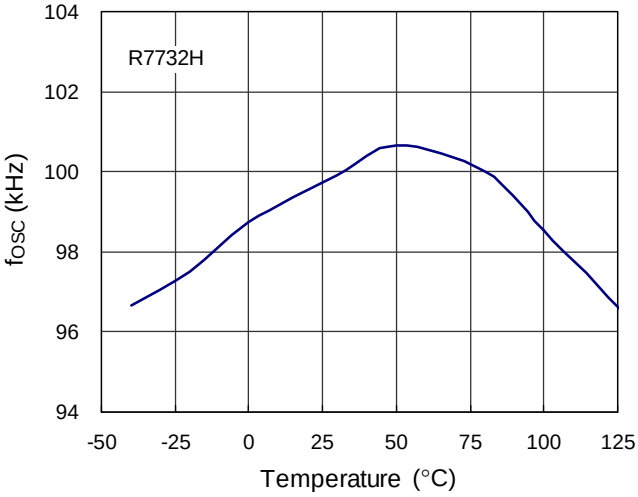
f_{OSC} vs. Temperature



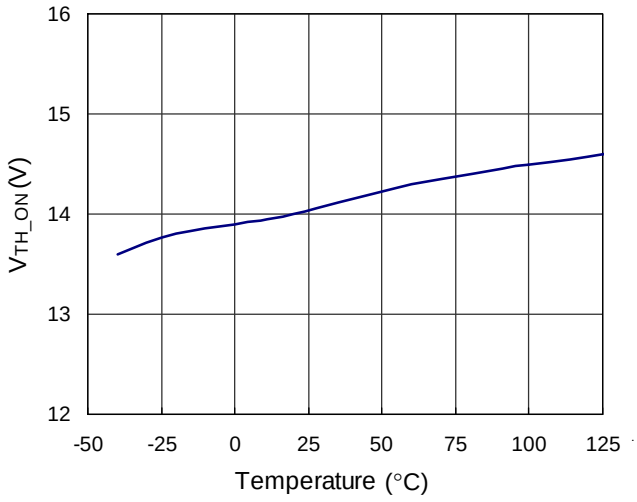
f_{OSC} vs. V_{DD}



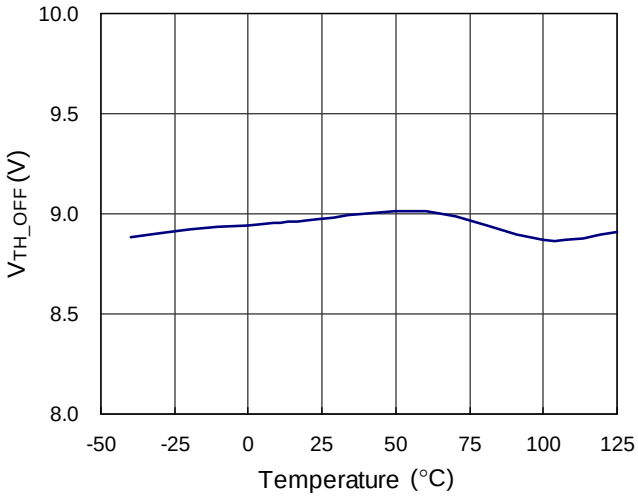
f_{OSC} vs. Temperature



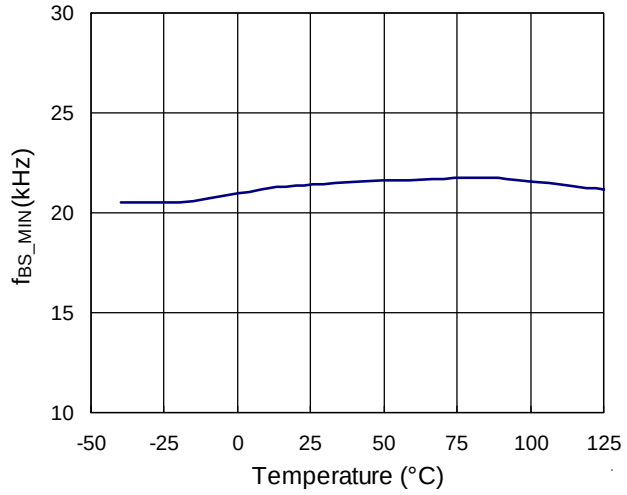
V_{TH_ON} vs. Temperature



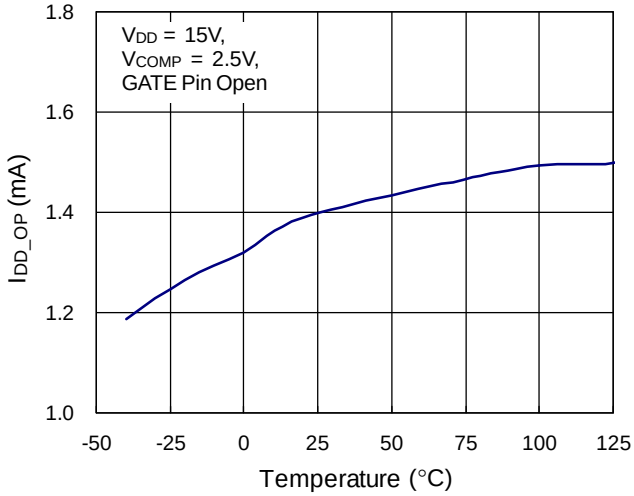
V_{TH_OFF} vs. Temperature



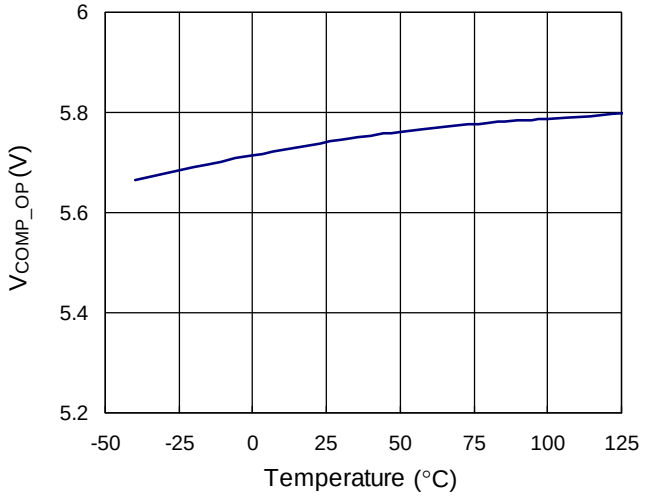
f_{BS_MIN} vs. Temperature



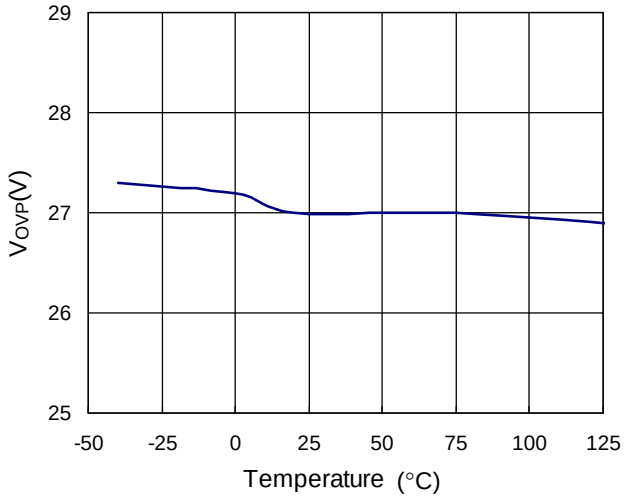
I_{DD_OP} vs. Temperature



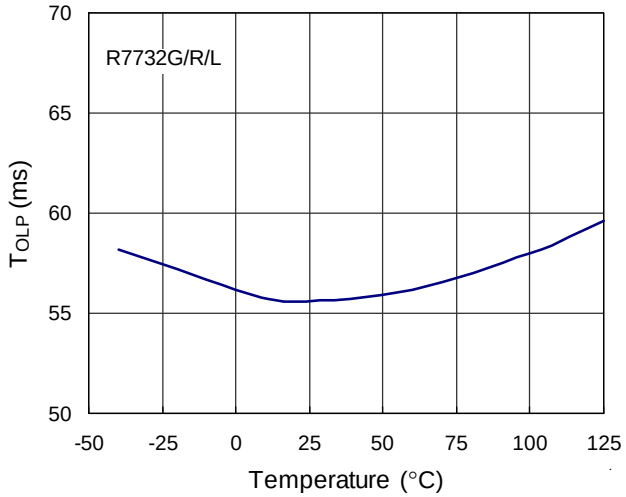
V_{COMP_OP} vs. Temperature



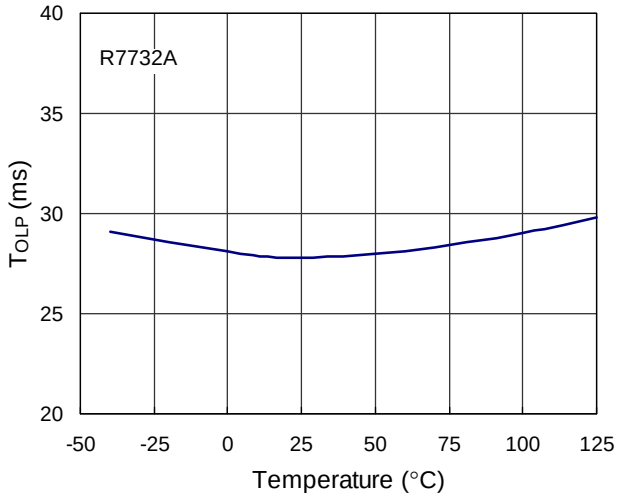
V_{OVP} vs. Temperature



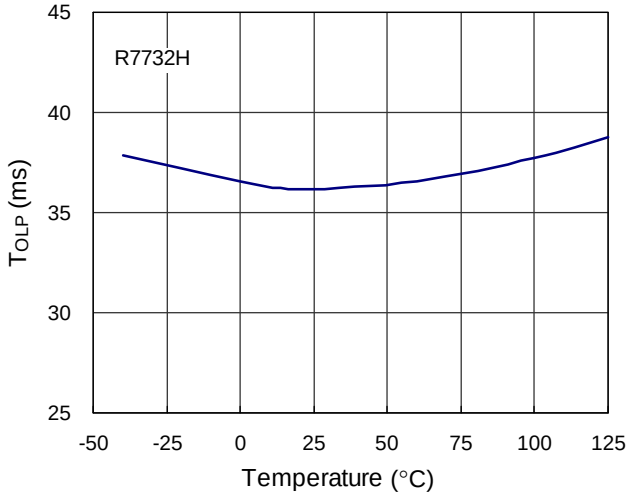
T_{OLP} vs. Temperature



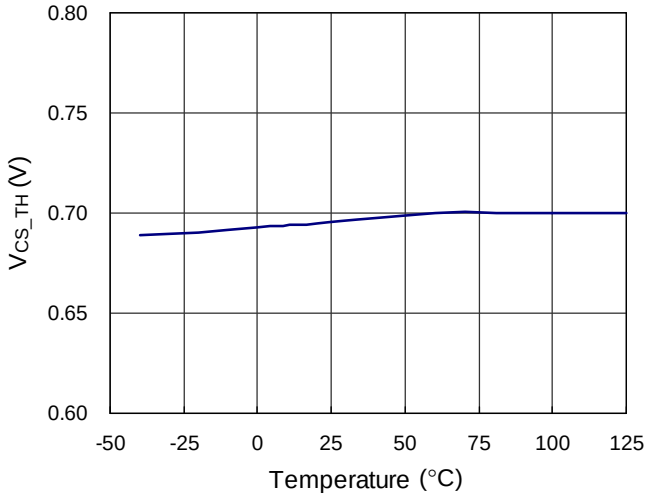
T_{OLP} vs. Temperature



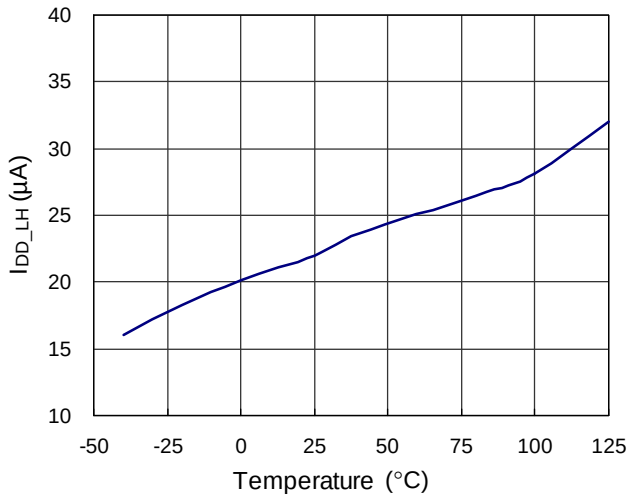
T_{OLP} vs. Temperature



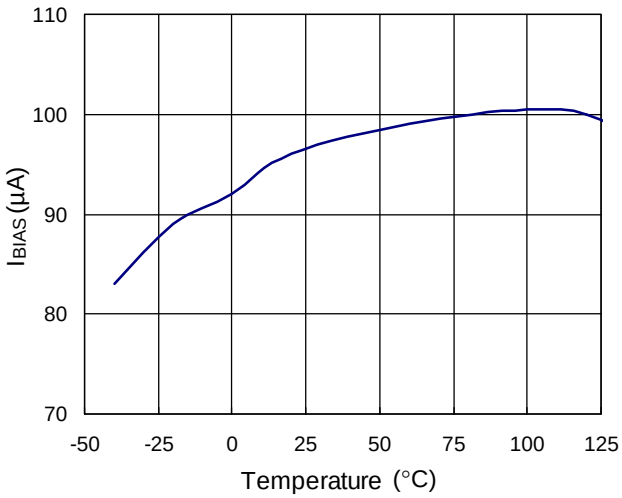
V_{CS_TH} vs. Temperature



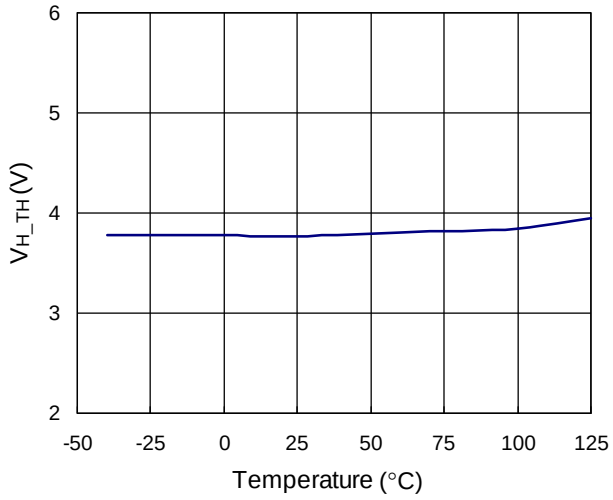
I_{DD_LH} vs. Temperature



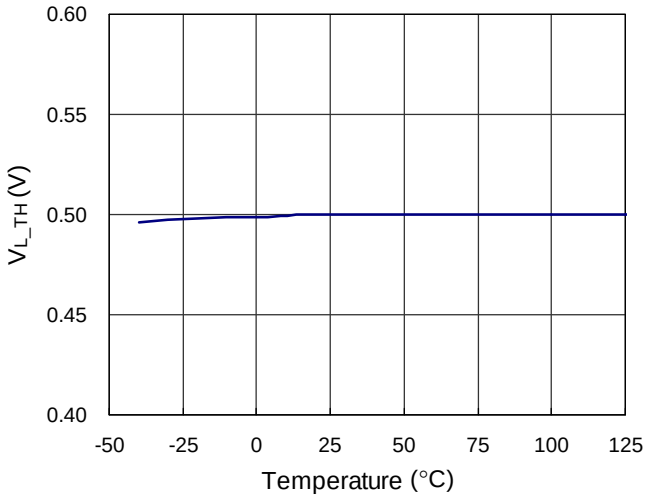
I_{BIAS} vs. Temperature



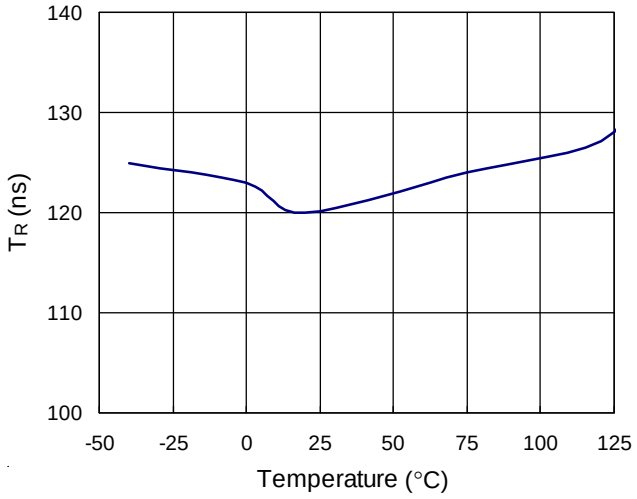
V_{H_TH} vs. Temperature



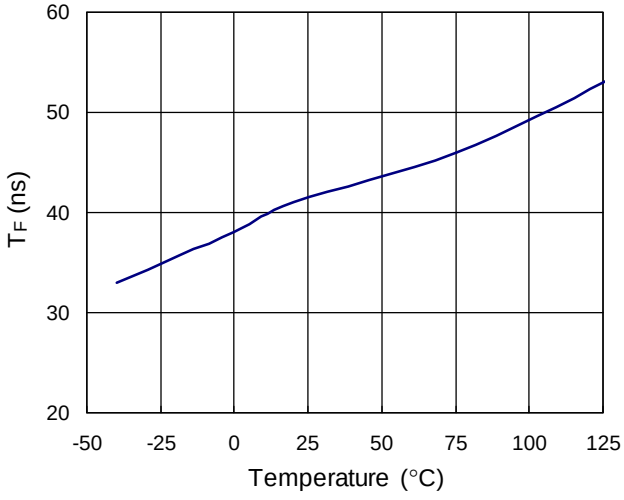
V_{L_TH} vs. Temperature



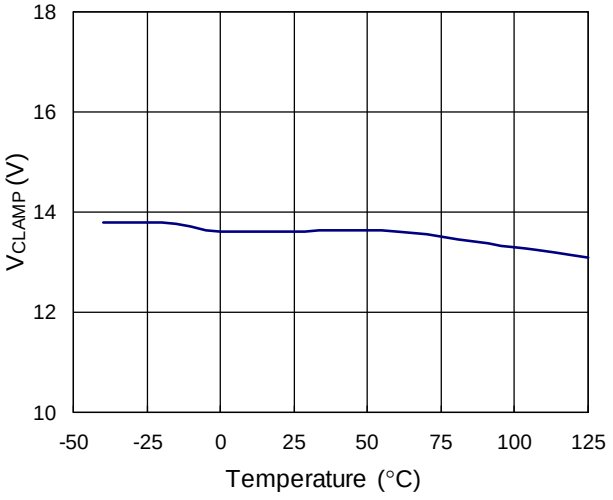
T_R vs. Temperature



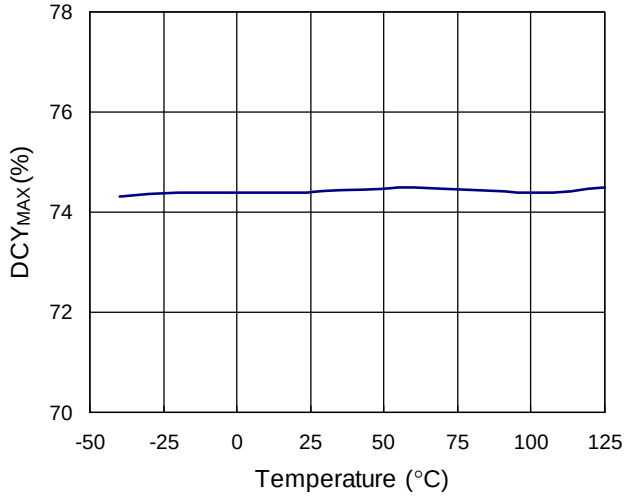
T_F vs. Temperature



V_{CLAMP} vs. Temperature



DCY_{MAX} vs. Temperature



Application Information

- **Burst Switching Green Mode :** During light load, switching loss will dominate the power efficiency calculation. This mode is to cut switching loss. When the output load gets light, feedback signal drops and touches V_{BURL}. PWM signal will be blanked and system ceases to switch. After V_{OUT} drops and feedback signal goes back to V_{BURH}, switching will be resumed.
- **VDD Holdup Mode:** Under light load or load transient moment, feedback signal will drop and touch V_{BURL}. Then PWM signal will be blanked and system ceases to switch. V_{DD} could drop down to turn off threshold voltage. To avoid this, when V_{DD} drops to a setting threshold (Typ. = 10V), the hysteresis comparator will bypass PWM and burst mode loop and forces switching at a very low level to supply energy to VDD pin. VDD holdup mode was also improved to hold up V_{DD} by less switching cycles. This mode is very useful in reducing start-up resistor loss while still get start-up time in spec.

It's not likely for V_{DD} to touch UVLO turn off threshold during any light load condition. This will also makes bias winding design and transient design easier.

Furthermore, VDD holdup mode is only designed to prevent V_{DD} from touching turn off threshold voltage under light load or load transient moment. Relative to burst mode, switching loss will increase on the system at VDD holdup mode, so it is highly recommended that the system should avoid operating at this mode during light load or no load condition, normally.

Start-up Circuit

To minimize power loss, it's recommended that the start-up current is from bleeding resistor. It's not only good for power saving but also could reset latch mode protection quickly. Figure 1 shows I_{DD_Avg} vs. $R_{Bleeding}$ curve. User can apply this curve to design the adequate bleeding resistor.

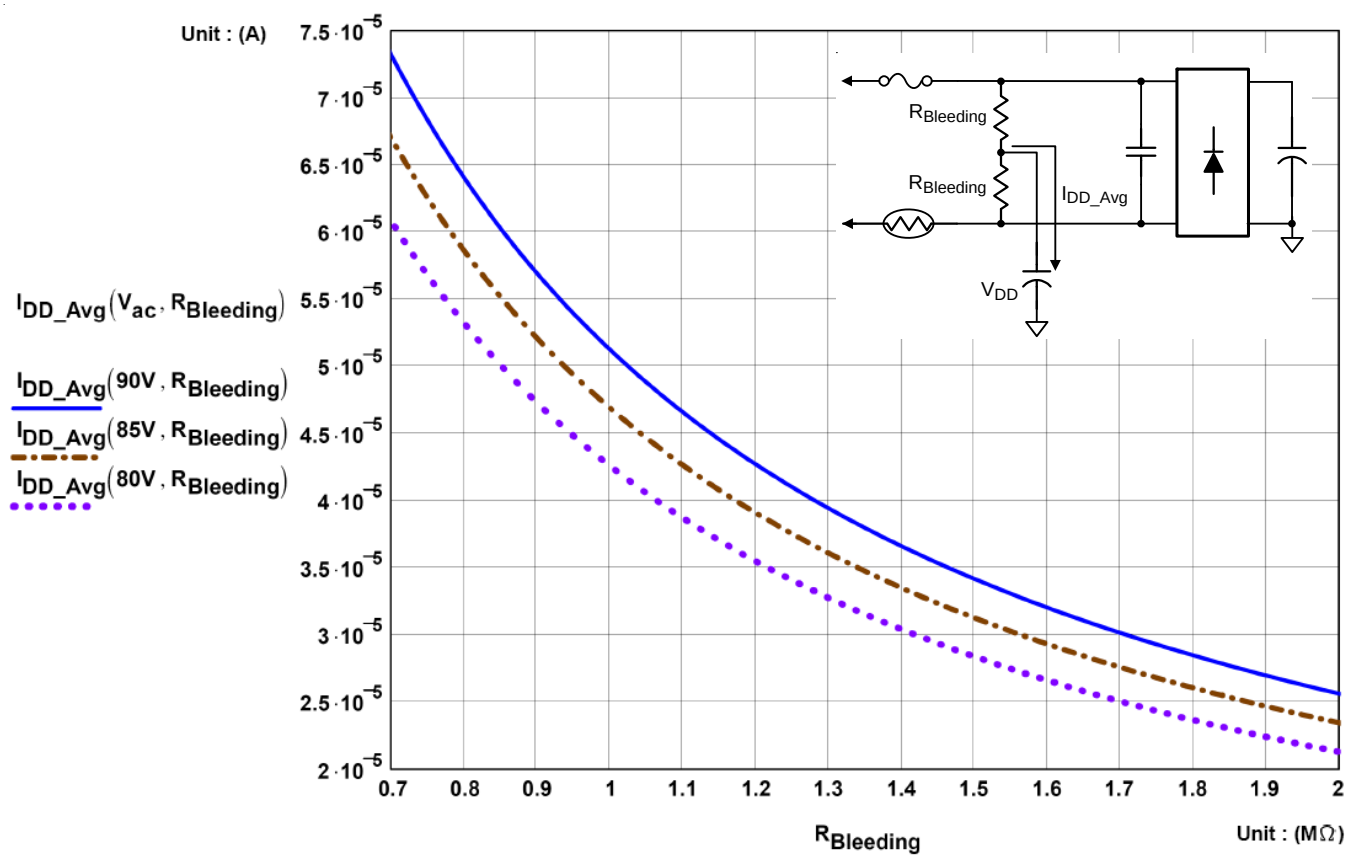


Figure 1. I_{DD_Avg} vs. $R_{Bleeding}$ Curve

Gate Driver

A totem pole gate driver is fine tuned to meet both EMI and efficiency requirement in low power application. An internal pull low circuit is activated after pretty low V_{DD} to prevent external MOSFET from accidentally turning on during UVLO.

Oscillator

To guarantee precise frequency, it's trimmed to 5% tolerance. It also generates slope compensation saw-tooth, 75% maximum duty cycle pulse and overload protection slope. It can typically operate at built-in 65kHz center frequency and features frequency jittering function. Its jittering depth is 6% with about 4ms envelope frequency at 65kHz.

Tight Current Limit Tolerance

Since R7732 is the successor of R7731A, its current limit setting is completely the same as R7731A. Generally, the saw current limit applied to low cost flyback controller because of simple design. However, saw current limit is hard to test in mass production. Therefore, it's generally "guaranteed by design". The variation of process and package will make its tolerance wider. It will lead to 20% to 30% variation when doing OLP test at certain line voltage. This will cause yield loss in power supply mass production. Through well foundry control, design and test / trim mode in final test, R7732 current limit tolerance is tight enough to make design easier.

PRO Pin Application

R7732 features a PRO pin, as shown in Figure 2, and it can be applied for external arbitrary OVP or OTP (ex: Figure 3 to Figure 6).

If the voltage of PRO pin is greater than pull-low threshold V_{L_TH}, the controller is enabled and switching will occur. If the voltage of PRO pin falls below pull-low threshold or rises to pull-high threshold V_{H_TH}, the controller will be shut down and cease to switch after deglitch delay.

PRO pin is built in 1.5V internally, so leave PRO pin open if you don't need this function. If designer needs to apply a bypass capacitor on PRO pin, it should not be more than 1nF. The internal bias current of PRO pin is 100µA(Typ.). R7732 has internal OVP. For arbitrary OVP or OTP applications which behave as auto recovery or latch, it can get these by PRO pin. For PRO pin pulling high function applications, the voltage of PRO pin must rise above V_{H_TH} (The supply current of PRO pin must be greater than 1.2mA and be limited below 5mA.). When IC enters latch mode, the IC maximum operating current is 40µA (100°C), and it will be release until V_{DD} is fallen to V_{TH_OFF}.

PRO pin is guaranteed that below: If the voltage of PRO pin reaches 4.1V or falls below 0.47V, the system will be protected.

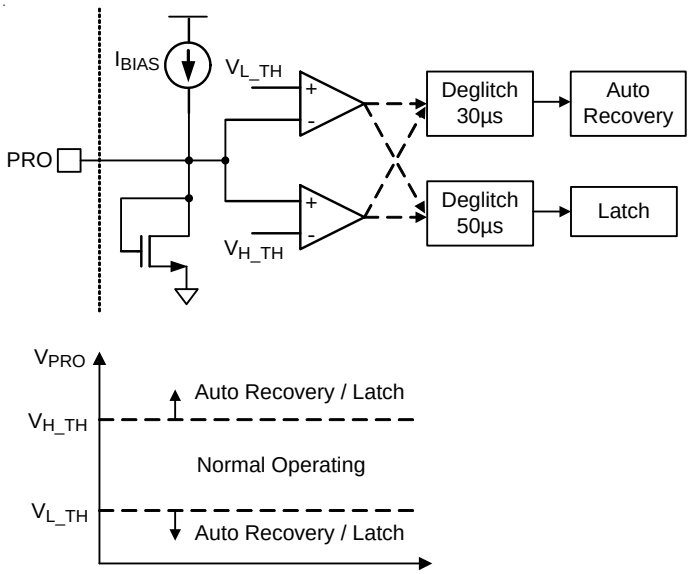
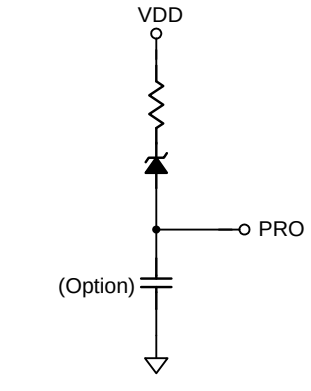


Figure 2. PRO Pin Diagram



V_{DD} OVP : $V_{DD} > V_R + V_Z + 3.8V$

Figure 3. For VDD OVP Only

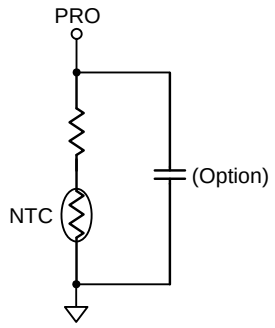


Figure 4. For OTP Only

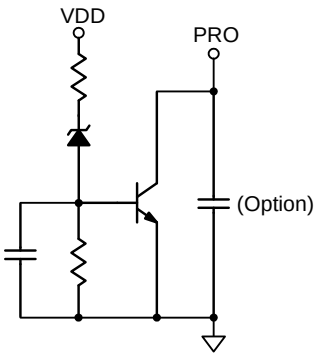


Figure 5. For VDD OVP

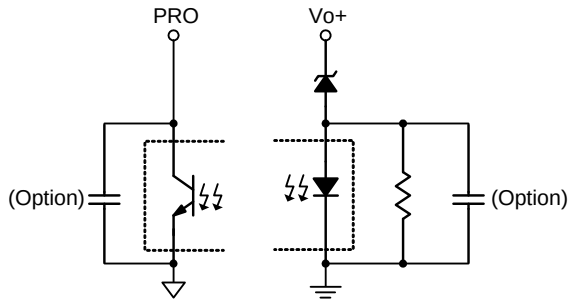


Figure 6. For V_{OUT} OVP

Protection

R7732 provide fruitful protection functions that intend to protect system from being damaged. All the protection functions can be listed as below:

- **Cycle-by-Cycle Current Limit:** This is a basic but very useful function and it can be implemented easily in current mode controller.
- **Over Load Protection:** Long time cycle-by-cycle current limit will lead to system thermal stress. To further protect system, system will be shut down after 56ms (R7732A: 28ms; R7732H: 36ms).

Through our proprietary prolong turn off period during hiccup(R7732A: latch), the power loss and thermal during OLP will be averaged to an acceptable level over the ON/OFF cycle of the IC. This will last until fault is removed.

- **Brownout Protection:** During heavy load, this will trigger 56ms(R7732A: 28ms; R7732H: 36ms) protection and shut down the system. If it is in light load condition, system will be shut down after V_{DD} is running low and triggers UVLO.
- **CS Pin Open Protection:** When CS pin is opened, the system will be shut down after couples of cycle. It could pass CS pin open test easier.
- **Over Voltage Protection:** Output voltage can be roughly sensed by VDD pin. If the sensed voltage reaches 27V threshold, system will be shut down and hiccup after 20μs deglitch delay for R7732G/R/H or latch after 70μs deglitch delay for R7732L/A. This will last until fault is removed.
- **Feedback Open and Opto-Coupler Short:** This will trigger OVP or OLP. It depends on which one occurs first.
- **Secondary Rectifier Short Protection:** As shown in Figure 7. The current spike during secondary rectifier short test is extremely high because of the saturated main transformer. Meanwhile, the transformer acts like a leakage inductance. During high line, the current in power MOSFET is sometimes too high to wait for OLP delay time. To offer better and easier protection design, R7732 shut down the controller after couples of cycles before fuse is blown up.

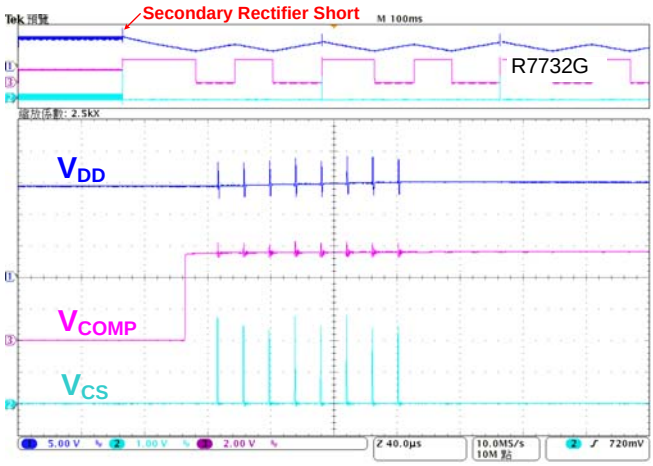


Figure 7. Secondary Rectifier Short Protection

Negative Voltage Spike on Each Pin

Negative voltage (< -0.3V) on each pin will cause substrate injection. It leads to controller damage or circuit false trigger. Generally, it happens at CS pin due to negative spike because of improper layout or inductive current sense resistor. Therefore, it is highly recommended to add a R-C filter to avoid CS pin damage, as shown in Figure 8. Proper layout and careful circuit design should be done to guarantee yield rate in mass production.

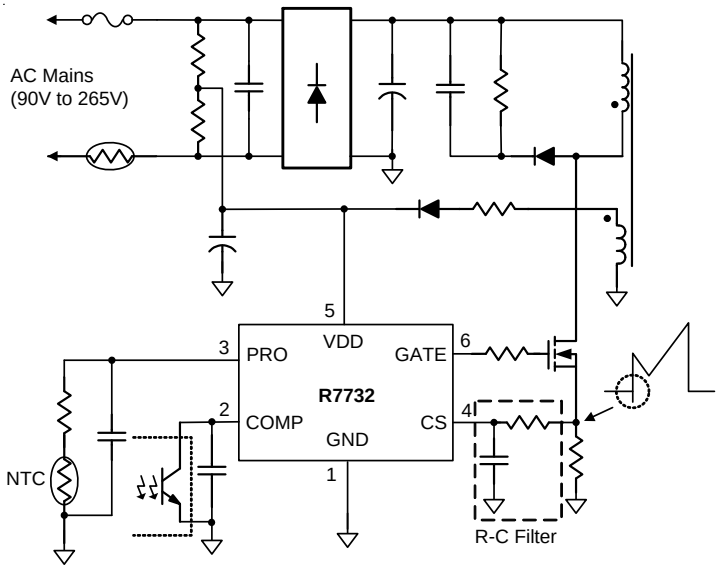


Figure 8. R-C Filter on CS Pin

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-23-6 packages, the thermal resistance, θ_{JA}, is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (250°C/W) = 0.4W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

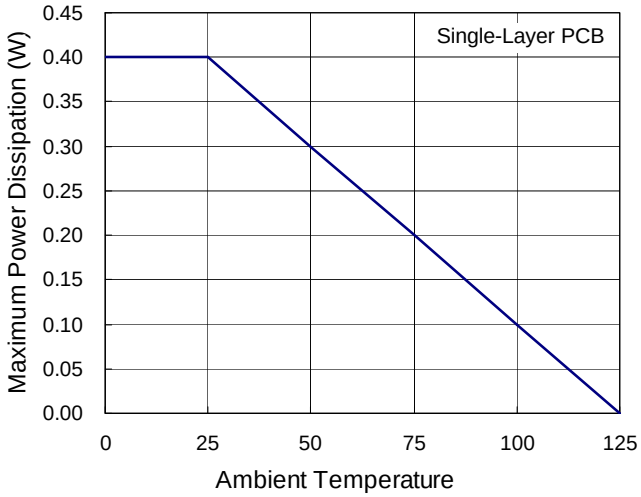


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when you want to design PCB layout for switching power supply:

- The current path (1) from bulk capacitor, transformer, MOSFET, Rcs return to bulk capacitor is a huge high frequency current loop. It must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially.
- The path (2) from RCD snubber circuit to MOSFET is also a high switching loop, too. Keep it as small as possible.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of bulk capacitor (a), MOSFET (b), auxiliary winding (c) and IC control circuit (d). Finally, connect them together on bulk capacitor ground (a). The areas of these ground traces should be kept large.

- Placing bypass capacitor for abating noise on IC is highly recommended. The bypass capacitor should be placed as close to controller as possible.
- In order to minimize reflected trace inductance and EMI, it is minimized the area of the loop connecting the secondary winding, the output diode, and the output filter capacitor. In addition, apply sufficient copper area at the anode and cathode terminal of the diode for heatsinking. Apply a larger area at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.

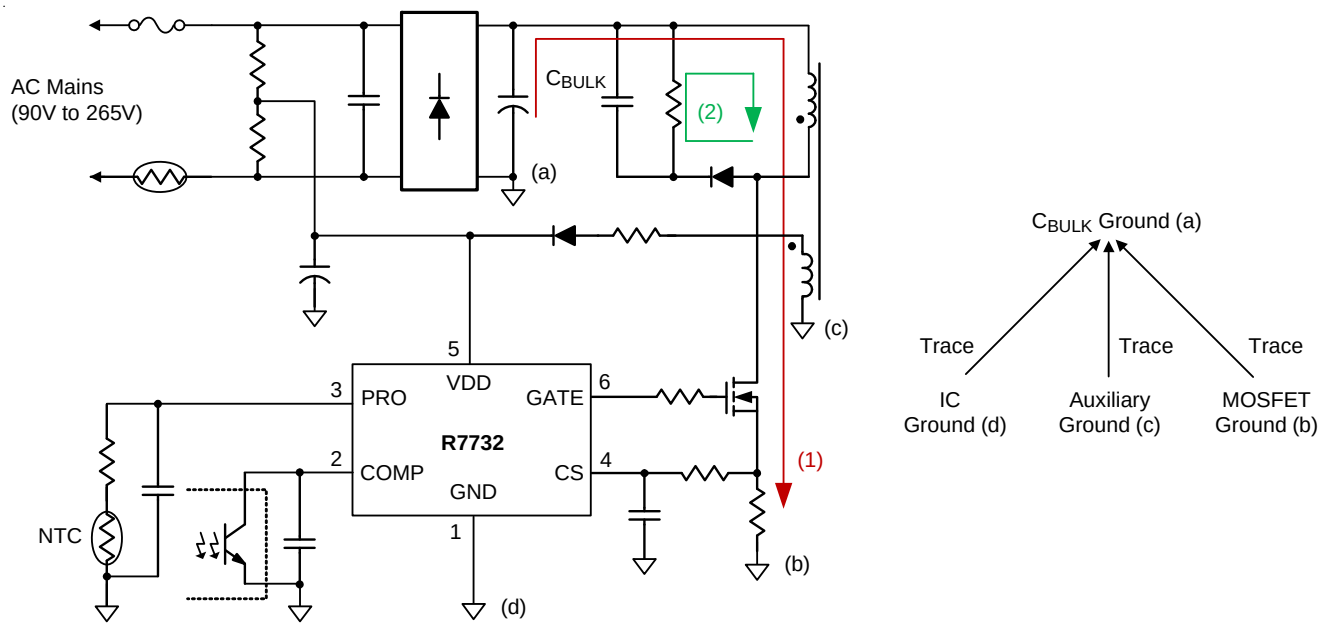
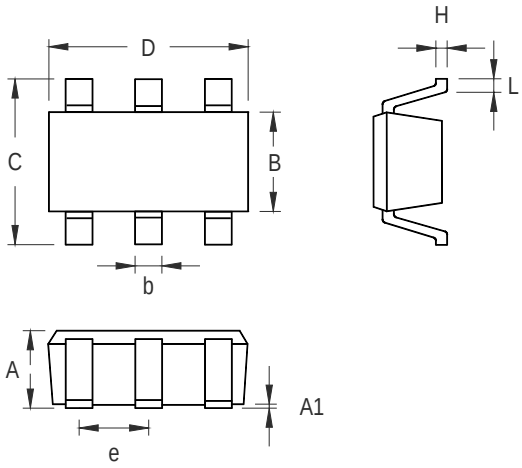


Figure 10. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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