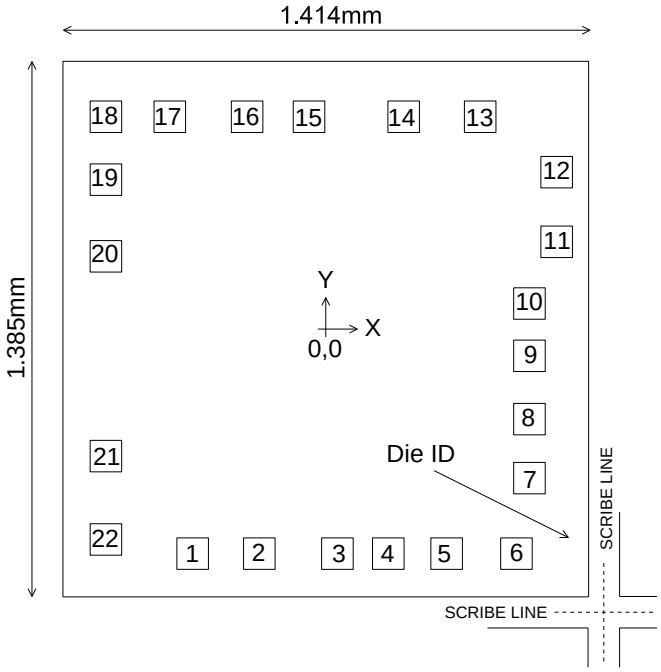
DIE SPECIFICATIONS

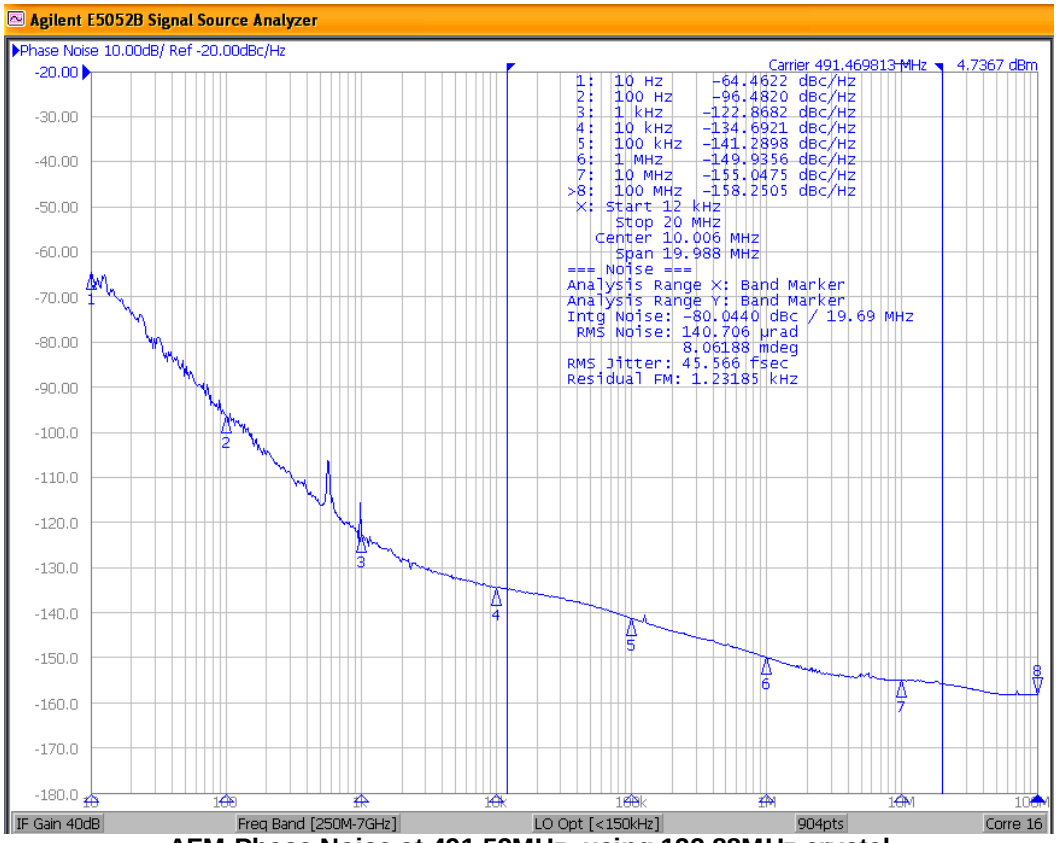


Chip size, active area	1.414mm x 1.385mm
Chip thickness	200 ± 20µm
PAD size	80µm x 80µm
Scribe Line Dimension	X = 80µm Y = 80µm
Chip Base	GND level
Die ID: PL560-08DC PL565-08DC	 C561A 3222222 C561A 7777722

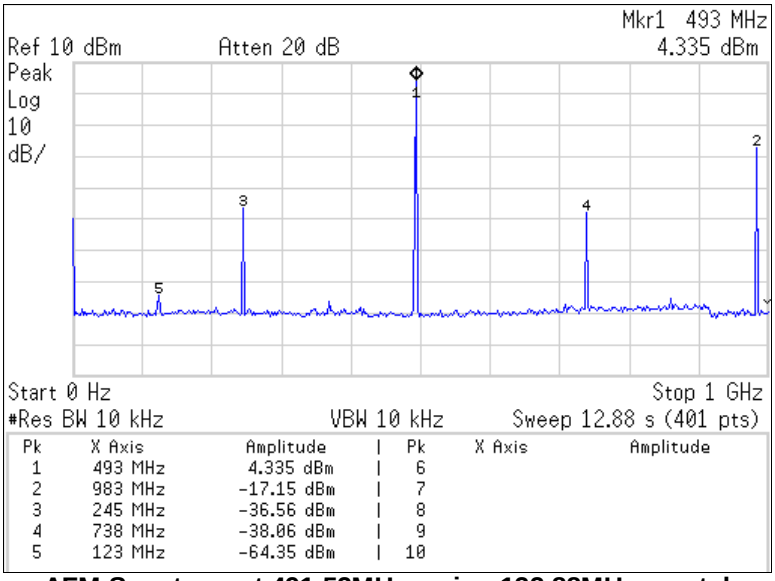
PAD/PIN ASSIGNMENT AND DESCRIPTION (The X/Y coordinates indicate pad centers)

Name	Pad Assignment*			QFN Pin #	Type	Description
	Pad #	X (µm)	Y (µm)			
L4X	1	-352	-557	7	I	External inductor connection
VDDOSC	2	-183	-557	8	P	VDD connection
GNDANA	3	+15	-557	9	P	GND connection
GNDANA	4	+144	-557		P	GND connection
GNDBUF	5	+292	-557		P	GND connection
GNDBUF	6	+469	-557		P	GND connection
GNDBUF	7	+502	-365		P	GND connection
PECLB	8	+502	-215	10	O	LVPECL complementary output
PECL	9	+502	-54	11	O	LVPECL output
VDDBUF	10	+502	+79	12	P	VDD connection
VDDBUF	11	+571	+236		P	VDD connection
VDDANA	12	+571	+413	13	P	VDD connection
N.C.	13	+377	+554	-		
OESEL	14	+183	+554	14	I	OE style selection pin
VDDOSC	15	-57	+554	15	P	VDD connection
L2X	16	-214	+554	16	I	External inductor connection
OSCOFFSEL	17	-410	+554	1	I	Oscillator Off selection pin
GNDOSC	18	-572	+554	2	P	GND connection
VCON	19	-572	+394	3	I	Control voltage input
XIN	20	-572	+199	4	I	Crystal Input pad
XOUT	21	-572	-309	5	O	Crystal Output pad
OE	22	-572	-521	6	I	Output Enable input

*** Note: Pad coordinates referenced to the center of the die.**



AFM Phase Noise at 491.52MHz, using 122.88MHz crystal



AFM Spectrum at 491.52MHz, using 122.88MHz crystal

The analog frequency multiplication preserves the low phase noise of the quartz crystal oscillator while keeping unwanted sub harmonics from the multiplication at very low levels. Sub harmonics appear only at large distance from the carrier, far outside the loop bandwidth of a PLL that uses the AFM signal to multiply up further to a multiple GHz network clock. This means the impact of the sub harmonics on the application is negligible.

PHASE NOISE PERFORMANCE

Part Number	Input Freq. Range (MHz)	Output Freq. Range (MHz)	Phase Noise at Frequency Offset From Carrier (dBc/Hz)								Phase Jitter 12KHz ~ 20MHz (ps)
			Carrier Freq. (MHz)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz	
PL560-08	62.5 - 150	250 - 600	491.52	-64	-96	-123	-135	-141	-150	-155	0.05
PL565-08	150 - 200	600 - 800	622.08	-56	-87	-113	-134	-143	-149	-153	0.04

Phase noise was measured using Agilent E5052B.

SUB-HARMONIC PERFORMANCE

Part Number	Input Frequency (MHz)	Output Frequency (MHz)	Spectral Specifications / Sub-harmonic Content (dBc), Freq. (MHz)						
			Carrier Freq. (Fc)	@ -75% (Fc)	@ -50% (Fc)	@ -25% (Fc)	@ +25% (Fc)	@ +50% (Fc)	@ +75% (Fc)
PL560-08	122.88	491.52	491.52	-60	-40	-70	-70	-40	-70
PL565-08	155.52	622.08	622.08	-60	-40	-40	-40	-40	-50

Note: Spectral specifications were obtained using Agilent E7401A

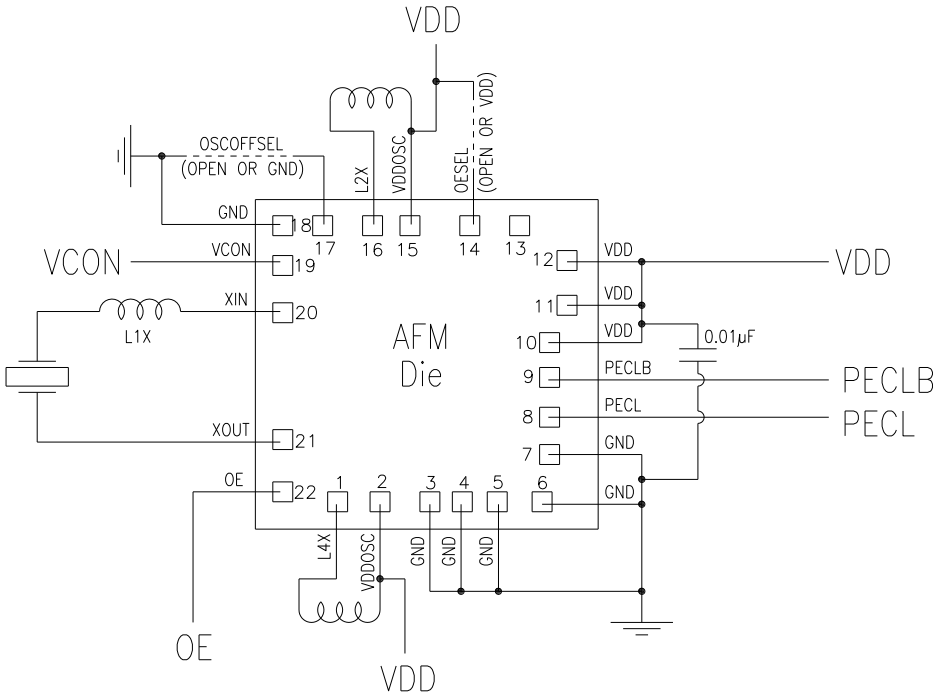
AFM MULTIPLYING TECHNIQUE

The analog frequency multiplication is achieved through a “squaring” operation.

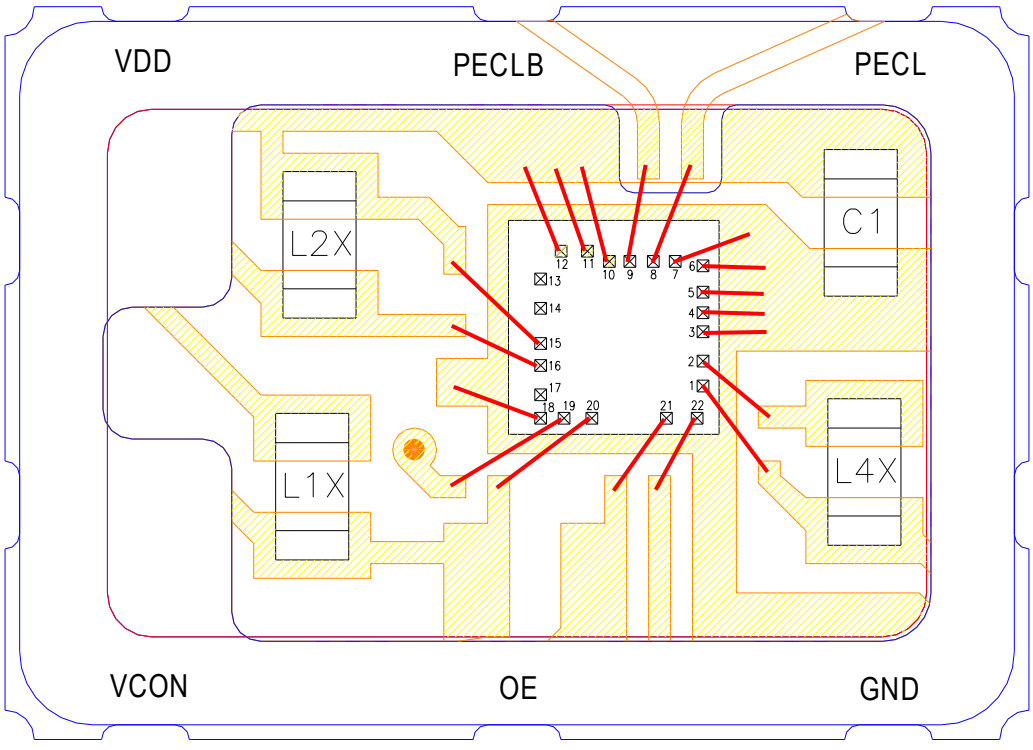
The math is as follows: $SIN^2(x) = 0.5 - 0.5 \times COS(2x)$

A very important property of this processing is that the result is a pure sine wave with double frequency. In theory there are no sub harmonics but in practice the squaring operation is not perfect and a low level of sub harmonics is present anyway. The key is that the resulting sub harmonics are very low and simple filtering with only one inductor per squarer is adequate for excellent performance.

AFM DIE APPLICATION CIRCUIT



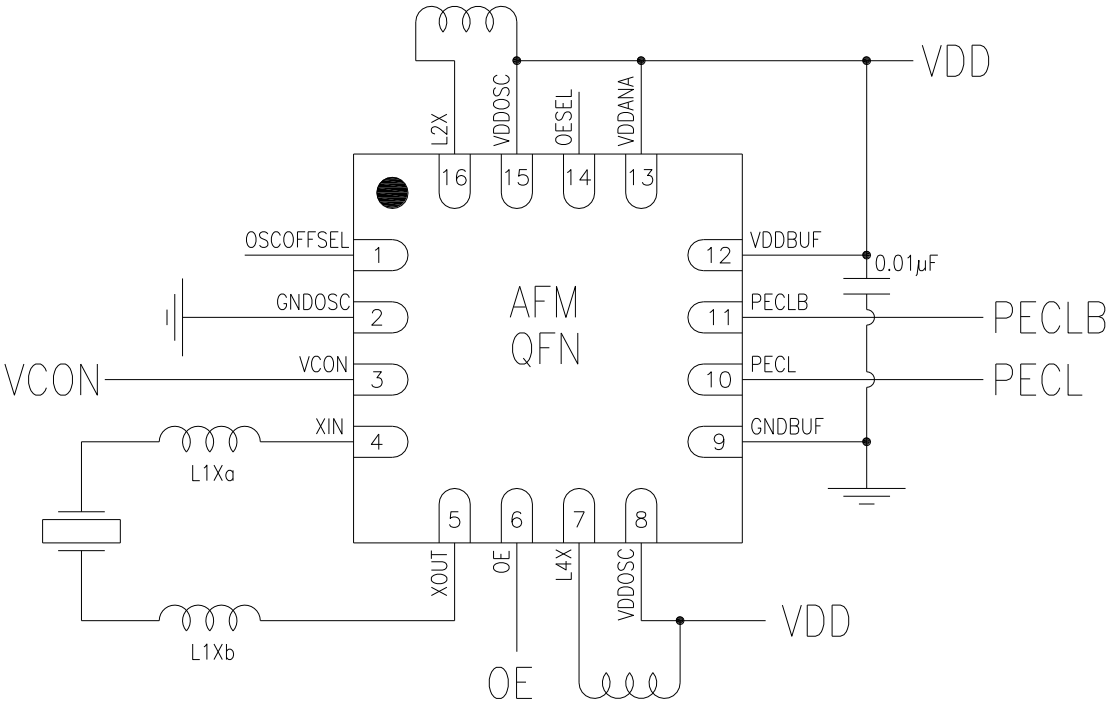
A 7x5mm ceramic substrate was designed to assemble and operate the AFM die at optimum performance:



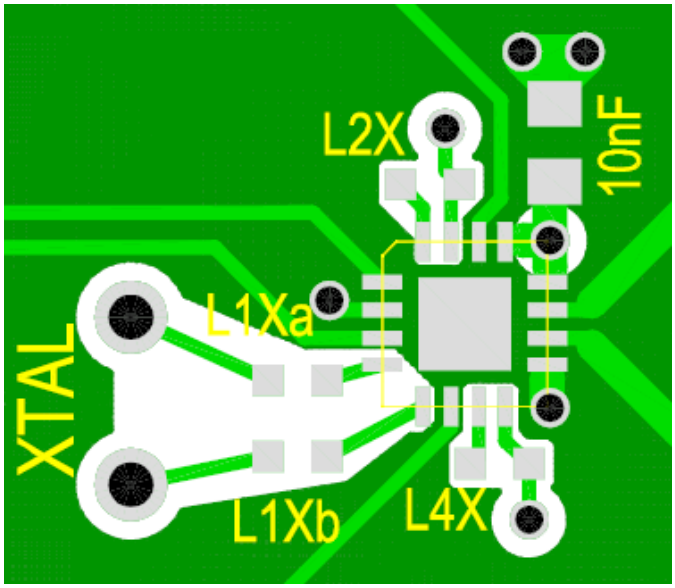
Substrate part number: Kyocera KD-VB0F48

Please see PL560-08DC and PL565-08DC Tuning Assistant documents for passive component values.

AFM QFN PACKAGE APPLICATION CIRCUIT



RECOMMENDED PCB LAYOUT



- Avoid ground planes underneath the crystal and inductor traces to limit parasitic capacitance.
- Add bypass capacitor close to VDDBUF pin.
- Avoid bypass capacitors near VDDOSC pins to lower cross-talk of unwanted frequencies.
- L1X(a,b) can be used to increase the VCXO pulling range. Using a ferrite core inductor limits the oscillation amplitude which can have a positive effect on phase noise.
- L2X and L4X tune the frequency multiplier tank circuits. They need to be wire wound inductors with high Q-factor, preferably >20.
- The large center pad is the “thermal relief” pad and can be connected to ground.

INDUCTOR VALUE OPTIMIZATION

The required inductor values for the best performance depend on the operating frequency, and the board layout or module specifications. The listed values in this datasheet are based on the calculated parasitic values from Micrel's evaluation board design. These inductor values provide the user with a starting point to determine the optimum inductor values. Additional fine-tuning may be required to determine the optimal solution.

The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between L2X / L4X and adjacent VDDOSC pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.

To assist with the inductor value optimization, Micrel has developed AFM "Tuning Assistant" documents. You can download these documents from Micrel's web site (www.micrel.com). The documents consist of tables with recommended inductor values for certain output frequency ranges.

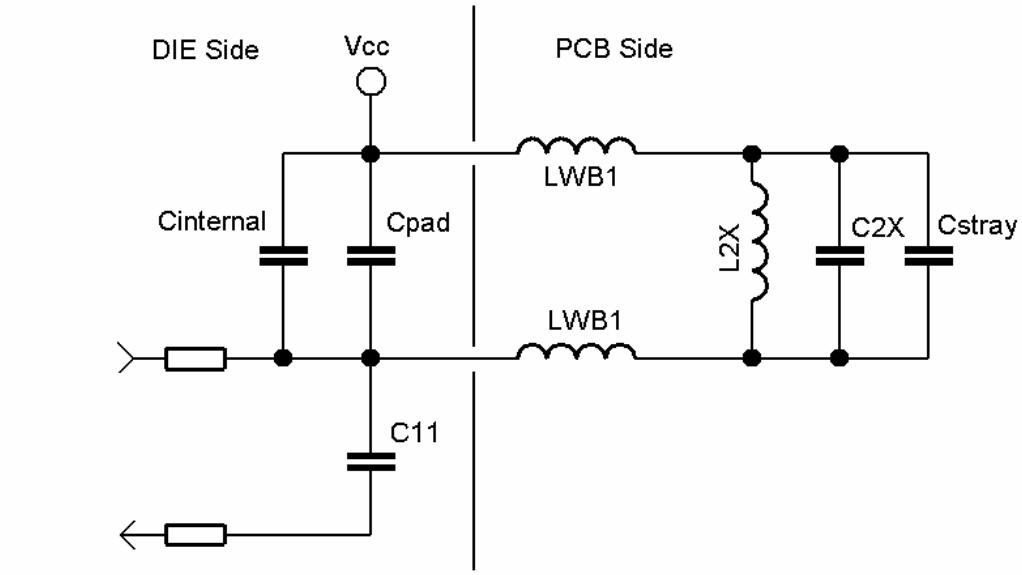


Figure 10: Diagram Representation of the Related System Inductance and Capacitance

DIE SIDE
- Cinternal at L2X = 7.625 pF , at L4X = 6.25 pF
- Cpad = 1.0 pF, Bond pad and its ESD circuitry
- C11 = 0.4 pF, The following amplifier stage

PCB side
- LWB1 = 2 nH, (2 places), Stray inductance
- Cstray = 0.5 pF, Stray capacitance
- L2X (L4X) = 2x or 4x inductor
- C2X (C4X) = range (0.1 to 2.7 pF), Fine tune the tank, if used.

Work out the resonance of this network and you have a good first guess for the required inductor values for optimum performance. Non-linear behavior at large signal amplitudes can shift the tank resonance significantly, especially at the L2X side, to a lower frequency than the calculation suggests. The Tuning Assistant documents are based upon actual lab tests and are corrected for the non-linear behavior.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, DC	V_I	GND-0.5	V_{DD}+0.5	V
Output Voltage, DC	V_O	GND-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature, Industrial	T_{A_I}	-40	+85	°C
Ambient Operating Temperature, Commercial	T_{A_C}	0	+70	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (HBM)			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

VOLTAGE CONTROL SPECIFICATION

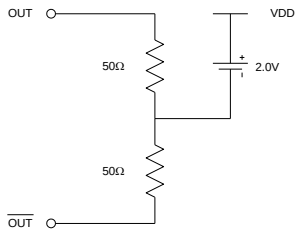
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range*		XTAL C_0 /C_1 <300	200			ppm
CLK Output Pullability*		VCON= 1.65V, ± 1.65V XTAL C_0 /C_1 <300	±100	±120		ppm
Linearity				5	10	%
VCON Input Impedance			130			kΩ
VCON Modulation BW		0V < VCON < 3.3V, -3dB		40		kHz

* Note: The VCXO Tuning Range and Pullability can be controlled with the value for inductor L1X. See Tuning Assistant document for a guide to chose the L1X value based upon crystal frequency and motional parameters.

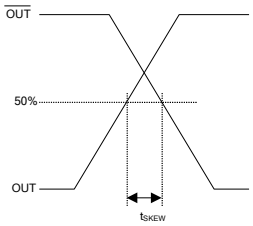
LVPECL ELECTRICAL CHARACTERISTICS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, loaded outputs	I_{DD}	Fout = 622.08MHz		75	80	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@V_{DD}–1.3V, PL560-08	40	50	60	%
		@V_{DD}–1.3V, PL565-08	45	50	55	%
Short Circuit Current				±50		mA
Output High Voltage	V_{OH}	R_L = 50Ω to (V_{DD} – 2V)	V_{DD}-1.025			V
Output Low Voltage	V_{OL}				V_{DD}-1.620	V
Clock Rise Time	t_r	@ 20/80%		0.25	0.45	ns
Clock Fall Time	t_f	@ 80/20%		0.25	0.45	ns

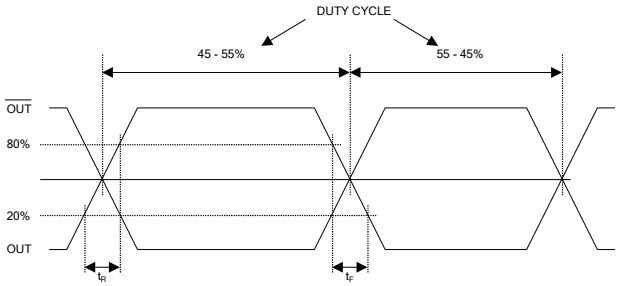
LVPECL Levels Test Circuit



LVPECL Output Skew



LVPECL Transition Time Waveform



OE LOGIC SELECTION

OESEL	OE	Output State
0 (Default)	0 (Default)	Enabled
	1	Tri-state
1	0	Tri-state
	1 (Default)	Enabled

0 (Default): Connect to GND or leave floating to set to "0". Internal pull-down.
1 (Default): Connect to VDD or leave floating to set to "1". Internal pull-up.
0: Connect to GND to set to "0". 1: Connect to VDD to set to "1".

OSCOFFSEL LOGIC SELECTION

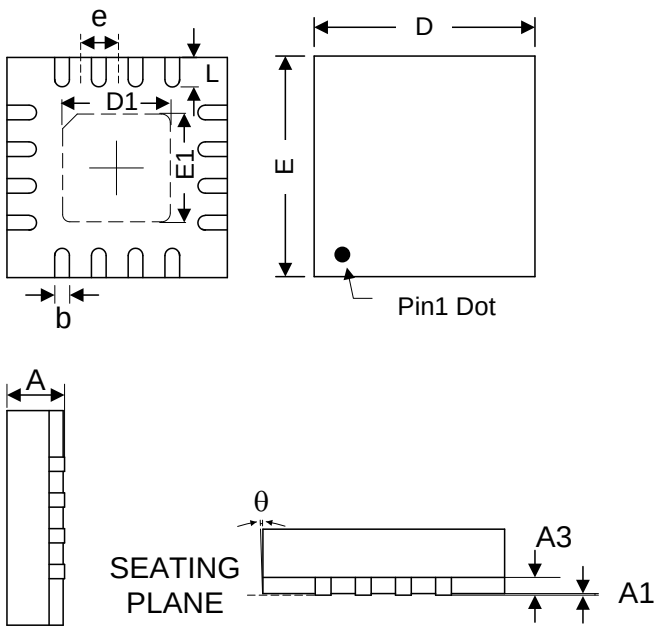
OSCOFFSEL	Functionality description
0	The crystal oscillator shuts down when the output is disabled with OE.
1 (Default)	Only the output will disable with OE. All other circuits, including the crystal oscillator are always running.

1 (Default): Connect to VDD or leave floating to set to "1". Internal pull-up.
0: Connect to GND to set to "0".

PACKAGE INFORMATION

QFN-16L

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20	
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e		0.50BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL56X-08 X X X

PART NUMBER

PACKAGE TYPE
Q= QFN-16L
D= Die

NONE= TUBE
R= TAPE AND REEL

TEMPERATURE
C=COMMERCIAL
I=INDUSTRIAL

Order Number	Marking	Package Option*
PL560/5-08DC	-	Die Only
PL560/5-08QC	P560/5 08(I) LLL	QFN – Tube
PL560/5-08QC-R		QFN – Tape and Reel

Marking Notes : “LLL”, “LLLLL” represents the production lot number