

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, PIC<sup>32</sup> logo, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**MICROCHIP**

# PIC18F8723 FAMILY

## 64/80-Pin, 1-Mbit, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

### Peripheral Highlights:

- 12-Bit, Up to 16-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Two Master Synchronous Serial Port (MSSP) modules supporting 2/3/4-Wire SPI (all four modes) and I<sup>2</sup>C™ Master and Slave modes
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Four Programmable External Interrupts
- Four Input Change Interrupts

### External Memory Interface:

- Address Capability of Up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 8, 12, 16 and 20-Bit Address modes

### Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 15  $\mu$ A Typical
- Sleep Current Down to 0.2  $\mu$ A Typical
- Timer1 Oscillator: 1.8  $\mu$ A, 32 kHz, 2V
- Watchdog Timer: 2.1  $\mu$ A

### Special Microcontroller Features:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- nanoWatt Technology

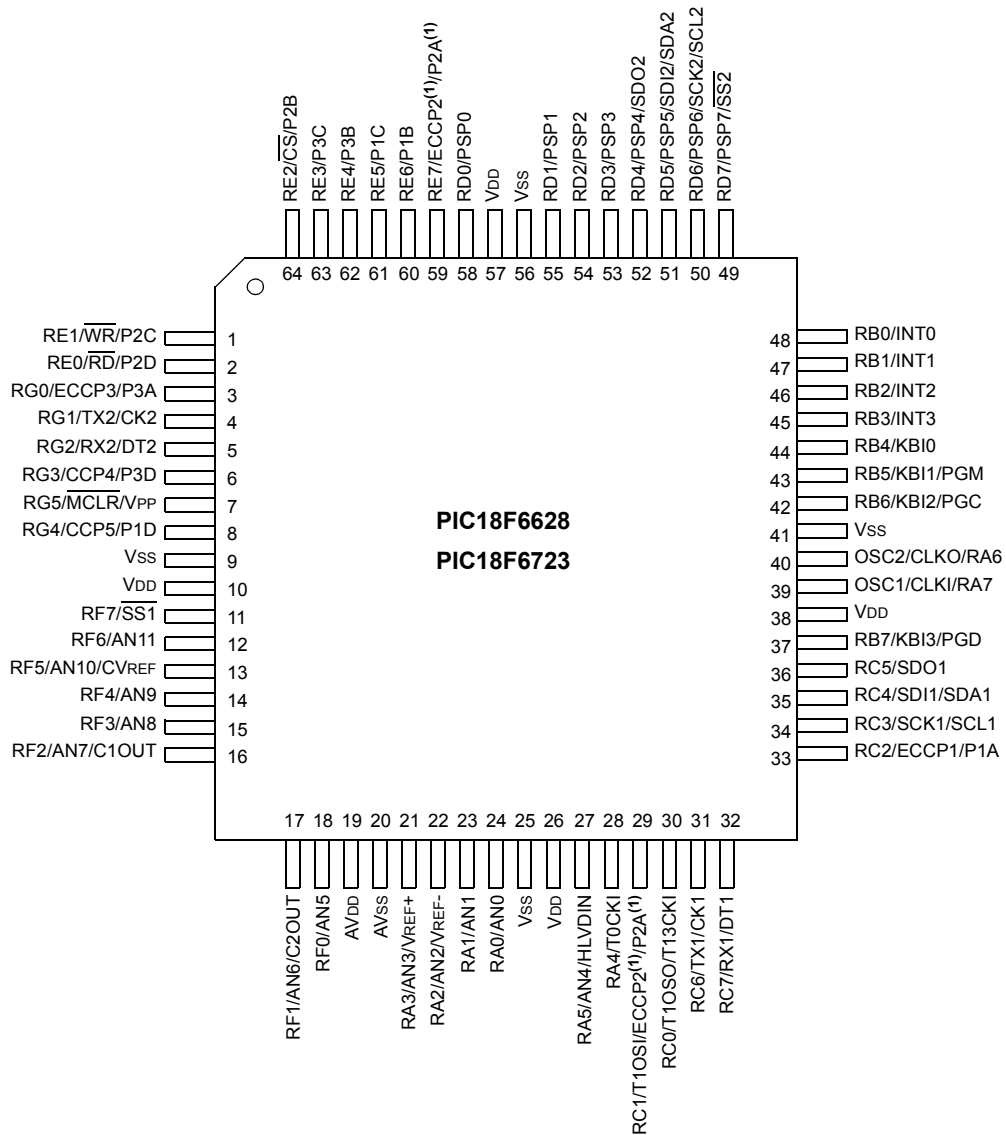
**Note:** This document is supplemented by the "PIC18F8722 Family Data Sheet" (DS39646). See **Section 1.0 "Device Overview"**.

Device	Program Memory		Data Memory		I/O	12-Bit A/D (ch)	CCP/ ECCP (PWM)	MSSP			EUSART	Comparators	Timers 8/16-Bit	External Bus
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I <sup>2</sup> C™					
PIC18F6628	96K	49152	3936	1024	54	12	2/3	2	Y	Y	2	2	2/3	N
PIC18F6723	128K	65536	3936	1024	54	12	2/3	2	Y	Y	2	2	2/3	N
PIC18F8628	96K	49152	3936	1024	70	16	2/3	2	Y	Y	2	2	2/3	Y
PIC18F8723	128K	65536	3936	1024	70	16	2/3	2	Y	Y	2	2	2/3	Y

# PIC18F8723

## Pin Diagrams

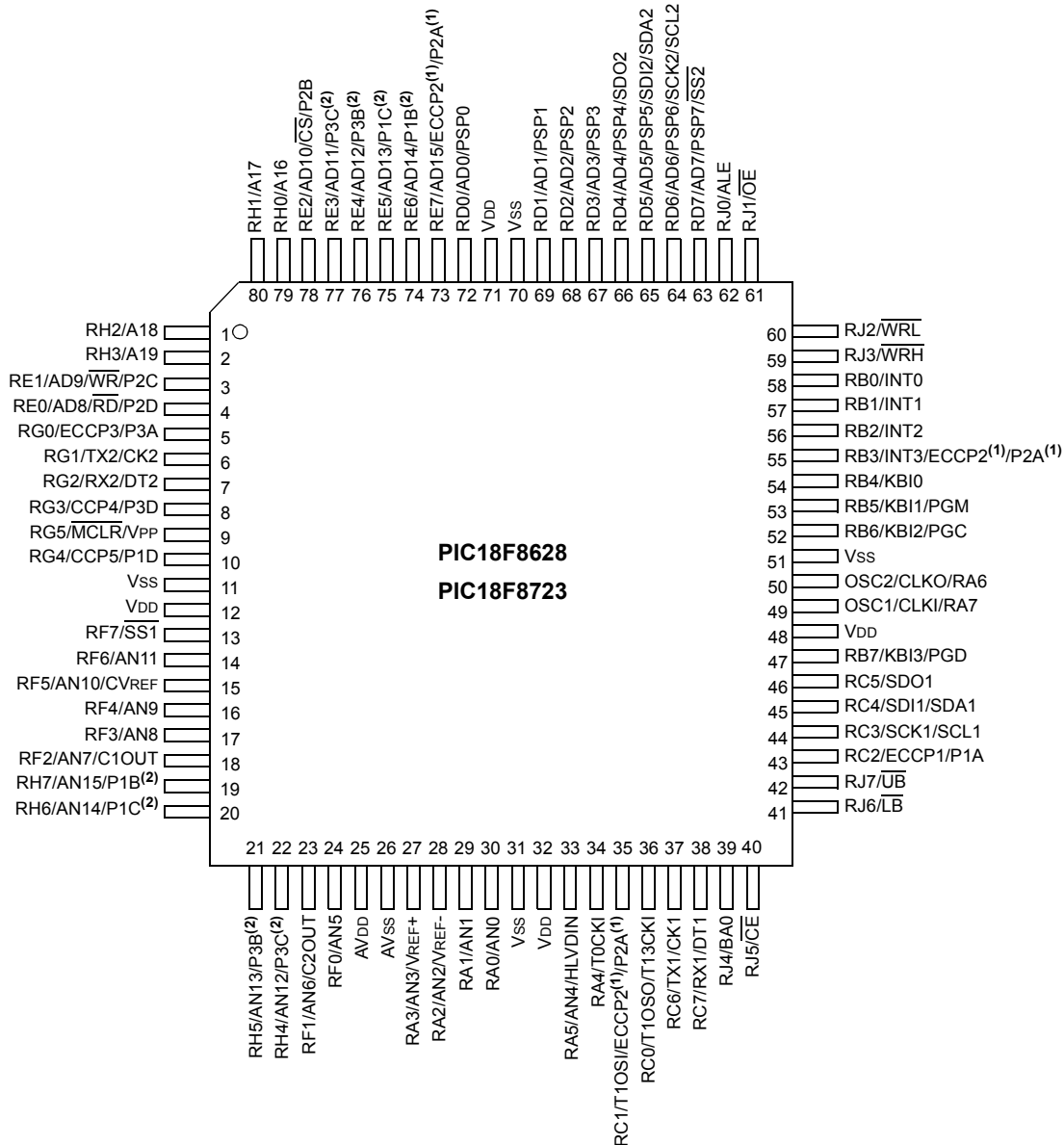
### 64-Pin TQFP



**Note 1:** The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit.

## Pin Diagrams (Continued)

### 80-Pin TQFP



**Note** 1: The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit and Processor mode settings.  
2: P1B, P1C, P3B and P3C pin placement is determined by the ECCPMX Configuration bit.

# PIC18F8723

---

## Table of Contents

1.0	Device Overview .....	9
2.0	12-Bit Analog-to-Digital Converter (A/D) Module .....	31
3.0	Special Features of the CPU .....	41
4.0	Electrical Characteristics .....	43
5.0	Packaging Information.....	49
	Appendix A: Revision History.....	51
	Appendix B: Device Differences.....	51
	Appendix C: Conversion Considerations .....	52
	Appendix D: Migration From Baseline to Enhanced Devices.....	52
	Appendix E: Migration From Mid-Range to Enhanced Devices .....	53
	Appendix F: Migration From High-End to Enhanced Devices .....	53
	Index .....	55
	The Microchip Web Site .....	57
	Customer Change Notification Service .....	57
	Customer Support .....	57
	Reader Response .....	58
	PIC18F8723 family Product Identification System .....	59

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at [docerrors@microchip.com](mailto:docerrors@microchip.com) or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com](http://www.microchip.com) to receive the most current information on all of our products.

# PIC18F8723

---

NOTES:

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6628
- PIC18F6723
- PIC18F8628
- PIC18F8723
- PIC18LF6628
- PIC18LF6723
- PIC18LF8628
- PIC18LF8723

**Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F8722 family devices. For information on the features and specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the "*PIC18F8722 Family Data Sheet*" (DS39646).

The PIC18F8723 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F8723 introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F8723 family implements a 12-bit A/D Converter. A/D Converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

## 1.2 Details on Individual Family Members

Devices in the PIC18F8723 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash program memory (96 Kbytes for PIC18FX628 devices and 128 Kbytes for PIC18FX723).
- A/D channels (12 for PIC18F6628/6723 devices and 16 for PIC18F8628/8723 devices).
- I/O ports (seven bidirectional ports on PIC18F6628/6723 devices and nine bidirectional ports on PIC18F8628/8723 devices).
- External Memory Bus, configurable for 8 and 16-bit operation

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F8723 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F6628), accommodate an operating V<sub>DD</sub> range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF6628), function over an extended V<sub>DD</sub> range of 2.0V to 5.5V.



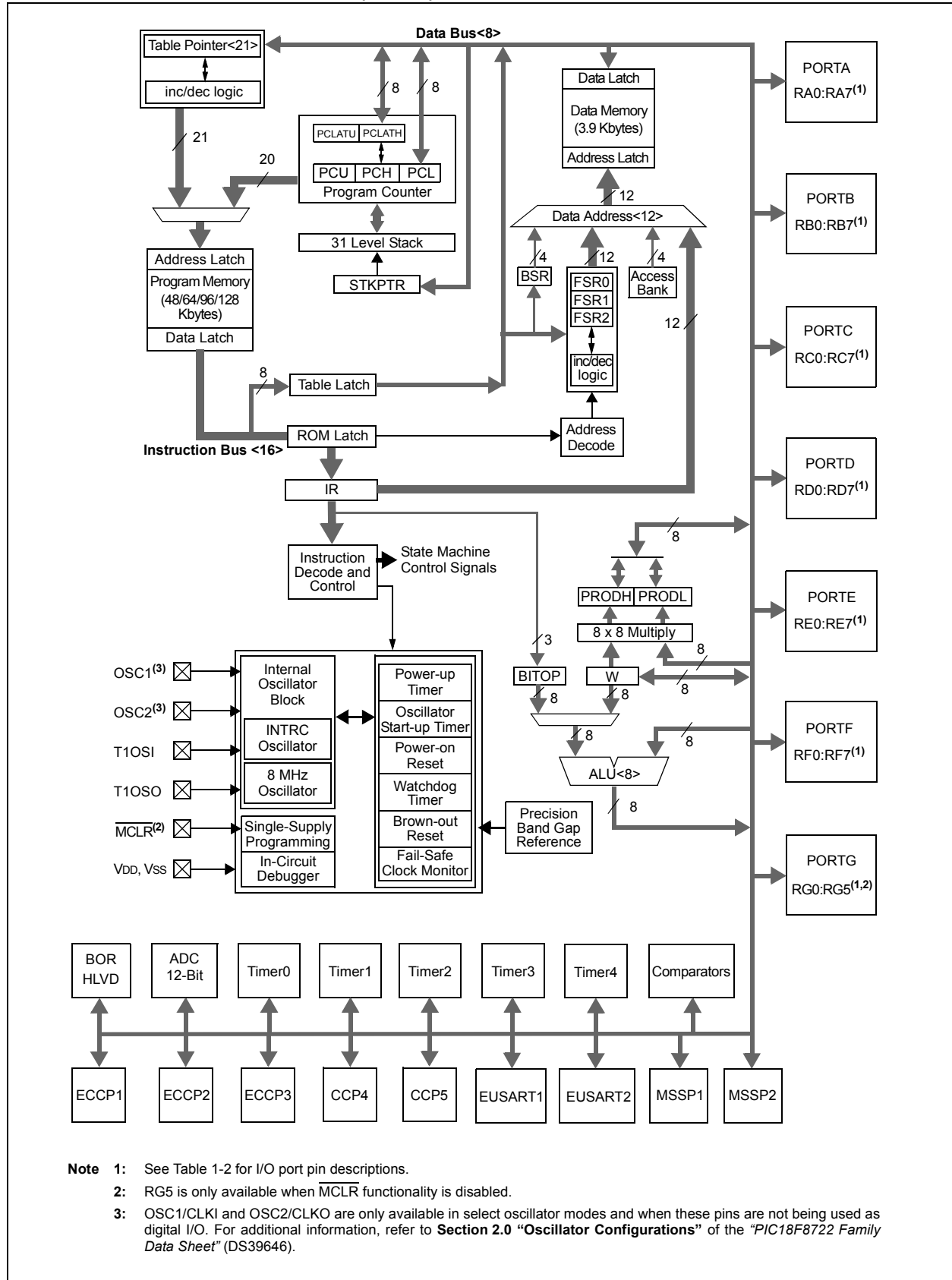
# PIC18F8723 FAMILY

**TABLE 1-1: DEVICE FEATURES**

Features	PIC18F6628	PIC18F6723	PIC18F8628	PIC18F8723
Operating Frequency	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz	DC – 40 MHz
Program Memory (Bytes)	96K	128K	96K	128K
Program Memory (Instructions)	49152	65536	49152	65536
Data Memory (Bytes)	3936	3936	3936	3936
Data EEPROM Memory (Bytes)	1024	1024	1024	1024
Interrupt Sources	28	28	29	29
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Timers	5	5	5	5
Capture/Compare/PWM Modules	2	2	2	2
Enhanced Capture/Compare/PWM Modules	3	3	3	3
Enhanced USART	2	2	2	2
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Parallel Communications (PSP)	Yes	Yes	Yes	Yes
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	16 Input Channels	16 Input Channels
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable High/Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled	75 Instructions; 83 with Extended Instruction Set Enabled
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

# PIC18F8723 FAMILY

**FIGURE 1-1: PIC18F6628/6723 (64-PIN) BLOCK DIAGRAM**



\_\_\_\_\_



# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG5/MCLR/VPP RG5 MCLR  VPP	7	I I  P	ST ST  	Master Clear (input) or programming voltage (input). Digital input. Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input.
OSC1/CLKI/RA7 OSC1  CLKI  RA7	39	I  I  I/O	ST  CMOS  TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2  CLKO  RA6	40	O  O  I/O	—  —  TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	24	I/O I	TTL Analog	PORTA is a bidirectional I/O port.
RA0 AN0				Digital I/O. Analog input 0.
RA1/AN1	23	I/O I	TTL Analog	Digital I/O.
RA1 AN1				Analog input 1.
RA2/AN2/VREF-	22	I/O I I	TTL Analog Analog	Digital I/O.
RA2 AN2				Analog input 2.
VREF-				A/D reference voltage (low) input.
RA3/AN3/VREF+	21	I/O I I	TTL Analog Analog	Digital I/O.
RA3 AN3				Analog input 3.
VREF+				A/D reference voltage (high) input.
RA4/T0CKI	28	I/O I	ST ST	Digital I/O.
RA4 T0CKI				Timer0 external clock input.
RA5/AN4/HLVDIN	27	I/O I I	TTL Analog Analog	Digital I/O.
RA5 AN4				Analog input 4.
HLVDIN				High/Low-Voltage Detect input.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0/FLT0	48			PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
FLT0		I	ST	PWM Fault input for ECCPx.
RB1/INT1	47			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
RB2/INT2	46			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
RB3/INT3	45			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
RB4/KBI0	44			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
RB5/KBI1/PGM	43			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	42			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	37			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	30	I/O	ST	PORTC is a bidirectional I/O port.  Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC0		O	—	
T1OSO		I	ST	
T13CKI				
RC1/T1OSI/ECCP2/P2A	29	I/O	ST	Digital I/O. Timer1 oscillator input. Enhanced Capture 2 input/Compare 2 output/ PWM2 output. ECCP2 PWM output A.
RC1		I	CMOS	
T1OSI		I/O	ST	
ECCP2 <sup>(1)</sup>		O	—	
P2A <sup>(1)</sup>				
RC2/ECCP1/P1A	33	I/O	ST	Digital I/O. Enhanced Capture 1 input/Compare 1 output/ PWM1 output. ECCP1 PWM output A.
RC2		I/O	ST	
ECCP1		O	—	
P1A				
RC3/SCK1/SCL1	34	I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC3		I/O	ST	
SCK1		I/O	ST	
SCL1				
RC4/SDI1/SDA1	35	I/O	ST	Digital I/O. SPI data in. I <sup>2</sup> C data I/O.
RC4		I	ST	
SDI1		I/O	ST	
SDA1				
RC5/SDO1	36	I/O	ST	Digital I/O. SPI data out.
RC5		O	—	
SDO1				
RC6/TX1/CK1	31	I/O	ST	Digital I/O. EUSART1 asynchronous transmit. EUSART1 synchronous clock (see related RX1/DT1).
RC6		O	—	
TX1		I/O	ST	
CK1				
RC7/RX1/DT1	32	I/O	ST	Digital I/O. EUSART1 asynchronous receive. EUSART1 synchronous data (see related TX1/CK1).
RC7		I	ST	
RX1		I/O	ST	
DT1				

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/PSP0	58	I/O	ST	PORTD is a bidirectional I/O port.  Digital I/O.
RD0 PSP0			TTL	
RD1/PSP1	55	I/O	ST	Digital I/O.
RD1 PSP1			TTL	
RD2/PSP2	54	I/O	ST	Digital I/O.
RD2 PSP2			TTL	
RD3/PSP3	53	I/O	ST	Digital I/O.
RD3 PSP3			TTL	
RD4/PSP4/SDO2	52	I/O	ST	Digital I/O.
RD4 PSP4		I/O	TTL	
SDO2		O	—	
RD5/PSP5/SDI2/ SDA2	51	I/O	ST	Digital I/O.
RD5 PSP5		I/O	TTL	
SDI2		I	ST	
SDA2		I/O	I <sup>2</sup> C/SMB	
RD6/PSP6/SCK2/ SCL2	50	I/O	ST	Digital I/O.
RD6 PSP6		I/O	TTL	
SCK2		I/O	ST	
SCL2		I/O	I <sup>2</sup> C/SMB	
RD7/PSP7/SS2	49	I/O	ST	Digital I/O.
RD7 PSP7		I/O	TTL	
SS2		I	TTL	

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.



# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE0/ $\overline{\text{RD}}$ /P2D RE0 $\overline{\text{RD}}$ P2D	2	I/O I O	ST TTL —	<p>PORTE is a bidirectional I/O port.</p> <p>Digital I/O. Read control for Parallel Slave Port. ECCP2 PWM output D.</p>
RE1/ $\overline{\text{WR}}$ /P2C RE1 $\overline{\text{WR}}$ P2C	1	I/O I O	ST TTL —	<p>Digital I/O. Write control for Parallel Slave Port. ECCP2 PWM output C.</p>
RE2/ $\overline{\text{CS}}$ /P2B RE2 $\overline{\text{CS}}$ P2B	64	I/O I O	ST TTL —	<p>Digital I/O. Chip select control for Parallel Slave Port. ECCP2 PWM output B.</p>
RE3/P3C RE3 P3C	63	I/O O	ST —	<p>Digital I/O. ECCP3 PWM output C.</p>
RE4/P3B RE4 P3B	62	I/O O	ST —	<p>Digital I/O. ECCP3 PWM output B.</p>
RE5/P1C RE5 P1C	61	I/O O	ST —	<p>Digital I/O. ECCP1 PWM output C.</p>
RE6/P1B RE6 P1B	60	I/O O	ST —	<p>Digital I/O. ECCP1 PWM output B.</p>
RE7/ECCP2/P2A RE7 ECCP2 <sup>(2)</sup>  P2A <sup>(2)</sup>	59	I/O I/O O	ST ST —	<p>Digital I/O. Enhanced Capture 2 input/Compare 2 output/ PWM2 output. ECCP2 PWM output A.</p>

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF0/AN5	18	I/O I	ST Analog	PORTF is a bidirectional I/O port.  Digital I/O. Analog input 5.
RF0				
AN5				
RF1/AN6/C2OUT	17	I/O I O	ST Analog —	Digital I/O. Analog input 6. Comparator 2 output.
RF1				
AN6 C2OUT				
RF2/AN7/C1OUT	16	I/O I O	ST Analog —	Digital I/O. Analog input 7. Comparator 1 output.
RF2				
AN7 C1OUT				
RF3/AN8	15	I/O I	ST Analog	Digital I/O. Analog input 8.
RF3				
AN8				
RF4/AN9	14	I/O I	ST Analog	Digital I/O. Analog input 9.
RF4				
AN9				
RF5/AN10/CVREF	13	I/O I O	ST Analog Analog	Digital I/O. Analog input 10. Comparator reference voltage output.
RF5				
AN10 CVREF				
RF6/AN11	12	I/O I	ST Analog	Digital I/O. Analog input 11.
RF6				
AN11				
RF7/SS1	11	I/O I	ST TTL	Digital I/O. SPI slave select input.
RF7				
SS1				

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/ECCP3/P3A	3			PORTG is a bidirectional I/O port.
RG0		I/O	ST	Digital I/O.
ECCP3		I/O	ST	Enhanced Capture 3 input/Compare 3 output/PWM3 output.
P3A	4	O	—	ECCP3 PWM output A.
RG1/TX2/CK2				
RG1		I/O	ST	Digital I/O.
TX2	5	O	—	EUSART2 asynchronous transmit.
CK2		I/O	ST	EUSART2 synchronous clock (see related RX2/DT2).
RG2/RX2/DT2				
RG2	6	I/O	ST	Digital I/O.
RX2		I	ST	EUSART2 asynchronous receive.
DT2		I/O	ST	EUSART2 synchronous data (see related TX2/CK2).
RG3/CCP4/P3D	6			
RG3		I/O	ST	Digital I/O.
CCP4		I/O	ST	Capture 4 input/Compare 4 output/PWM4 output.
P3D	8	O	—	ECCP3 PWM output D.
RG4/CCP5/P1D				
RG4		I/O	ST	Digital I/O.
CCP5	8	I/O	ST	Capture 5 input/Compare 5 output/PWM5 output.
P1D		O	—	ECCP1 PWM output D.
RG5				See RG5/MCLR/VPP pin.
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	10, 26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™ = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG5/MCLR/VPP RG5 MCLR  VPP	9	I I  P	ST ST  	Master Clear (input) or programming voltage (input). Digital input. Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input.
OSC1/CLKI/RA7 OSC1  CLKI  RA7	49	I  I  I/O	ST  CMOS  TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2  CLKO  RA6	50	O  O  I/O	—  —  TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).  
**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).  
**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).  
**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).  
**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RA0/AN0	30	I/O I	TTL Analog	PORTA is a bidirectional I/O port.
RA0 AN0				Digital I/O. Analog input 0.
RA1/AN1	29	I/O I	TTL Analog	Digital I/O.
RA1 AN1				Analog input 1.
RA2/AN2/VREF-	28	I/O I I	TTL Analog Analog	Digital I/O.
RA2 AN2				Analog input 2.
VREF-				A/D reference voltage (low) input.
RA3/AN3/VREF+	27	I/O I I	TTL Analog Analog	Digital I/O.
RA3 AN3				Analog input 3.
VREF+				A/D reference voltage (high) input.
RA4/T0CKI	34	I/O I	ST ST	Digital I/O.
RA4 T0CKI				Timer0 external clock input.
RA5/AN4/HLVDIN	33	I/O I I	TTL Analog Analog	Digital I/O.
RA5 AN4				Analog input 4.
HLVDIN				High/Low-Voltage Detect input.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
- 2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).
- 3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
- 4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
- 5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0/FLT0	58			PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0		I/O	TTL	Digital I/O.
INT0		I	ST	External interrupt 0.
FLT0		I	ST	PWM Fault input for ECCPx.
RB1/INT1	57			
RB1		I/O	TTL	Digital I/O.
INT1		I	ST	External interrupt 1.
RB2/INT2	56			
RB2		I/O	TTL	Digital I/O.
INT2		I	ST	External interrupt 2.
RB3/INT3/ECCP2/P2A	55			
RB3		I/O	TTL	Digital I/O.
INT3		I	ST	External interrupt 3.
ECCP2 <sup>(1)</sup>		O	—	Enhanced Capture 2 input/Compare 2 output/ PWM2 output.
P2A <sup>(1)</sup>		O	—	ECCP2 PWM output A.
RB4/KBI0	54			
RB4		I/O	TTL	Digital I/O.
KBI0		I	TTL	Interrupt-on-change pin.
RB5/KBI1/PGM	53			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	52			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD	47			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	36			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/ECCP2/P2A	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
ECCP2 <sup>(2)</sup>		I/O	ST	Enhanced Capture 2 input/Compare 2 output/PWM2 output.
P2A <sup>(2)</sup>		O	—	ECCP2 PWM output A.
RC2/ECCP1/P1A	43			
RC2		I/O	ST	Digital I/O.
ECCP1		I/O	ST	Enhanced Capture 1 input/Compare 1 output/PWM1 output.
P1A		O	—	ECCP1 PWM output A.
RC3/SCK1/SCL1	44			
RC3		I/O	ST	Digital I/O.
SCK1		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL1		I/O	ST	Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC4/SDI1/SDA1	45			
RC4		I/O	ST	Digital I/O.
SDI1		I	ST	SPI data in.
SDA1		I/O	ST	I <sup>2</sup> C data I/O.
RC5/SDO1	46			
RC5		I/O	ST	Digital I/O.
SDO1		O	—	SPI data out.
RC6/TX1/CK1	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART1 asynchronous transmit.
CK1		I/O	ST	EUSART1 synchronous clock (see related RX1/DT1).
RC7/RX1/DT1	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART1 asynchronous receive.
DT1		I/O	ST	EUSART1 synchronous data (see related TX1/CK1).

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
- 2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).
- 3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
- 4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
- 5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/AD0/PSP0	72			PORTD is a bidirectional I/O port.
RD0		I/O	ST	Digital I/O.
AD0		I/O	TTL	External memory address/data 0.
PSP0		I/O	TTL	Parallel Slave Port data.
RD1/AD1/PSP1	69			
RD1		I/O	ST	Digital I/O.
AD1		I/O	TTL	External memory address/data 1.
PSP1		I/O	TTL	Parallel Slave Port data.
RD2/AD2/PSP2	68			
RD2		I/O	ST	Digital I/O.
AD2		I/O	TTL	External memory address/data 2.
PSP2		I/O	TTL	Parallel Slave Port data.
RD3/AD3/PSP3	67			
RD3		I/O	ST	Digital I/O.
AD3		I/O	TTL	External memory address/data 3.
PSP3		I/O	TTL	Parallel Slave Port data.
RD4/AD4/PSP4/SDO2	66			
RD4		I/O	ST	Digital I/O.
AD4		I/O	TTL	External memory address/data 4.
PSP4		I/O	TTL	Parallel Slave Port data.
SDO2		O	—	SPI data out.
RD5/AD5/PSP5/SDI2/SDA2	65			
RD5		I/O	ST	Digital I/O.
AD5		I/O	TTL	External memory address/data 5.
PSP5		I/O	TTL	Parallel Slave Port data.
SDI2		I	ST	SPI data in.
SDA2		I/O	I <sup>2</sup> C/SMB	I <sup>2</sup> C™ data I/O.
RD6/AD6/PSP6/SCK2/SCL2	64			
RD6		I/O	ST	Digital I/O.
AD6		I/O	TTL	External memory address/data 6.
PSP6		I/O	TTL	Parallel Slave Port data.
SCK2		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL2		I/O	I <sup>2</sup> C/SMB	Synchronous serial clock input/output for I <sup>2</sup> C mode.
RD7/AD7/PSP7/SS2	63			
RD7		I/O	ST	Digital I/O.
AD7		I/O	TTL	External memory address/data 7.
PSP7		I/O	TTL	Parallel Slave Port data.
SS2		I	TTL	SPI slave select input.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
- 2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).
- 3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
- 4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
- 5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).



# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE0/AD8/ $\overline{\text{RD}}$ /P2D	4	I/O	ST	PORTE is a bidirectional I/O port.  Digital I/O. External memory address/data 8. Read control for Parallel Slave Port. ECCP2 PWM output D.
RE0		I/O	TTL	
AD8		I	TTL	
P2D		O	—	
RE1/AD9/ $\overline{\text{WR}}$ /P2C	3	I/O	ST	Digital I/O. External memory address/data 9. Write control for Parallel Slave Port. ECCP2 PWM output C.
RE1		I/O	TTL	
AD9		I	TTL	
P2C		O	—	
RE2/AD10/ $\overline{\text{CS}}$ /P2B	78	I/O	ST	Digital I/O. External memory address/data 10. Chip select control for Parallel Slave Port. ECCP2 PWM output B.
RE2		I/O	TTL	
AD10		I	TTL	
P2B		O	—	
RE3/AD11/P3C	77	I/O	ST	Digital I/O. External memory address/data 11. ECCP3 PWM output C.
RE3		I/O	TTL	
AD11		O	—	
P3C <sup>(4)</sup>				
RE4/AD12/P3B	76	I/O	ST	Digital I/O. External memory address/data 12. ECCP3 PWM output B.
RE4		I/O	TTL	
AD12		O	—	
P3B <sup>(4)</sup>				
RE5/AD13/P1C	75	I/O	ST	Digital I/O. External memory address/data 13. ECCP1 PWM output C.
RE5		I/O	TTL	
AD13		O	—	
P1C <sup>(4)</sup>				
RE6/AD14/P1B	74	I/O	ST	Digital I/O. External memory address/data 14. ECCP1 PWM output B.
RE6		I/O	TTL	
AD14		O	—	
P1B <sup>(4)</sup>				
RE7/AD15/ECCP2/ P2A	73	I/O	ST	Digital I/O. External memory address/data 15. Enhanced Capture 2 input/Compare 2 output/ PWM2 output. ECCP2 PWM output A.
RE7		I/O	TTL	
AD15		I/O	ST	
ECCP2 <sup>(3)</sup>				
P2A <sup>(3)</sup>		O	—	

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF0/AN5	24	I/O I	ST Analog	PORTF is a bidirectional I/O port.  Digital I/O. Analog input 5.
RF0				
AN5				
RF1/AN6/C2OUT	23	I/O I O	ST Analog —	Digital I/O. Analog input 6. Comparator 2 output.
RF1				
AN6 C2OUT				
RF2/AN7/C1OUT	18	I/O I O	ST Analog —	Digital I/O. Analog input 7. Comparator 1 output.
RF2				
AN7 C1OUT				
RF3/AN8	17	I/O I	ST Analog	Digital I/O. Analog input 8.
RF3				
AN8				
RF4/AN9	16	I/O I	ST Analog	Digital I/O. Analog input 9.
RF4				
AN9				
RF5/AN10/CVREF	15	I/O I O	ST Analog Analog	Digital I/O. Analog input 10. Comparator reference voltage output.
RF5				
AN10 CVREF				
RF6/AN11	14	I/O I	ST Analog	Digital I/O. Analog input 11.
RF6				
AN11				
RF7/SS1	13	I/O I	ST TTL	Digital I/O. SPI slave select input.
RF7				
SS1				

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).  
**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).  
**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).  
**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).  
**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/ECCP3/P3A	5			PORTG is a bidirectional I/O port.
RG0		I/O	ST	Digital I/O.
ECCP3		I/O	ST	Enhanced Capture 3 input/Compare 3 output/PWM3 output.
P3A	6	O	—	ECCP3 PWM output A.
RG1/TX2/CK2				
RG1		I/O	ST	Digital I/O.
TX2		O	—	EUSART2 asynchronous transmit.
CK2	7	I/O	ST	EUSART2 synchronous clock (see related RX2/DT2).
RG2/RX2/DT2				
RG2		I/O	ST	Digital I/O.
RX2		I	ST	EUSART2 asynchronous receive.
DT2	8	I/O	ST	EUSART2 synchronous data (see related TX2/CK2).
RG3/CCP4/P3D				
RG3		I/O	ST	Digital I/O.
CCP4		I/O	ST	Capture 4 input/Compare 4 output/PWM4 output.
P3D	10	O	—	ECCP3 PWM output D.
RG4/CCP5/P1D				
RG4		I/O	ST	Digital I/O.
CCP5		I/O	ST	Capture 5 input/Compare 5 output/PWM5 output.
P1D	10	O	—	ECCP1 PWM output D.
RG5				See RG5/MCLR/VPP pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).
- 2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).
- 3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).
- 4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).
- 5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH0/A16 RH0 A16	79	I/O I/O	ST TTL	PORTH is a bidirectional I/O port.  Digital I/O. External memory address/data 16.
RH1/A17 RH1 A17	80	I/O I/O	ST TTL	Digital I/O. External memory address/data 17.
RH2/A18 RH2 A18	1	I/O I/O	ST TTL	Digital I/O. External memory address/data 18.
RH3/A19 RH3 A19	2	I/O I/O	ST TTL	Digital I/O. External memory address/data 19.
RH4/AN12/P3C RH4 AN12 P3C <sup>(5)</sup>	22	I/O I O	ST Analog —	Digital I/O. Analog input 12. ECCP3 PWM output C.
RH5/AN13/P3B RH5 AN13 P3B <sup>(5)</sup>	21	I/O I O	ST Analog —	Digital I/O. Analog input 13. ECCP3 PWM output B.
RH6/AN14/P1C RH6 AN14 P1C <sup>(5)</sup>	20	I/O I O	ST Analog —	Digital I/O. Analog input 14. ECCP1 PWM output C.
RH7/AN15/P1B RH7 AN15 P1B <sup>(5)</sup>	19	I/O I O	ST Analog —	Digital I/O. Analog input 15. ECCP1 PWM output B.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).  
**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).  
**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).  
**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).  
**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

# PIC18F8723 FAMILY

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RJ0/ALE RJ0 ALE	62	I/O O	ST —	PORTJ is a bidirectional I/O port.  Digital I/O. External memory address latch enable.
RJ1/ $\overline{\text{OE}}$ RJ1 $\overline{\text{OE}}$	61	I/O O	ST —	Digital I/O. External memory output enable.
RJ2/ $\overline{\text{WRL}}$ RJ2 $\overline{\text{WRL}}$	60	I/O O	ST —	Digital I/O. External memory write low control.
RJ3/ $\overline{\text{WRH}}$ RJ3 $\overline{\text{WRH}}$	59	I/O O	ST —	Digital I/O. External memory write high control.
RJ4/BA0 RJ4 BA0	39	I/O O	ST —	Digital I/O. External memory byte address 0 control.
RJ5/ $\overline{\text{CE}}$ RJ4 $\overline{\text{CE}}$	40	I/O O	ST —	Digital I/O External memory chip enable control.
RJ6/ $\overline{\text{LB}}$ RJ6 $\overline{\text{LB}}$	41	I/O O	ST —	Digital I/O. External memory low byte control.
RJ7/ $\overline{\text{UB}}$ RJ7 $\overline{\text{UB}}$	42	I/O O	ST —	Digital I/O. External memory high byte control.
Vss	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVss	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      Analog = Analog input  
I = Input      O = Output  
P = Power      I<sup>2</sup>C™/SMB = I<sup>2</sup>C/SMBus input buffer

- Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).  
**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).  
**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).  
**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).  
**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 12 inputs for the 64-pin devices (PIC18F6628/6723) and 16 for the 80-pin devices (PIC18F8628/8723). This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

### REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7						bit 0	

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)  
 0001 = Channel 1 (AN1)  
 0010 = Channel 2 (AN2)  
 0011 = Channel 3 (AN3)  
 0100 = Channel 4 (AN4)  
 0101 = Channel 5 (AN5)  
 0110 = Channel 6 (AN6)  
 0111 = Channel 7 (AN7)  
 1000 = Channel 8 (AN8)  
 1001 = Channel 9 (AN9)  
 1010 = Channel 10 (AN10)  
 1011 = Channel 11 (AN11)  
 1100 = Channel 12 (AN12)<sup>(1,2)</sup>  
 1101 = Channel 13 (AN13)<sup>(1,2)</sup>  
 1110 = Channel 14 (AN14)<sup>(1,2)</sup>  
 1111 = Channel 15 (AN15)<sup>(1,2)</sup>

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress

0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D Converter module is enabled

0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on PIC18F6628/6723 devices.

**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

# PIC18F8723 FAMILY

## REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6

**Unimplemented:** Read as '0'

bit 5-4

**VCFG1:VCFG0:** Voltage Reference Configuration bits

	A/D VREF+	A/D VREF-
00	AVDD	AVSS
01	External VREF+	AVSS
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0

**PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG<3:0>	AN15 <sup>(1)</sup>	AN14 <sup>(1)</sup>	AN13 <sup>(1)</sup>	AN12 <sup>(1)</sup>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input

D = Digital I/O

**Note 1:** AN15 through AN12 are available only on PIC18F8628/8723 devices.

# PIC18F8723 FAMILY

## REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD<sup>(1)</sup>

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the **SLEEP** instruction to be executed before starting a conversion.



# PIC18F8723 FAMILY

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS), or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

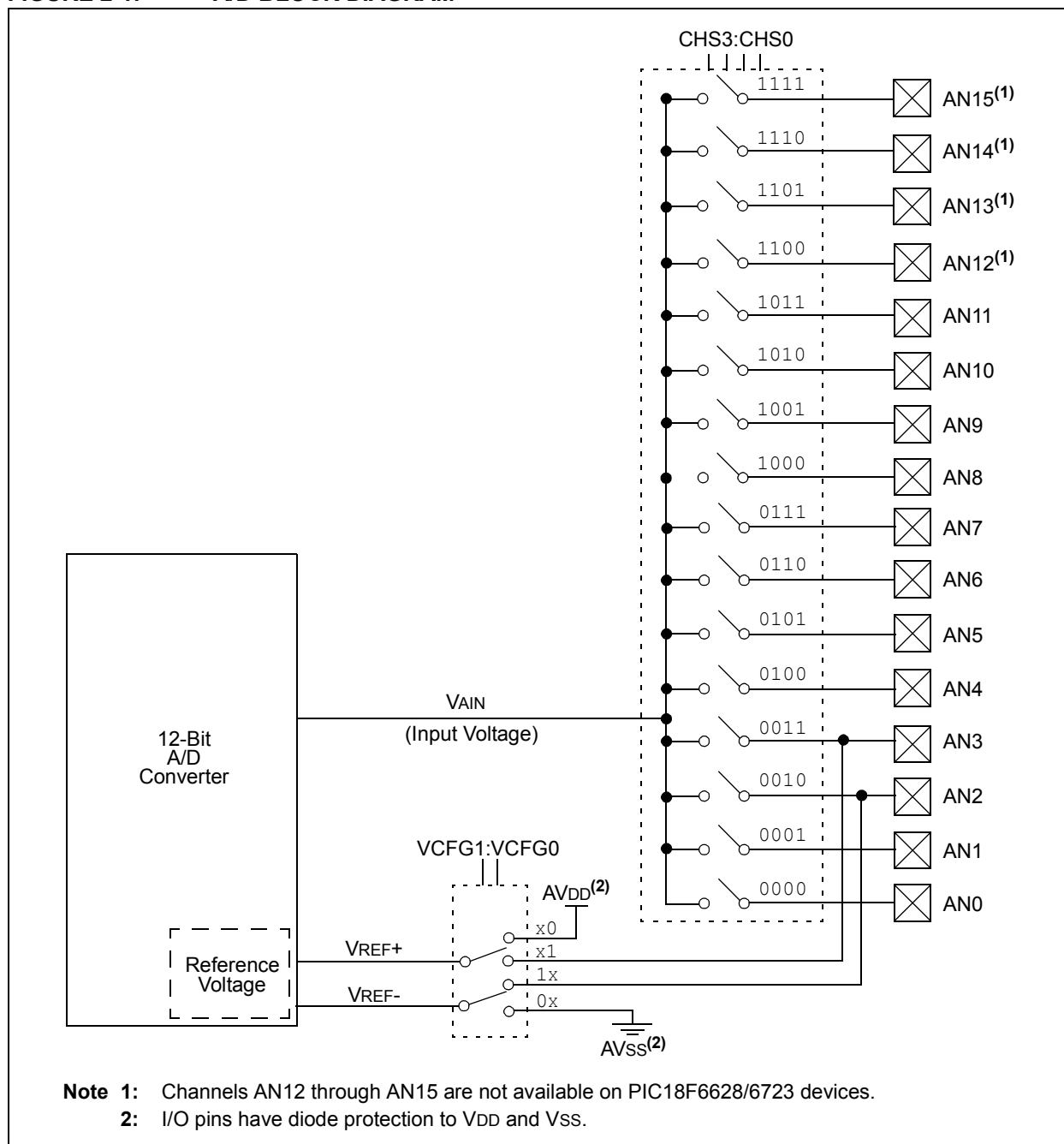
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**



The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets and is not affected by any other Reset.

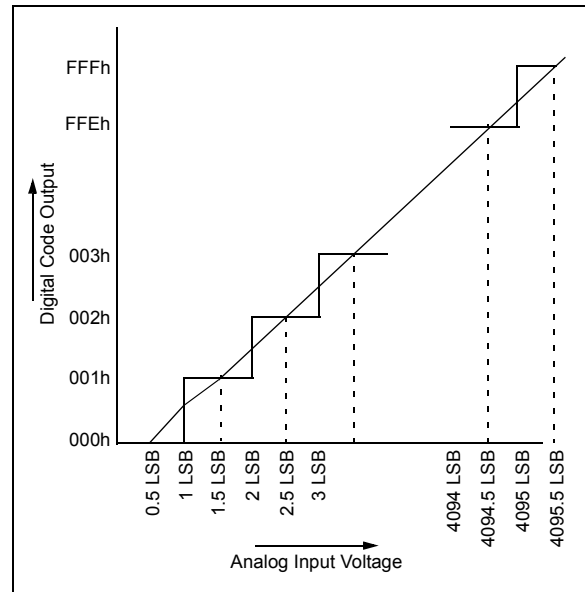
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 “A/D Acquisition Requirements”**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

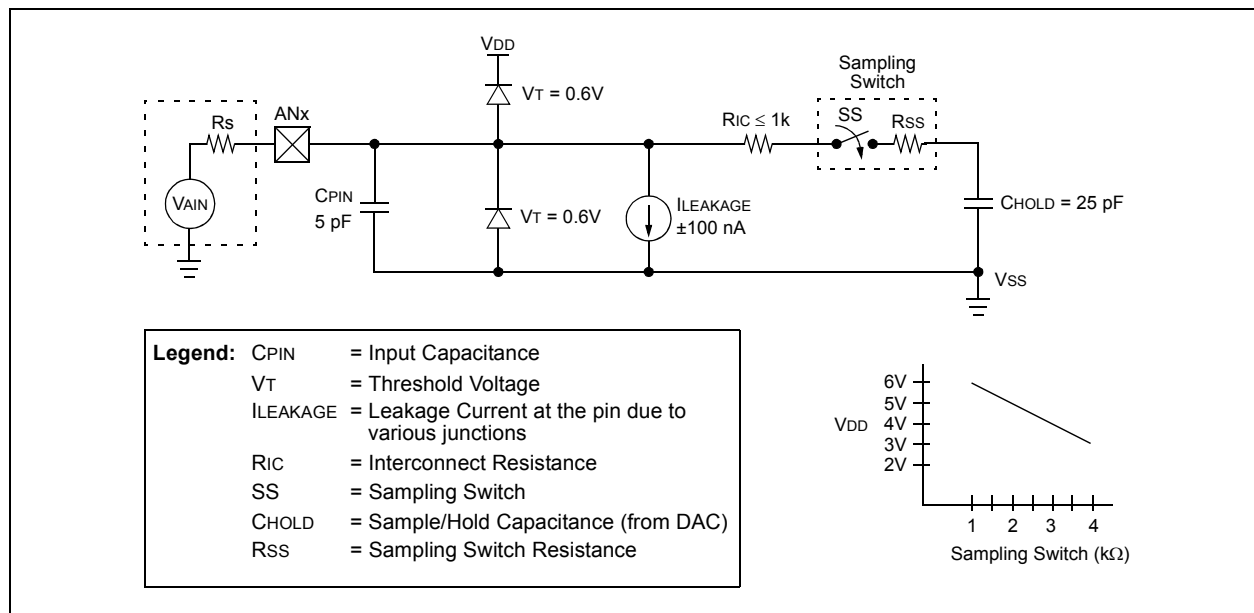
1. Configure the A/D module:
  - Configure analog pins, voltage reference and digital I/O (ADCON1)
  - Select A/D input channel (ADCON0)
  - Select A/D acquisition time (ADCON2)
  - Select A/D conversion clock (ADCON2)
  - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
  - Clear ADIF bit
  - Set ADIE bit
  - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
  - Set GO/DONE bit (ADCON0<1>)

5. Wait for A/D conversion to complete by either:
  - Polling for the GO/DONE bit to be cleared
 OR
  - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as  $T_{AD}$ . A minimum wait of 2  $T_{AD}$  is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**



**FIGURE 2-3: ANALOG INPUT MODEL**



# PIC18F8723 FAMILY

## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

**Note:** When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSB error is used (4096 steps for the 12-bit A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSB
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system max.)

### EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= \text{TAMP} + \text{TC} + \text{TCOFF} \end{aligned}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} \text{V}_{\text{HOLD}} &= (\text{V}_{\text{REF}} - (\text{V}_{\text{REF}}/4096)) \cdot (1 - e^{-(\text{TC}/\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS})}) \\ \text{or} \\ \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \end{aligned}$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{TAMP} + \text{TC} + \text{TCOFF} \\ \text{TAMP} &= 0.2 \mu\text{s} \\ \text{TCOFF} &= (\text{Temp} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad 1.2 \mu\text{s} \end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μs.

$$\begin{aligned} \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \mu\text{s} \\ &\quad -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0002441) \mu\text{s} \\ &\quad 1.56 \mu\text{s} \\ \text{TACQ} &= 0.2 \mu\text{s} + 1.56 \mu\text{s} + 1.2 \mu\text{s} \\ &\quad 2.96 \mu\text{s} \end{aligned}$$

## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 $\mu$ s
Operation	ADCS2:ADCS0	Maximum Fosc
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	40.00 MHz
RC <sup>(1)</sup>	x11	1.00 MHz <sup>(2)</sup>

**Note 1:** The RC source has a typical TAD time of 2.5  $\mu$ s.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

# PIC18F8723 FAMILY

---

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the AD<sub>CS</sub>2:AD<sub>CS</sub>0 bits in AD<sub>CON</sub>2 should be updated in accordance with the clock source to be used. The AC<sub>QT</sub>2:AC<sub>QT</sub>0 bits do not need to be adjusted as the AD<sub>CS</sub>2:AD<sub>CS</sub>0 bits adjust the T<sub>AD</sub> time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If the AC<sub>QT</sub>2:AC<sub>QT</sub>0 bits are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the `SLEEP` instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The AD<sub>CON</sub>1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V<sub>OH</sub> or V<sub>OL</sub>) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

**Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the  $\overline{\text{GO/DONE}}$  bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the  $\overline{\text{GO/DONE}}$  bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

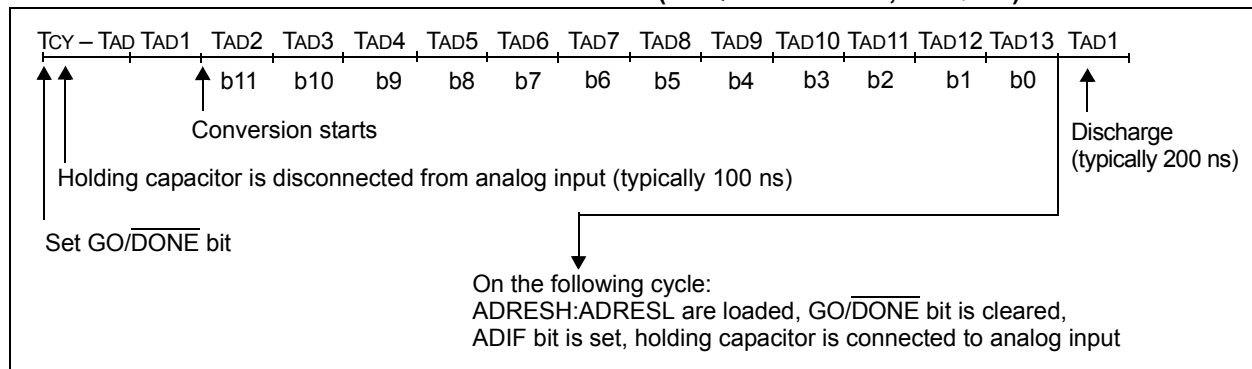
After the A/D conversion is completed or aborted, a 2 T<sub>CY</sub> wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The  $\overline{\text{GO/DONE}}$  bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2  $\mu\text{s}$  after enabling the A/D before beginning an acquisition and conversion cycle.

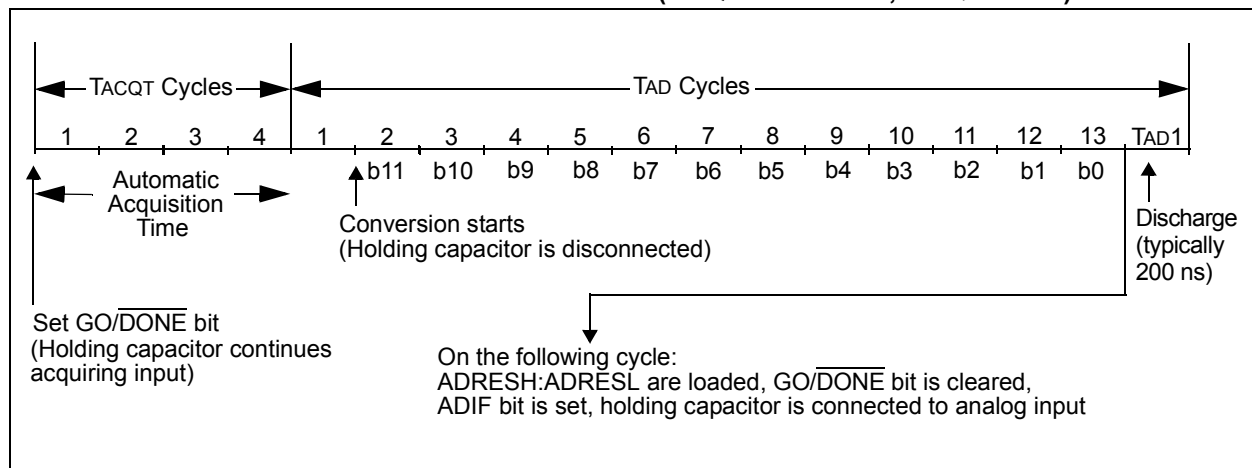
## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



# PIC18F8723 FAMILY

## 2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the

desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(3)
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	(3)
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	(3)
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	(3)
PIR2	OSCFIF	CMIF	—	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	(3)
PIE2	OSCFIE	CMIE	—	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	(3)
IPR2	OSCFIP	CMIP	—	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	(3)
ADRESH	A/D Result Register High Byte								(3)
ADRESL	A/D Result Register Low Byte								(3)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	(3)
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	(3)
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	(3)
TRISA	TRISA7 <sup>(1)</sup>	TRISA6 <sup>(1)</sup>	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	(3)
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	(3)
TRISH <sup>(2)</sup>	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	(3)

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**2:** These registers are not implemented on PIC18F6628/6723 devices.

**3:** For these Reset values, see the "PIC18F8722 Family Data Sheet" (DS39646).

## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to **Section 25.1 “Configuration Bits”** in the *“PIC18F8722 Family Data Sheet”* (DS39646). Device ID information presented in this section is for the PIC18F8723 family only.

PIC18F8723 family devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

## 3.1 Device ID Registers

The Device ID registers are “read-only” registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(1)</sup>
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(1)</sup>

**Legend:** x = unknown

**Note 1:** See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.



# PIC18F8723 FAMILY

## REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F8723 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-5 **DEV2:DEV0:** Device ID bits  
See Register 3-2 for a complete listing.

bit 4-0 **REV4:REV0:** Revision ID bits  
These bits are used to indicate the device revision.

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F8723 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-0 **DEV10:DEV3:** Device ID bits

DEV10:DEV3 (DEVID2<7:0>)	DEV2:DEV0 (DEVID1<7:5>)	Device
0100 1001	110	PIC18F6628
0100 1010	000	PIC18F6723
0100 1001	111	PIC18F8628
0100 1010	001	PIC18F8723

## 4.0 ELECTRICAL CHARACTERISTICS

**Note:** Other than some basic data, this section documents only the PIC18F8723 family's specifications that differ from those of the PIC18F8722 family devices. For detailed information on the electrical specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the "PIC18F8722 Family Data Sheet" (DS39646).

### Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on any pin with respect to V <sub>SS</sub> (except V <sub>DD</sub> and $\overline{\text{MCLR}}$ ) .....	-0.3V to (V <sub>DD</sub> + 0.3V)
Voltage on V <sub>DD</sub> with respect to V <sub>SS</sub> .....	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V <sub>SS</sub> ( <b>Note 2</b> ) .....	0V to +13.25V
Total power dissipation ( <b>Note 1</b> ) .....	1.0W
Maximum current out of V <sub>SS</sub> pin .....	300 mA
Maximum current into V <sub>DD</sub> pin .....	250 mA
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub> ) .....	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> ) .....	±20 mA
Maximum output current sunk by any I/O pin .....	25 mA
Maximum output current sourced by any I/O pin .....	25 mA
Maximum current sunk by all ports .....	200 mA
Maximum current sourced by all ports .....	200 mA

**Note 1:** Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

- 2:** Voltage spikes below V<sub>SS</sub> at the RG5/ $\overline{\text{MCLR}}$ /V<sub>PP</sub> pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the RG5/ $\overline{\text{MCLR}}$ /V<sub>PP</sub> pin, rather than pulling this pin directly to V<sub>SS</sub>.

**† NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# PIC18F8723 FAMILY

FIGURE 4-1: PIC18F8723 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

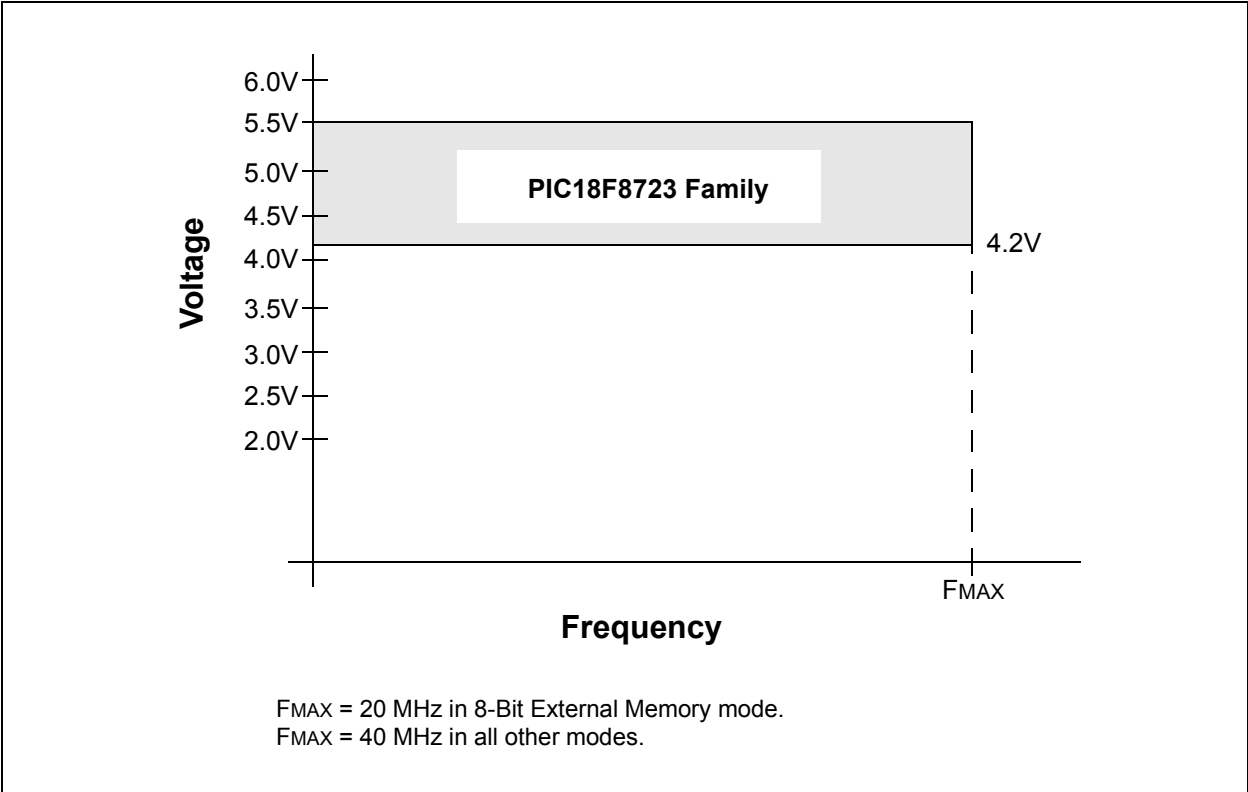
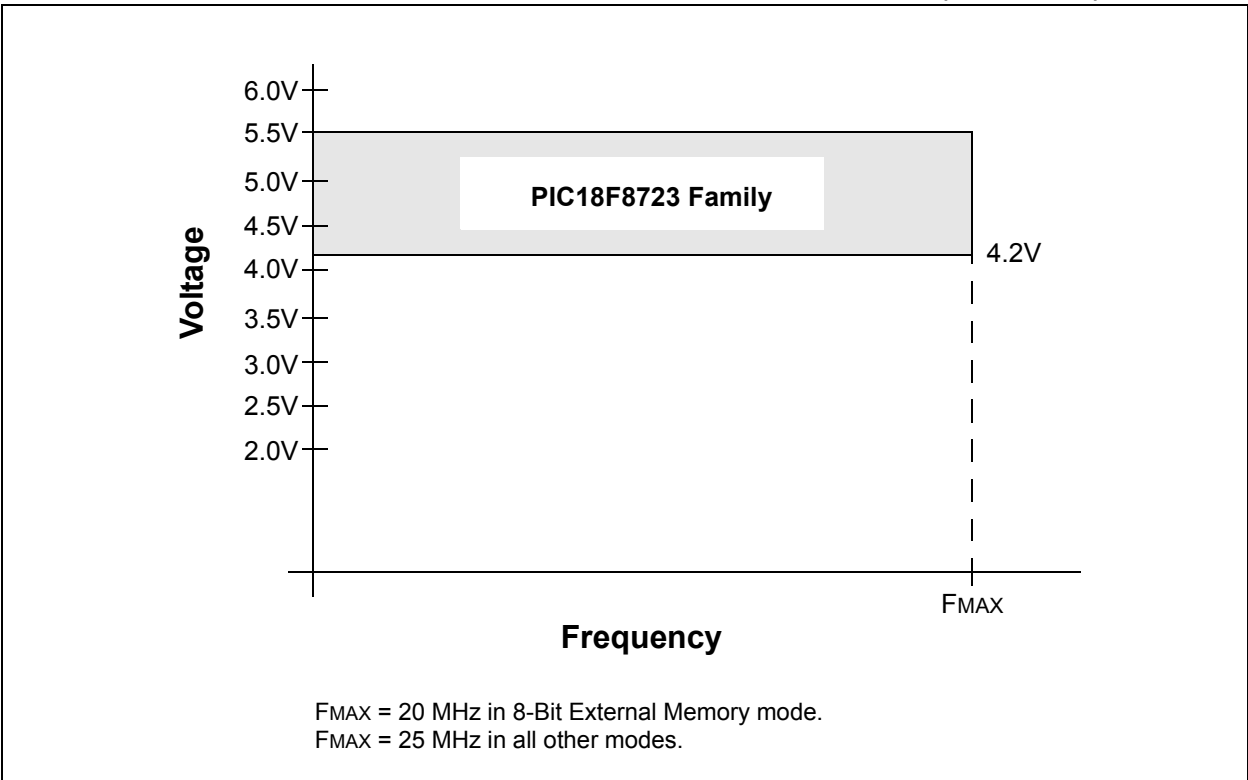
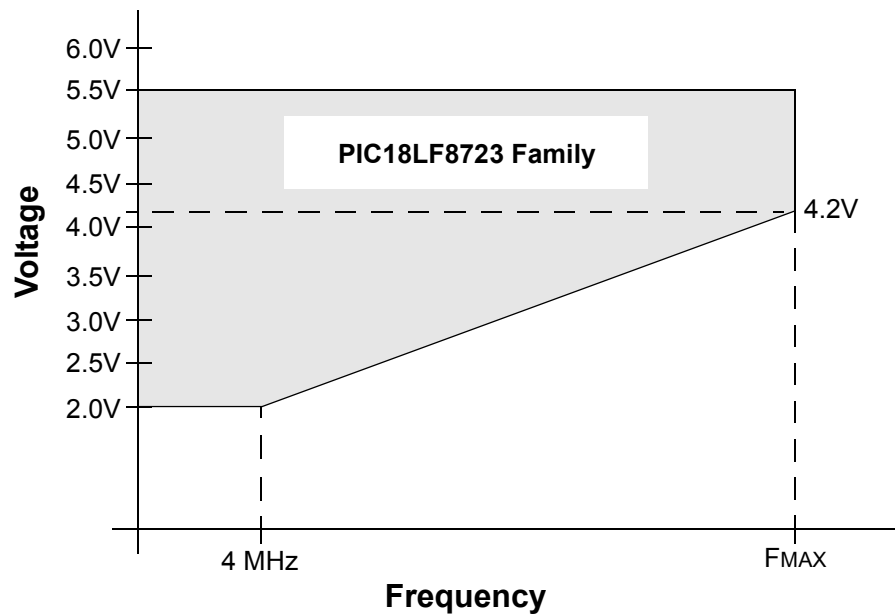


FIGURE 4-2: PIC18F8723 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)



# PIC18F8723 FAMILY

FIGURE 4-3: PIC18LF8723 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



In 8-Bit External Memory mode:

$F_{MAX} = (9.55 \text{ MHz/V}) (V_{DDAPP\text{MIN}} - 2.0\text{V}) + 4 \text{ MHz}$ , if  $V_{DDAPP\text{MIN}} \leq 4.2\text{V}$ ;  
 $F_{MAX} = 25 \text{ MHz}$ , if  $V_{DDAPP\text{MIN}} > 4.2\text{V}$ .

In all other modes:

$F_{MAX} = (16.36 \text{ MHz/V}) (V_{DDAPP\text{MIN}} - 2.0\text{V}) + 4 \text{ MHz}$ ;  
 $F_{MAX} = 40 \text{ MHz}$ , if  $V_{DDAPP\text{MIN}} > 4.2\text{V}$ .

**Note:**  $V_{DDAPP\text{MIN}}$  is the minimum voltage of the PIC<sup>®</sup> device in the application.

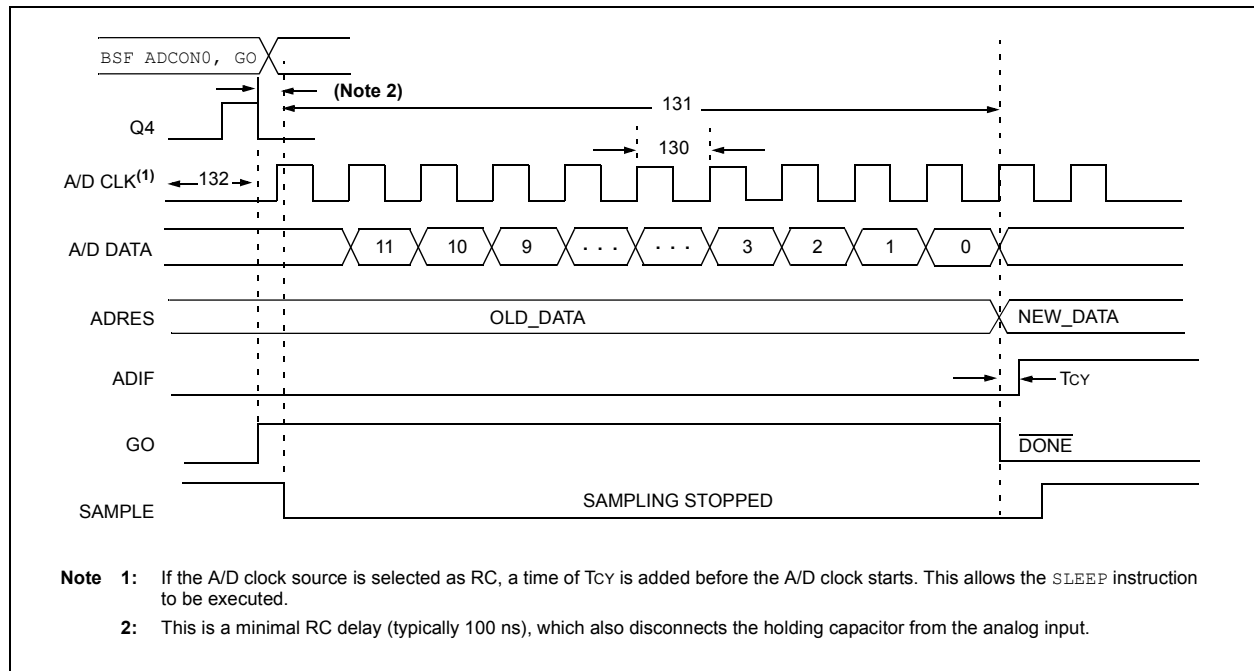
# PIC18F8723 FAMILY

**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F8723 FAMILY (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions	
A01	NR	Resolution	—	—	12	bit		$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	$\pm 2.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.0$	LSB	$V_{DD} = 5.0V$	
A04	EDL	Differential Linearity Error	—	$<\pm 1$	$+1.5/-1.0$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$+1.5/-1.0$	LSB	$V_{DD} = 5.0V$	
A06	EOFF	Offset Error	—	$<\pm 1$	$\pm 5$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 3$	LSB	$V_{DD} = 5.0V$	
A07	EGN	Gain Error	—	$<\pm 1$	$\pm 1.25$	LSB	$V_{DD} = 3.0V$	$\Delta V_{REF} \geq 3.0V$
			—	—	$\pm 2.00$	LSB	$V_{DD} = 5.0V$	
A10	—	Monotonicity	Guaranteed <sup>(1)</sup>			—		$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	$\Delta V_{REF}$	Reference Voltage Range ( $V_{REFH} - V_{REFL}$ )	3	—	$V_{DD} - V_{SS}$	V		For 12-bit resolution
A21	$V_{REFH}$	Reference Voltage High	$V_{SS} + 3.0V$	—	$V_{DD} + 0.3V$	V		For 12-bit resolution
A22	$V_{REFL}$	Reference Voltage Low	$V_{SS} - 0.3V$	—	$V_{DD} - 3.0V$	V		For 12-bit resolution
A25	$V_{AIN}$	Analog Input Voltage	$V_{REFL}$	—	$V_{REFH}$	V		
A30	$Z_{AIN}$	Recommended Impedance of Analog Voltage Source	—	—	2.5	k $\Omega$		
A50	I <sub>REF</sub>	V <sub>REF</sub> Input Current <sup>(2)</sup>	—	—	5	$\mu A$		During V <sub>AIN</sub> acquisition. During A/D conversion cycle.
			—	—	150	$\mu A$		

- Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
- Note 2:**  $V_{REFH}$  current is from the RA3/AN3/V<sub>REF</sub>+ pin or V<sub>DD</sub>, whichever is selected as the V<sub>REFH</sub> source.  $V_{REFL}$  current is from the RA2/AN2/V<sub>REF</sub>-/ $\overline{CVREF}$  pin or V<sub>SS</sub>, whichever is selected as the V<sub>REFL</sub> source.

**FIGURE 4-4: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	$\mu\text{s}$ TOSC based, $V_{REF} \geq 3.0\text{V}$
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	$\mu\text{s}$ $V_{DD} = 3.0\text{V}$ ; TOSC based, $V_{REF}$ full range
			PIC18FXXXX	—	1	$\mu\text{s}$ A/D RC mode
			PIC18LFXXXX	—	3	$\mu\text{s}$ $V_{DD} = 3.0\text{V}$ ; A/D RC mode
131	TCNV	Conversion Time (not including acquisition time) <sup>(2)</sup>	13	14	TAD	
132	TACQ	Acquisition Time <sup>(3)</sup>	1.4	—	$\mu\text{s}$	
135	TSWC	Switching Time from Convert → Sample	—	(Note 4)		
137	TDIS	Discharge Time	0.2	—	$\mu\text{s}$	

**Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

**Note 2:** ADRES registers may be read on the following  $T_{cy}$  cycle.

**Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion ( $V_{DD}$  to  $V_{SS}$  or  $V_{SS}$  to  $V_{DD}$ ). The source impedance ( $R_s$ ) on the input channels is  $50\Omega$ .

**Note 4:** On the following cycle of the device clock.

# PIC18F8723 FAMILY

---

NOTES:

## 5.0 PACKAGING INFORMATION

For packaging information, see the “*PIC18F8722 Family Data Sheet*” (DS39646).



# PIC18F8723 FAMILY

---

NOTES:

# PIC18F8723 FAMILY

## APPENDIX A: REVISION HISTORY

### Revision A (August 2007)

Original data sheet for the PIC18F8723 family of devices.

### Revision B (October 2009)

Updated to remove Preliminary status.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: PIC18F8723 FAMILY DEVICE DIFFERENCES**

Features	PIC18F6628	PIC18F6723	PIC18F8628	PIC18F8723
Program Memory (Bytes)	96K	128K	96K	128K
Program Memory (Instructions)	49152	65536	49152	65536
Interrupt Sources	28	28	29	29
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Capture/Compare/PWM Modules	2	2	2	2
Enhanced Capture/Compare/PWM Modules	3	3	3	3
Parallel Communications (PSP)	Yes	Yes	Yes	Yes
External Memory Bus	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	12 Input Channels	12 Input Channels	16 Input Channels	16 Input Channels
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

# PIC18F8723 FAMILY

---

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**

## **APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES**

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, *"Migrating Designs from PIC16C74A/74B to PIC18C442"*. The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available on our web site, [www.microchip.com](http://www.microchip.com), as Literature Number DS00716.

## **APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES**

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN726, *"PIC17CXXX to PIC18CXXX Migration"*.

This Application Note is available on our web site, [www.microchip.com](http://www.microchip.com), as Literature Number DS00726.

# PIC18F8723 FAMILY

---

NOTES:

## INDEX

### A

A/D .....	31
A/D Converter Interrupt, Configuring .....	35
Acquisition Requirements .....	36
ADCON0 Register .....	31
ADCON1 Register .....	31
ADCON2 Register .....	31
ADRESH Register .....	31, 34
ADRESL Register .....	31
Analog Port Pins, Configuring .....	38
Associated Registers .....	40
Configuring the Module .....	35
Conversion Clock (TAD) .....	37
Conversion Status (GO/DONE Bit) .....	34
Conversions .....	39
Converter Characteristics .....	46
Discharge .....	39
Operation in Power-Managed Modes .....	38
Selecting and Configuring Acquisition Time .....	37
Special Event Trigger (ECCP2) .....	40
Transfer Function .....	35
Use of the ECCP2 Trigger .....	40
Absolute Maximum Ratings .....	43
ADCON0 Register .....	31
GO/DONE Bit .....	34
ADCON1 Register .....	31
ADCON2 Register .....	31
ADRESH Register .....	31
ADRESL Register .....	31, 34
Analog-to-Digital Converter. See A/D.	

### B

Block Diagrams .....	
A/D .....	34
Analog Input Model .....	35
PIC18F6628/6723 .....	11
PIC18F8628/8723 .....	12

### C

Compare (ECCP2 Module) .....	
Special Event Trigger .....	40
Conversion Considerations .....	52
Customer Change Notification Service .....	57
Customer Notification Service .....	57
Customer Notification System .....	7
Customer Support .....	57

### D

Device Differences .....	51
Device ID Registers .....	41
Device Overview .....	
Features (table) .....	10
Special Features .....	9

### E

Electrical Characteristics .....	43
Equations .....	
A/D Acquisition Time .....	36
A/D Minimum Charging Time .....	36
Calculating the Minimum Required Acquisition Time .....	36
Errata .....	7
External Memory Interface .....	3

### F

Features Summary Table .....	3
------------------------------	---

### I

Internet Address .....	57
Interrupt Sources .....	
A/D Conversion Complete .....	35

### M

Microchip Internet Web Site .....	57
Migration From Baseline to Enhanced Devices .....	52
Migration From High-End to Enhanced Devices .....	53
Migration From Mid-Range to Enhanced Devices .....	53
More Information .....	7
Customer Notification System .....	7
Errata .....	7

### O

Overview .....	
External Memory Interface .....	3
Features Summary Table .....	3
Peripheral Highlights .....	3
Power-Managed Modes .....	3
Special Microcontroller Features .....	3

### P

Packaging Information .....	49
Peripheral Highlights .....	3
Pin Diagrams .....	
64-Pin TQFP .....	4
80-Pin TQFP .....	5
Pin Functions .....	
AVDD (64-pin) .....	20
AVDD (80-pin) .....	30
AVss (64-pin) .....	20
AVss (80-pin) .....	30
OSC1/CLKI/RA7 .....	13, 21
OSC2/CLKO/RA6 .....	13, 21
RA0/AN0 .....	14, 22
RA1/AN1 .....	14, 22
RA2/AN2/VREF- .....	14, 22
RA3/AN3/VREF+ .....	14, 22
RA4/T0CKI .....	14, 22
RA5/AN4/HLVDIN .....	14, 22
RB0/INT0/FLT0 .....	15, 23
RB1/INT1 .....	15, 23
RB2/INT2 .....	15, 23
RB3/INT3 .....	15
RB3/INT3/ECCP2/P2A .....	23
RB4/KBI0 .....	15, 23
RB5/KBI1/PGM .....	15, 23
RB6/KBI2/PGC .....	15, 23
RB7/KBI3/PGD .....	15, 23
RC0/T1OSO/T13CKI .....	16, 24
RC1/T1OSI/ECCP2/P2A .....	16, 24
RC2/ECCP1/P1A .....	16, 24
RC3/SCK1/SCL1 .....	16, 24
RC4/SDI1/SDA1 .....	16, 24
RC5/SDO1 .....	16, 24
RC6/TX1/CK1 .....	16, 24
RC7/RX1/DT1 .....	16, 24
RD0/AD0/PSP0 .....	25
RD0/PSP0 .....	17

# PIC18F8723 FAMILY

RD1/AD1/PSP1 .....	25
RD1/PSP1 .....	17
RD2/AD2/PSP2 .....	25
RD2/PSP2 .....	17
RD3/AD3/PSP3 .....	25
RD3/PSP3 .....	17
RD4/AD4/PSP4/SDO2 .....	25
RD4/PSP4/SDO2 .....	17
RD5/AD5/PSP5/SDI2/SDA2 .....	25
RD5/PSP5/SDI2/SDA2 .....	17
RD6/AD6/PSP6/SCK2/SCL2 .....	25
RD6/PSP6/SCK2/SCL2 .....	17
RD7/AD7/PSP7/SS2 .....	25
RD7/PSP7/SS2 .....	17
RE0/AD8/RD/P2D .....	26
RE0/RD/P2D .....	18
RE1/AD9/WR/P2C .....	26
RE1/WR/P2C .....	18
RE2/AD10/CS/P2B .....	26
RE2/CS/P2D .....	18
RE3/AD11/P3C .....	26
RE3/P3C .....	18
RE4/AD12/P3B .....	26
RE4/P3B .....	18
RE5/AD13/P1C .....	26
RE5/P1C .....	18
RE6/AD14/P1B .....	26
RE6/P1B .....	18
RE7/AD15/ECCP2/P2A .....	26
RE7/ECCP2/P2A .....	18
RF0/AN5 .....	19, 27
RF1/AN6/C2OUT .....	19, 27
RF2/AN7/C1OUT .....	19, 27
RF3/AN8 .....	19, 27
RF4/AN9 .....	19, 27
RF5/AN10/CVREF .....	19, 27
RF6/AN11 .....	19, 27
RF7/SS1 .....	19, 27
RG0/ECCP3/P3A .....	20, 28
RG1/TX2/CK2 .....	20, 28
RG2/RX2/DT2 .....	20, 28
RG3/CCP4/P3D .....	20, 28
RG4/CCP5/P1D .....	20, 28
RG5 .....	20, 28
RG5/MCLR/VPP .....	13, 21
RH0/A16 .....	29
RH1/A17 .....	29
RH2/A18 .....	29
RH3/A19 .....	29
RH4/AN12/P3C .....	29
RH5/AN13/P3B .....	29
RH6/AN14/P1C .....	29
RH7/AN15/P1B .....	29
RJ0/ALE .....	30
RJ1/OE .....	30
RJ2/WRL .....	30
RJ3/WRH .....	30
RJ4/BA0 .....	30
RJ5/CE .....	30
RJ6/LB .....	30
RJ7/UB .....	30
VDD .....	20
VDD .....	30
VSS .....	20
VSS .....	30

Pinout I/O Descriptions .....	13
PIC18F6628/6723 .....	21
PIC18F8628/8723 .....	3
Power-Managed Modes .....	38
and A/D Operation .....	59
Product Identification System .....	59

## R

Reader Response .....	58
Registers .....	
ADCON0 (A/D Control 0) .....	31
ADCON1 (A/D Control 1) .....	32
ADCON2 (A/D Control 2) .....	33
DEVID1 (Device ID 1) .....	42
DEVID2 (Device ID 2) .....	42
Revision History .....	51

## S

Special Features of the CPU .....	41
Device ID Registers .....	41
Special Microcontroller Features .....	3

## T

Timing Diagrams .....	
A/D Conversion .....	47
Timing Diagrams and Specifications .....	
A/D Conversion Requirements .....	47

## V

Voltage-Frequency Graphs .....	
Extended (PIC18F8723) .....	44
Industrial (PIC18F8723) .....	44
Industrial (PIC18LF8723) .....	45

## W

WWW Address .....	57
WWW, On-Line Support .....	7

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at [www.microchip.com](http://www.microchip.com). This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at [www.microchip.com](http://www.microchip.com), click on Customer Change Notification and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at: <http://support.microchip.com>**



# PIC18F8723 FAMILY

---

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager  
RE: Reader Response  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: PIC18F8723 Family Literature Number: DS39894B

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this document easy to follow? If not, why?

---

---

4. What additions to the document do you think would enhance the structure and subject?

---

---

5. What deletions from the document could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

# PIC18F8723 FAMILY

## PIC18F8723 FAMILY PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device <sup>(1) (2)</sup>	PIC18F6628/6723, PIC18F8628/8723, VDD range 4.2V to 5.5V PIC18LF6628/6723, PIC18LF8628/8723 <sup>(1)</sup> VDD range 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flatpack)		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

a) PIC18LF6723-I/PT 301 = Industrial temp., TQFP package, Extended VDD limits, QTP pattern #301.

b) PIC18F6723-E/PT = Extended temp., TQFP package, standard VDD limits.

**Note 1:** F = Standard Voltage Range  
LF = Wide Voltage Range

**2:** T = in tape and reel TQFP packages only.



---

## WORLDWIDE SALES AND SERVICE

---

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://support.microchip.com>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

#### Atlanta

Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

#### Boston

Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

#### Chicago

Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Cleveland

Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

#### Dallas

Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

Kokomo, IN  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

#### Santa Clara

Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

#### Toronto

Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Asia Pacific Office

Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### Australia - Sydney

Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Tel: 86-10-8528-2100  
Fax: 86-10-8528-2104

#### China - Chengdu

Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

#### China - Hong Kong SAR

Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Nanjing

Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

#### China - Qingdao

Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

#### China - Shanghai

Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

#### China - Shenyang

Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

#### China - Shenzhen

Tel: 86-755-8203-2660  
Fax: 86-755-8203-1760

#### China - Wuhan

Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

#### China - Xiamen

Tel: 86-592-2388138  
Fax: 86-592-2388130

#### China - Xian

Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

#### China - Zhuhai

Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

#### India - Bangalore

Tel: 91-80-3090-4444  
Fax: 91-80-3090-4080

#### India - New Delhi

Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

#### India - Pune

Tel: 91-20-2566-1512  
Fax: 91-20-2566-1513

#### Japan - Yokohama

Tel: 81-45-471- 6166  
Fax: 81-45-471-6122

#### Korea - Daegu

Tel: 82-53-744-4301  
Fax: 82-53-744-4302

#### Korea - Seoul

Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

#### Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

#### Malaysia - Penang

Tel: 60-4-227-8870  
Fax: 60-4-227-4068

#### Philippines - Manila

Tel: 63-2-634-9065  
Fax: 63-2-634-9069

#### Singapore

Tel: 65-6334-8870  
Fax: 65-6334-8850

#### Taiwan - Hsin Chu

Tel: 886-3-6578-300  
Fax: 886-3-6578-370

#### Taiwan - Kaohsiung

Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan - Taipei

Tel: 886-2-2500-6610  
Fax: 886-2-2508-0102

#### Thailand - Bangkok

Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

#### Austria - Wels

Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

#### Denmark - Copenhagen

Tel: 45-4450-2828  
Fax: 45-4485-2829

#### France - Paris

Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany - Munich

Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy - Milan

Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands - Drunen

Tel: 31-416-690399  
Fax: 31-416-690340

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### UK - Wokingham

Tel: 44-118-921-5869  
Fax: 44-118-921-5820

03/26/09