

PIC16(L)F170X/171X

Clocking Structure:

- 16 MHz Internal Oscillator Block:
 - $\pm 1\%$ at calibration
 - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
 - Three crystal/resonator modes up to 20 MHz
 - Two external clock modes up to 32 MHz
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- Oscillator Start-up Timer (OST)

Programming/Debug Features:

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
 - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC16(L)F170X/171X FAMILY TYPES

Device	Program Memory Flash (words)	Data SRAM (bytes)	I/O Pins	8-bit/16-bit Timers	High-Speed Comparators	Op Amp	10-bit ADC (ch)	5-/8-bit DAC	Zero Cross	CCP/PWM	COG	EUSART	I ² C™/SPI	CLC	NCO	Debug ⁽¹⁾
PIC16(L)F1703	2k	256	12	2/1	0	2	8	0/0	1	2/0	0	0	1	0	0	I/E
PIC16(L)F1704	4k	512	12	4/1	2	2	8	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1705	8k	1024	12	4/1	2	2	8	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1707	2k	256	18	2/1	0	2	8	0/0	1	2/0	0	0	1	0	0	I/E
PIC16(L)F1708	4k	512	18	4/1	2	2	12	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1709	8k	1024	18	4/1	2	2	12	0/1	1	2/2	1	1	1	3	0	I/E
PIC16(L)F1713	4k	512	25	4/1	2	2	17	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1716	8k	1024	25	4/1	2	2	17	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1717	8k	1024	36	4/1	2	2	28	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1718	16k	2048	25	4/1	2	2	17	1/1	1	2/2	1	1	1	4	1	I/E
PIC16(L)F1719	16k	2048	36	4/1	2	2	28	1/1	1	2/2	1	1	1	4	1	I/E

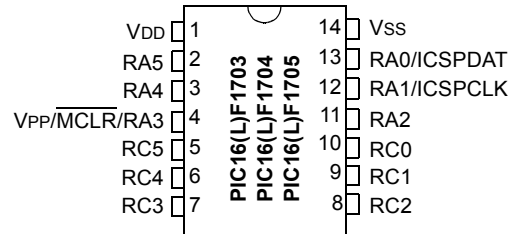
Note 1: I – Debugging integrated on chip; H – Debugging via ICD header; E – Debugging via Emulation header.

PACKAGES

Device	PDIP	TSSOP	QFN (4x4x0.9)	SOIC	SSOP	SPDIP	QFN (6x6x0.9)	UQFN (4x4x0.5)	TQFP	UQFN (5x5x0.5)
PIC16F1703	x	x	x	x						
PIC16F1704	x	x	x	x						
PIC16F1705	x	x	x	x						
PIC16F1707	x		x	x	x					
PIC16F1708	x		x	x	x					
PIC16F1709	x		x	x	x					
PIC16F1713				x	x	x	x	x		
PIC16F1716				x	x	x	x	x		
PIC16F1717	x								x	x
PIC16F1718				x	x	x	x	x		
PIC16F1719	x								x	x

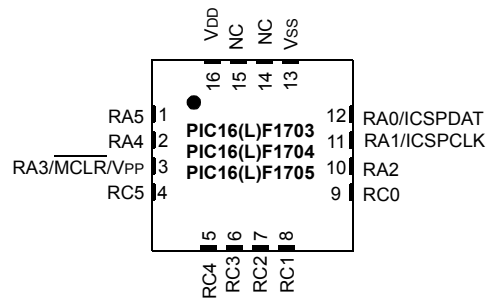
PIC16(L)F170X/171X

PIN DIAGRAM – 14-PIN PDIP, SOIC, SSOP



Note: See [Table 1](#) and [Table 2](#) for the pin allocation tables.

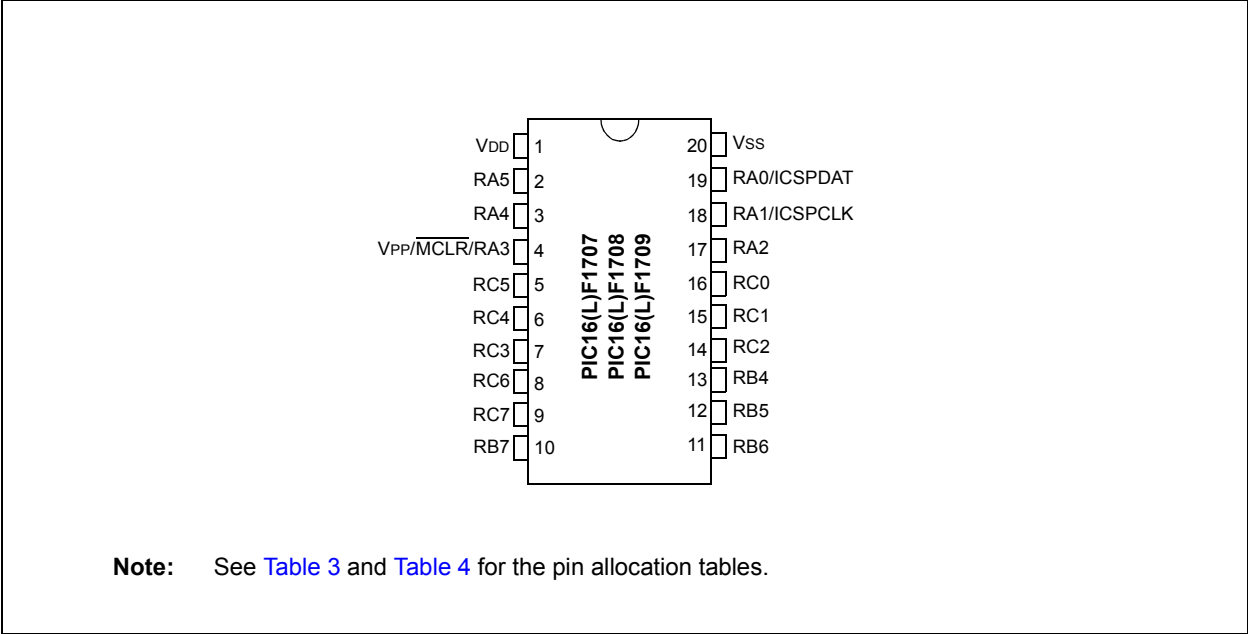
PIN DIAGRAM – 16-PIN QFN



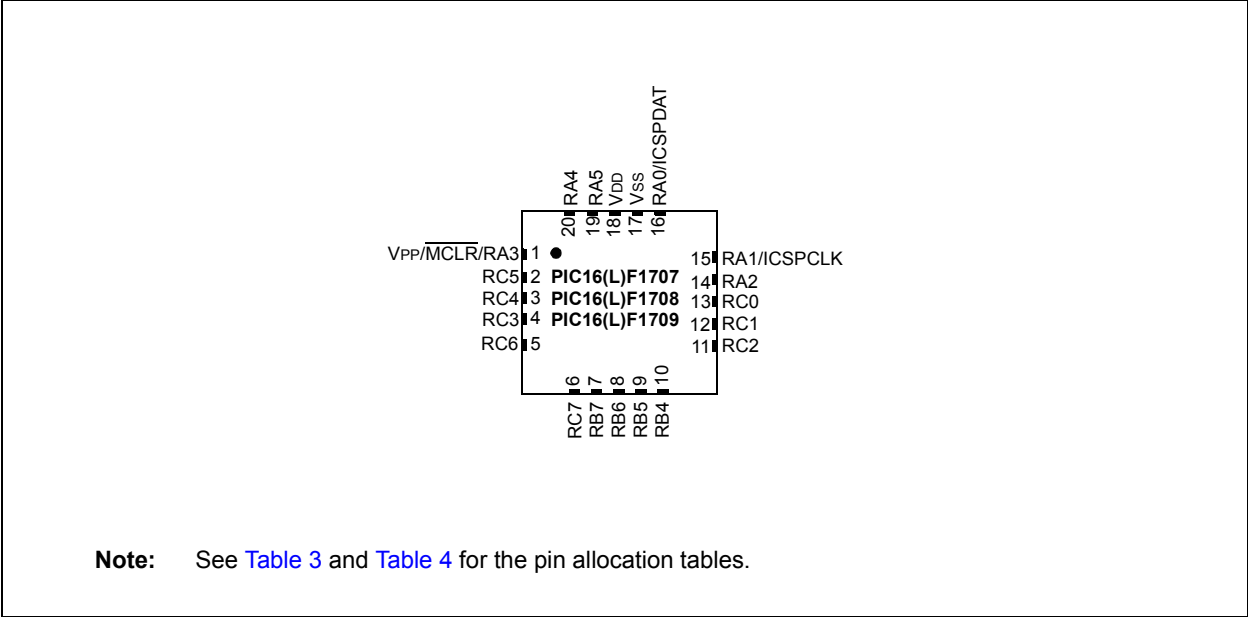
Note: See [Table 1](#) and [Table 2](#) or the pin allocation tables.

PIC16(L)F170X/171X

PIN DIAGRAM – 20-PIN PDIP, SOIC, SSOP

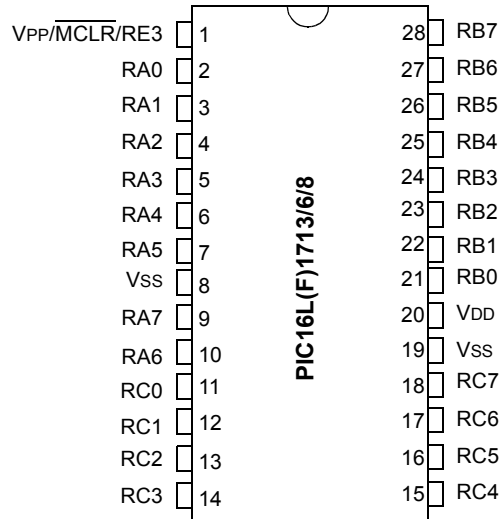


PIN DIAGRAM – 20-PIN QFN



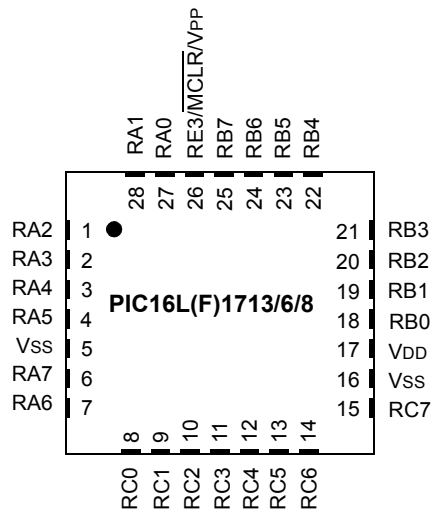
PIC16(L)F170X/171X

PIN DIAGRAM – 28-PIN PDIP, SOIC, SSOP



Note: See [Table 5](#) and [Table 6](#) for the pin allocation table.

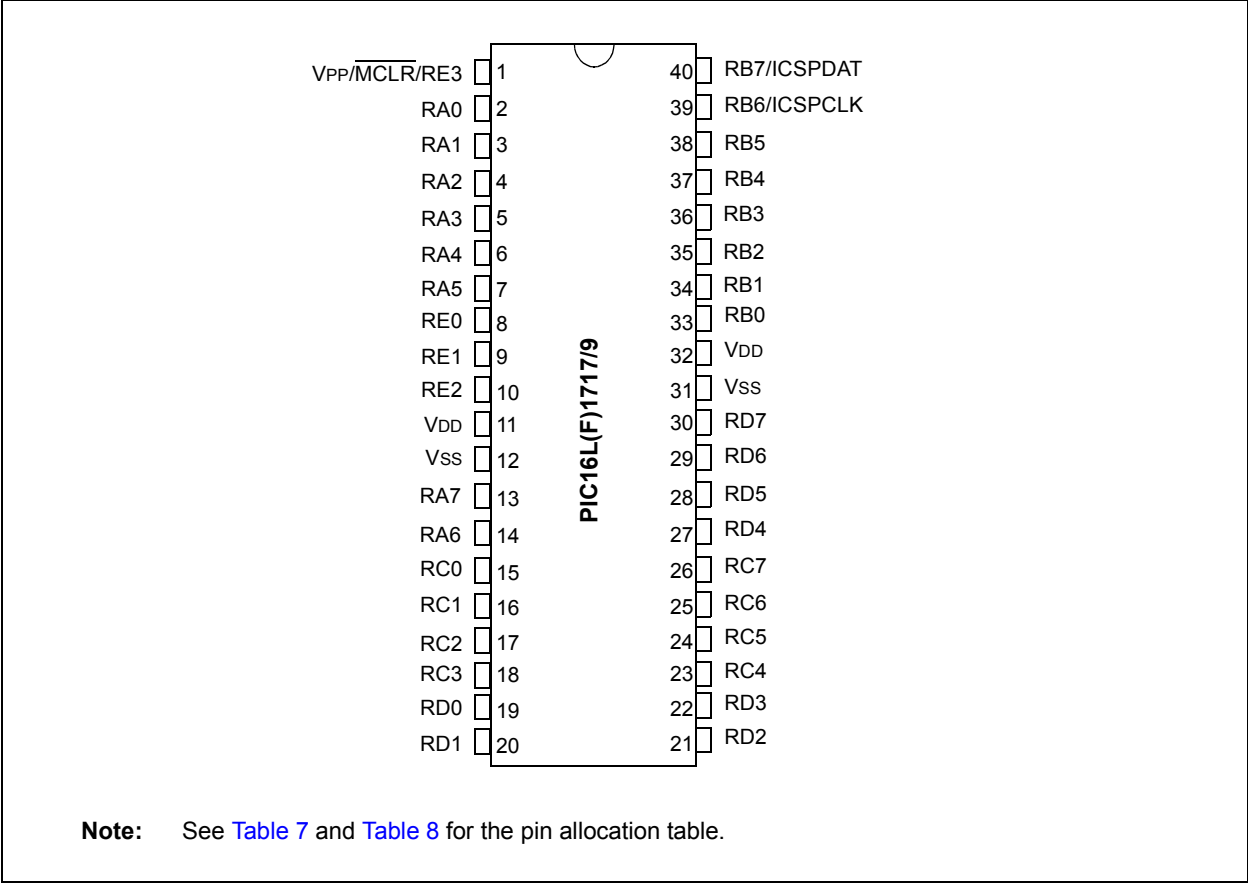
PIN DIAGRAM – 28-PIN (U)QFN



Note: See [Table 5](#) and [Table 6](#) for the pin allocation table.

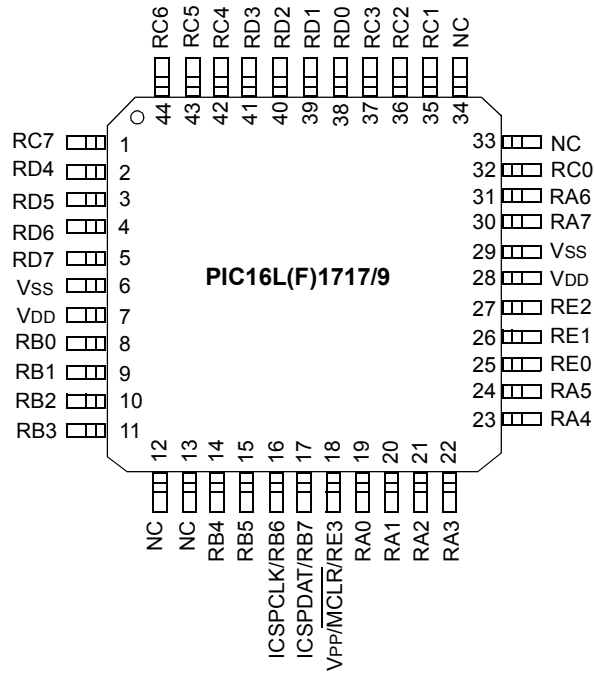
PIC16(L)F170X/171X

PIN DIAGRAM – 40-PIN PDIP



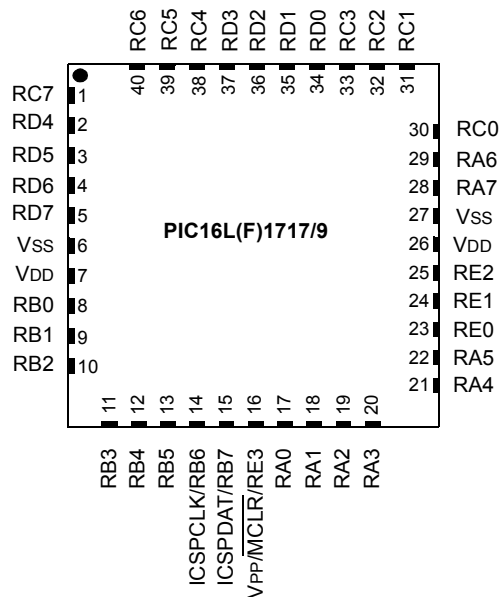
PIC16(L)F170X/171X

PIN DIAGRAM – 44-PIN TQFP (10x10)



Note: See [Table 7](#) and [Table 8](#) for the pin allocation table.

PIN DIAGRAM – 40-PIN UQFN (5x5)



Note: See [Table 7](#) and [Table 8](#) for the pin allocation table.

PIC16(L)F170X/171X

TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1703)

I/O ⁽²⁾	PDI ¹ /SOIC/SSOP	QFN	ADC	Reference	Op Amp	Zero Cross	Timers	CCP	MSSP	CLC	Interrupt	Pull-up	Basic
RA0	13	12	AN0	VREF-	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	ZCD	T0CK1 ⁽¹⁾	—	—	—	INT ⁽¹⁾ IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$ VPP
RA4	3	2	AN3	—	—	—	T1G ⁽¹⁾	—	—	—	IOC	Y	CLKOUT
RA5	2	1	—	—	—	—	T1CK1 ⁽¹⁾	—	—	—	IOC	Y	CLKIN
RC0	10	9	AN4	—	OPA1IN+	—	—	—	SCK ⁽¹⁾ SCL ⁽³⁾	—	IOC	Y	—
RC1	9	8	AN5	—	OPA1IN-	—	—	—	SDI ⁽¹⁾ SDA ⁽³⁾	—	IOC	Y	—
RC2	8	7	AN6	—	OPA1OUT	—	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	OPA2OUT	—	—	CCP2 ⁽¹⁾	SS ⁽¹⁾	—	IOC	Y	—
RC4	6	5	—	—	OPA2IN-	—	—	—	—	—	IOC	Y	—
RC5	5	4	—	—	OPA2IN+	—	—	CCP1 ⁽¹⁾	—	—	IOC	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	—	—	—	—	—	—	CPP1	SDA ⁽³⁾	—	—	—	—
	—	—	—	—	—	—	—	CPP2	SCL ⁽³⁾ SCK	—	—	—	—
	—	—	—	—	—	—	—	—	SDO	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 2: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1704/5)

I/O ⁽²⁾	PDIP/SOIC/SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	13	12	AN0	VREF-	C1IN+	—	DAC1OUT	—	—	—	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	11	10	AN2	—	—	—	DAC1OUT2	ZCD	T0CKI ⁽¹⁾	—	—	COGIN ⁽¹⁾	—	—	—	INT ⁽¹⁾ IOC	Y	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	MCLR V _{PP}
RA4	3	2	AN3	—	—	—	—	—	T1G ⁽¹⁾ SOSCO	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	1	—	—	—	—	—	—	T1CKI ⁽¹⁾ SOSCI	—	—	—	—	—	CLCIN3 ⁽¹⁾	IOC	Y	CLKIN OSC1
RC0	10	9	AN4	—	C2IN+	OPA1IN+	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	OPA1IN-	—	—	—	—	—	—	—	—	CLCIN2 ⁽¹⁾	IOC	Y	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	OPA1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	OPA2OUT	—	—	—	CCP2 ⁽¹⁾	—	—	SS ⁽¹⁾	—	CLCIN0 ⁽¹⁾	IOC	Y	—
RC4	6	5	—	—	—	OPA2IN-	—	—	—	—	—	—	—	CK ⁽¹⁾	CLCIN1 ⁽¹⁾	IOC	Y	—
RC5	5	4	—	—	—	OPA2IN+	—	—	—	CCP1 ⁽¹⁾	—	—	—	RX ⁽³⁾	—	IOC	Y	—
V _{DD}	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V _{DD}
V _{SS}	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	V _{SS}
OUT ⁽²⁾	—	—	—	—	C1OUT	—	—	—	—	CPP1	PWM3OUT	COGA	SDA ⁽³⁾	CK	CLC1OUT	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CPP2	PWM4OUT	COGB	SCL ⁽³⁾	DT ⁽³⁾	CLC2OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGC	SDO	TX	CLC3OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGD	SCK	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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TABLE 3: 20-PIN ALLOCATION TABLE (PIC16(L)F1707)

I/O ⁽²⁾	PDI/SSOP/ SOIC	QFN	ADC	Reference	Op Amp	Zero Cross	Timers	CCP	MSSP	Interrupt	Pull-up	Basic
RA0	19	16	AN0	VREF-	—	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	15	AN1	VREF+	—	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	14	AN2	—	—	ZCD	T0CKI ⁽¹⁾	—	—	INT ⁽¹⁾	Y	—
RA3	4	1	—	—	—	—	—	—	—	IOC	Y	MCLR V _{PP}
RA4	3	20	AN3	—	—	—	T1G ⁽¹⁾	—	—	IOC	Y	CLKOUT
RA5	2	19	—	—	—	—	T1CKI	—	—	IOC	Y	CLKIN
RB4	13	10	AN10	—	OPA1IN-	—	—	—	SCK ⁽¹⁾ SDA ⁽³⁾	IOC	Y	—
RB5	12	9	AN11	—	OPA1IN+	—	—	—	—	IOC	Y	—
RB6	11	8	—	—	—	—	—	—	SDI ⁽¹⁾ SCL ⁽³⁾	IOC	Y	—
RB7	10	7	—	—	—	—	—	—	—	IOC	Y	—
RC0	16	13	AN4	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	—	—	—	—	—	IOC	Y	—
RC2	14	11	AN6	—	OPA1OUT	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	OPA2OUT	—	—	CCP2 ⁽¹⁾	—	IOC	Y	—
RC4	6	3	—	—	OPA2IN-	—	—	—	—	IOC	Y	—
RC5	5	2	—	—	OPA2IN+	—	—	CCP1 ⁽¹⁾	—	IOC	Y	—
RC6	8	5	AN8	—	—	—	—	—	SS ⁽¹⁾	IOC	Y	—
RC7	9	6	AN9	—	—	—	—	—	—	IOC	Y	—
V _{DD}	1	18	—	—	—	—	—	—	—	—	—	V _{DD}
V _{SS}	20	17	—	—	—	—	—	—	—	—	—	V _{SS}
OUT ⁽²⁾	—	—	—	—	—	—	—	CPP1	SDA ⁽³⁾	—	—	—
	—	—	—	—	—	—	—	CPP2	SCL ⁽³⁾ SCK	—	—	—
—	—	—	—	—	—	—	—	—	SDO	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1708/9)

I/O(2)	PDI/SOIC/ SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	19	16	AN0	VREF-	C1IN+	—	DAC1OUT	—	—	—	—	—	—	—	—	IOC	Y	IOSPDAT
RA1	18	15	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	IOSPCLK
RA2	17	14	AN2	—	—	—	DAC1OUT2	ZCD	T0CK1(1)	—	—	COG1N(1)	—	—	—	INT1(1) IOC	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	MCLR VPP
RA4	3	20	AN3	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	19	—	—	—	—	—	—	T1CK1 SOSCI	—	—	—	—	—	CLC1N3(1)	IOC	Y	CLKIN OSC1
RB4	13	10	AN10	—	—	OPA1IN-	—	—	—	—	—	—	—	—	—	IOC	Y	—
RB5	12	9	AN11	—	—	OPA1IN+	—	—	—	—	—	—	—	—	—	IOC	Y	—
RB6	11	8	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RB7	10	7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC0	16	13	AN4	—	C2IN+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	AN5	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	CLC1N2(1)	IOC	Y	—
RC2	14	11	AN6	—	C1IN2- C2IN2-	OPA1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC3	7	4	AN7	—	C1IN3- C2IN3-	OPA2OUT	—	—	—	CCP2(1)	—	—	—	—	CLC1N0(1)	IOC	Y	—
RC4	6	3	—	—	—	OPA2IN-	—	—	—	—	—	—	—	—	CLC1N1(1)	IOC	Y	—
RC5	5	2	—	—	—	OPA2IN+	—	—	—	CCP1(1)	—	—	—	—	—	IOC	Y	—
RC6	8	5	AN8	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC7	9	6	AN9	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 - 2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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I/O ⁽²⁾	PDI/SOIC/ SSOP	QFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
OUT ⁽²⁾	—	—	—	—	C1OUT	—	—	—	—	GPP1	PWM3OUT	COGA	SDA ⁽³⁾	CK	CLC1OUT	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	GPP2	PWM4OUT	COGB	SCL ⁽³⁾	DT	CLC2OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGC	SDO	TX	CLC3OUT	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	COGD	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Any pin can be selected as a peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 5: 28-PIN ALLOCATION TABLE (PIC16L(F)1713/6/8) (PART 1)

I/O ⁽²⁾	PDI ⁽³⁾ , SIOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	2	27	AN0		C1IN0- C2IN0-											CLCIN0 ⁽¹⁾	IOC	Y	
RA1	3	28	AN1		C1IN1- C2IN1-	OPA1OUT										CLCIN1 ⁽¹⁾	IOC	Y	
RA2	4	1	AN2	Vref	C1IN0+ C2IN0+		DAC1OUT1										IOC	Y	
RA3	5	2	AN3	Vref+	C1IN1+												IOC	Y	
RA4	6	3				OPA1IN+			T0CK ⁽¹⁾								IOC	Y	
RA5	7	4	AN4			OPA1IN-	DAC2OUT1							nSS ⁽¹⁾			IOC	Y	OSC2 CLKOUT OSC1 CLKIN
RA6	10	7															IOC		
RA7	9	6									NCOCLK						IOC		
RB0	21	18	AN12		C2IN1+			ZCD					COGIN ⁽¹⁾				INT ⁽¹⁾ IOC		
RB1	22	19	AN10		C1IN3- C2IN3-	OPA2OUT											IOC		
RB2	23	20	AN8			OPA2IN-											IOC		
RB3	24	21	AN9		C1IN2- C2IN2-	OPA2IN+											IOC		
RB4	25	22	AN11														IOC	Y	
RB5	26	23	AN13						T1G ⁽¹⁾								IOC	Y	
RB6	27	24												SCL ⁽¹⁾		CLCIN2 ⁽¹⁾	IOC	Y	ICSPCLK
RB7	28	25					DAC1OUT2 DAC2OUT2									CLCIN3 ⁽¹⁾	IOC	Y	ICSPDAT
RC0	11	8							T1CK ⁽¹⁾ SOSCO								IOC	Y	
RC1	12	9							SOSCI	CCP2 ⁽¹⁾							IOC	Y	
RC2	13	10	AN14							CCP1 ⁽¹⁾							IOC	Y	
RC3	14	11	AN15											SCK ⁽¹⁾			IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

PIC16(L)F170X/171X

TABLE 6: 28-PIN ALLOCATION TABLE (PIC16L(F)1713/6/8) (PART 2)

I/O ⁽²⁾	PDIP, SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RC4	15	12	AN16											SDI ⁽¹⁾			IOC	Y	
RC5	16	13	AN17											SDA ⁽¹⁾					
RC6	17	14	AN18												CK ⁽³⁾		IOC	Y	
RC7	18	15	AN19												RX ⁽³⁾		IOC	Y	
RE3	1	26															IOC	Y	
Vdd	20	17																	MCLR
Vss	8	5																	Vpp
	19	16																	Vdd
																			Vss
OUT ⁽⁴⁾					C1OUT					CCP1	NCOOUT	PWM3OUT	COGA	SDA ⁽³⁾	TX/CK	CLC1OUT			
					C2OUT					CCP2		PWM4OUT	COGB	SCK/SCL ⁽³⁾	DT ⁽³⁾	CLC2OUT			
IN ⁽⁵⁾									T1G	CCP1	NCCLK		COGC	SCK/SCL ⁽³⁾	RX ⁽³⁾	CLC3OUT	CLCIN3		
									T1CKI				COGD			CLCIN2			
									T0CKI							CLCIN1			
																CLCIN0			

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

Note 4: Alternate outputs are excluded from solid shaded areas.

Note 5: Alternate inputs are excluded from dot shaded areas.

TABLE 7: PIN ALLOCATION TABLE (PIC16L(F)1717/9) (PART 1)

I/O ⁽²⁾	PDIP	TQFP	UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pullup	Basic
RA0	2	19	17	AN0		C1IN0- C2IN0-											CLCIN0 ⁽¹⁾	IOC	Y	
RA1	3	20	18	AN1		C1IN1- C2IN1-	OPA1OUT										CLCIN1 ⁽¹⁾	IOC	Y	
RA2	4	21	19	AN2	Vref	C1IN0+ C2IN0+		DAC1OUT1										IOC	Y	
RA3	5	22	20	AN3	Vref+	C1IN1+												IOC	Y	
RA4	6	23	21				OPA1IN+											IOC	Y	
RA5	7	24	22	AN4			OPA1IN-	DAC2OUT1								nSS ⁽¹⁾		IOC	Y	
RA6	14	31	29															IOC		OSC2 CLKOUT
RA7	13	30	28									NCOCLK						IOC		OSC1 CLKIN
RB0	33	8	8	AN12		C2IN1+			ZCD									INT ⁽¹⁾		
RB1	34	9	9	AN10		C1IN3- C2IN3-	OPA2OUT											IOC		
RB2	35	10	10	AN8			OPA2IN-											IOC		
RB3	36	11	11	AN9		C1IN2- C2IN2-	OPA2IN+											IOC		
RB4	37	14	12	AN11														IOC	Y	
RB5	38	15	13	AN13														IOC	Y	
RB6	39	16	14														CLCIN2 ⁽¹⁾	IOC	Y	ICSPCLK
RB7	40	17	15					DAC1OUT2 DAC2OUT2									CLCIN3 ⁽¹⁾	IOC	Y	ICSPDAT
RC0	15	32	30															IOC	Y	
RC1	16	35	31															IOC	Y	
RC2	17	36	32	AN14														IOC	Y	
RC3	18	37	33	AN15														IOC	Y	
RC4	23	42	38	AN16														IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
Note 2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
Note 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
Note 4: Alternate outputs are excluded from solid shaded areas.

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