Maximum Ratings (1)

Supply Voltage
- V_{DD} ..... -0.5V to +4.6V
- REF ..... -0.5V to +4.6V

Input Current ..... -50mA
Output Current ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... +260°C
Storage Temperature (Ts) ..... -65°C to +150°C
Junction Temperature ..... +150°C

Operation Ratings(2)

Supply Voltage
- V_{DD} ..... +3.0V to +3.6V
- V_{DD} ..... +2.375V to +2.625V

Operating Temperature (industrial) ..... -40°C to +85°C
Package Thermal Resistance (2)
θJA
- Still-Air ..... 157°C/W

θJB
- Junction-to-Board ..... 42°C

Notes:

1. Stresses greater then those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. θJA and θJB values are determined for a 4-layer board in still-air, unless otherwise stated.

DC Electrical Characteristics

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{IL}	Input LOW Voltage	V_{DD} = 3.3V			0.8	V
		V_{DD} = 2.5V			0.7	
V_{IH}	Input HIGH Voltage	V_{DD} = 3.3V		2.0		
		V_{DD} = 2.5V		1.7		
I_{IL}	Input LOW Current	V_{IN} = 0V			10	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			100	
V_{OL}	Output LOW Voltage	I_{OL} = 12mA	V_{DD} = 3.3V		0.25	V
			V_{DD} = 2.5V		0.35	
V_{OH}	Output HIGH Voltage	V_{DD} = 2.5V, I_{OH} = –12mA		1.9		
		V_{DD} = 3.3V, I_{OH} = –12mA		2.55		
I_{DD}	Supply Current	Unloaded outputs 66 MHz			22	mA

AC Electrical Characteristics

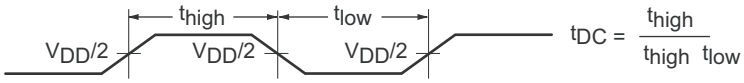
Parameter	Description	Test Conditions		Min.	Typ.	Max.	Units
F_O	Output Frequency	V_{DD} = 2.5V, C_L = 15pF		10		200	MHz
		V_{DD} = 3.3V, C_L = 15pF		10		220	MHz
BW	Bandwidth for PLL	V_{DD} = 2.5V			0.8		MHz
		V_{DD} = 3.3V			1.5		
t_{DC}	Duty Cycle(1)(4)	Measured at V_{DD}/2, 10pF load		45	50	55	%
t_R	Rise Time(1)(4)	For 3.3V: Measured between 0.8V and 2.0V @ 10pF				1	ns
		For 2.5V: Measured between 0.6V and 1.8V @ 10pF				1.8	
t_F	Fall Time(1)(4)	For 3.3V: Measured between 0.8V and 2.0V @ 10pF				1	
		For 2.5V: Measured between 0.6V and 1.8V @ 10pF				1.8	
$t_{sk(o)}$	Output to Output Skew(2)	All outputs equally loaded	V_{DD} = 3.3V			90	ps
			V_{DD} = 2.5V			90	
t_0	Delay, REF Rising Edge to CLKOUT Rising Edge(2)	Measured at V_{DD}/2 @ 66MHz	V_{DD} = 3.3V	-100		100	
			V_{DD} = 2.5V	-200		200	
$t_{SK(D)}$	Device-to-device Skew(3)	Measured at V_{DD}/2 on CLKx pins of device		-300		+300	
t_{JIT}	Cycle-to-Cycle Jitter	15pF load, >66MHz, standard drive	V_{DD} = 3.3V		47	110	ps
			V_{DD} = 2.5V		42	90	
		15pF load, >66MHz, high drive	V_{DD} = 3.3V		45	100	
			V_{DD} = 2.5V		40	80	
		30pF load, >66MHz, standard drive	V_{DD} = 3.3V		63	120	
			V_{DD} = 2.5V		83	130	
		30pF load, >66MHz, high drive	V_{DD} = 3.3V		51	115	
			V_{DD} = 2.5V		66	115	
t_{PJ}	Period Jitter (Peak)	15pF load, >66MHz, standard drive	V_{DD} = 3.3V		39	90	ps
			V_{DD} = 2.5V		28	60	
		15pF load, >66MHz, high drive	V_{DD} = 3.3V		39	85	
			V_{DD} = 2.5V		27	55	
		30pF load, >66MHz, standard drive	V_{DD} = 3.3V		48	85	
			V_{DD} = 2.5V		75	90	
		30pF load, >66MHz, high drive	V_{DD} = 3.3V		43	75	
			V_{DD} = 2.5V		60	80	
t_{LOCK}	PLL Lock Time (1)	Stable power supply, valid clocks presented on REF pin				1.0	ms

Note:

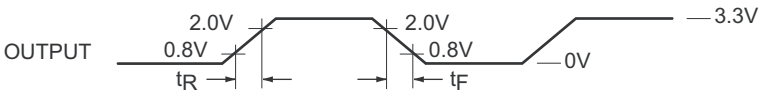
1. See Switching Waveforms
2. All clock output should have the same loading to achieve zero delay between the input and outputs and zero output-to-output skew. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-to-output delay. If input-to-output delay adjustments are needed, the CLKOUT load may be changed to vary the delay between the REF input to the clock outputs. Output-to-output skew includes CLK 1-4.
3. Specifications are guaranteed by design and not production tested.
4. Measured at 100MHz.

Switching Waveforms

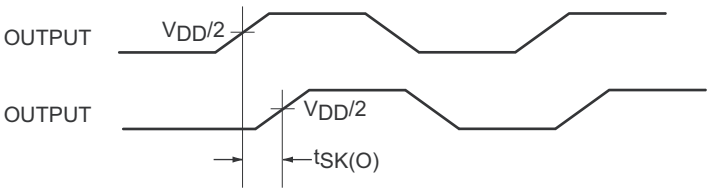
Duty Cycle Timing



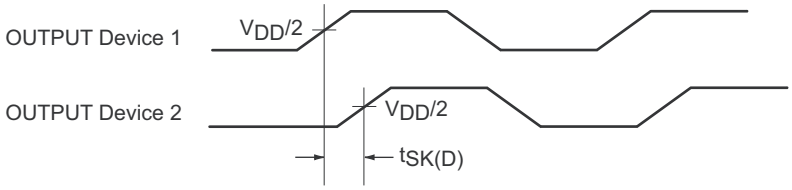
All Outputs Rise/Fall Time



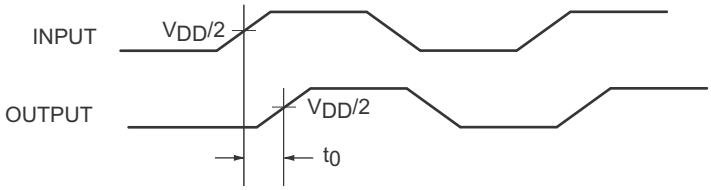
Output-Output Skew



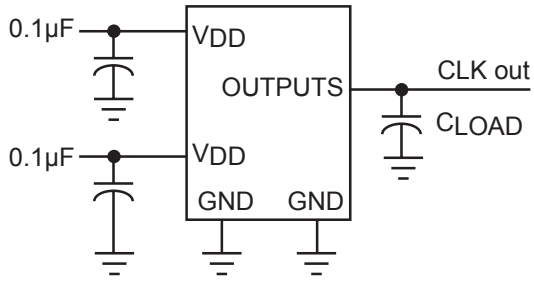
Device-Device Skew



Input-Output Propagation Delay

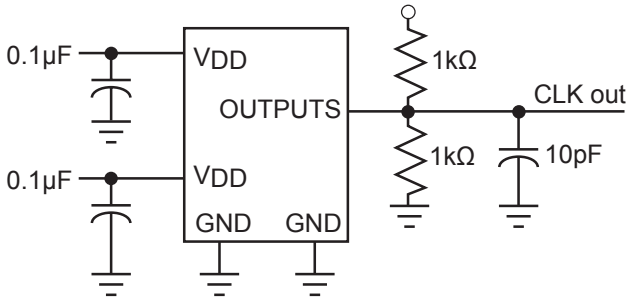


Test Circuit 1



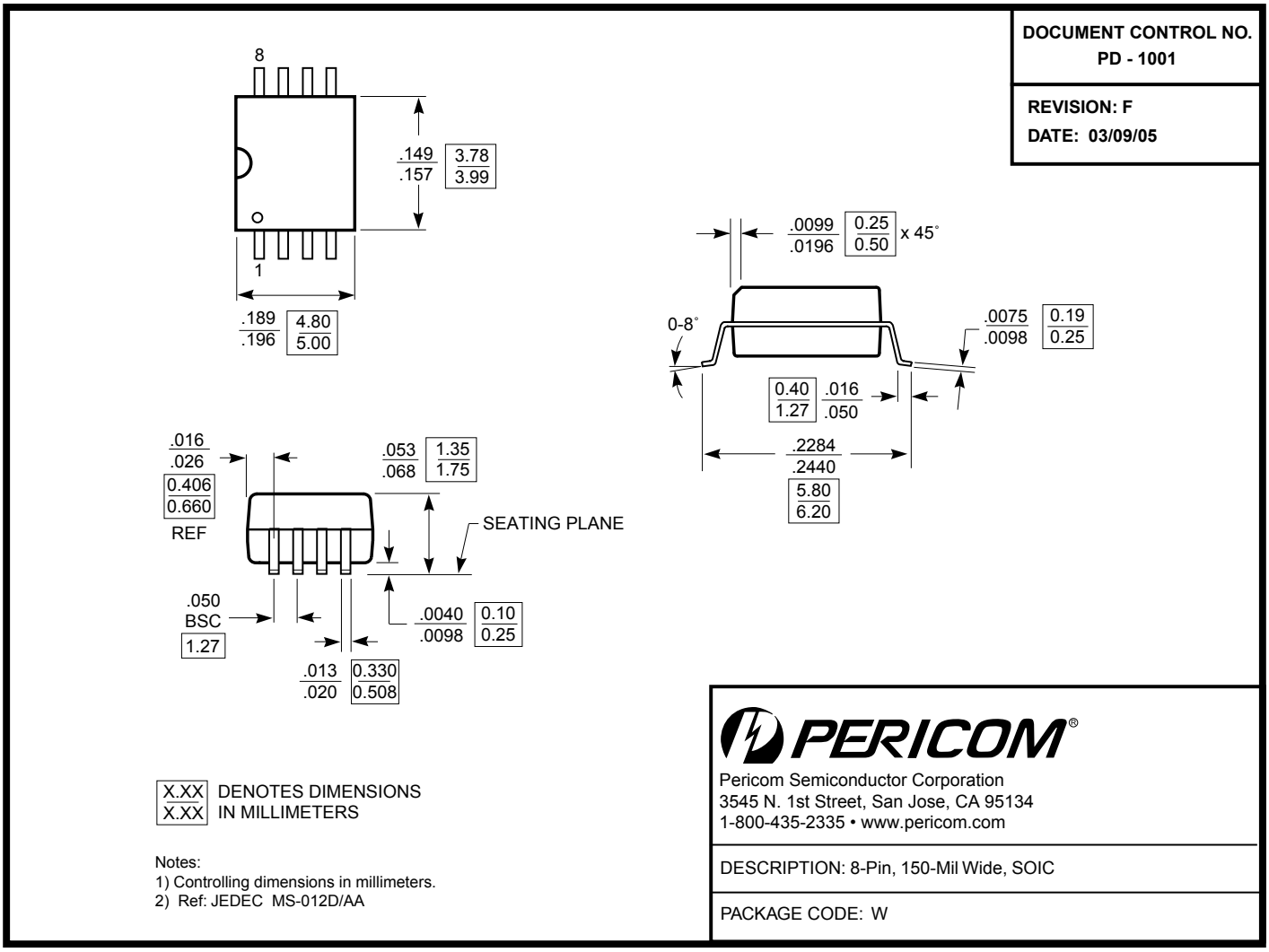
Test Circuit for all parameters except t_{SLEW}

Test Circuit 2



Test Circuit for t_{SLEW} ,Output slew

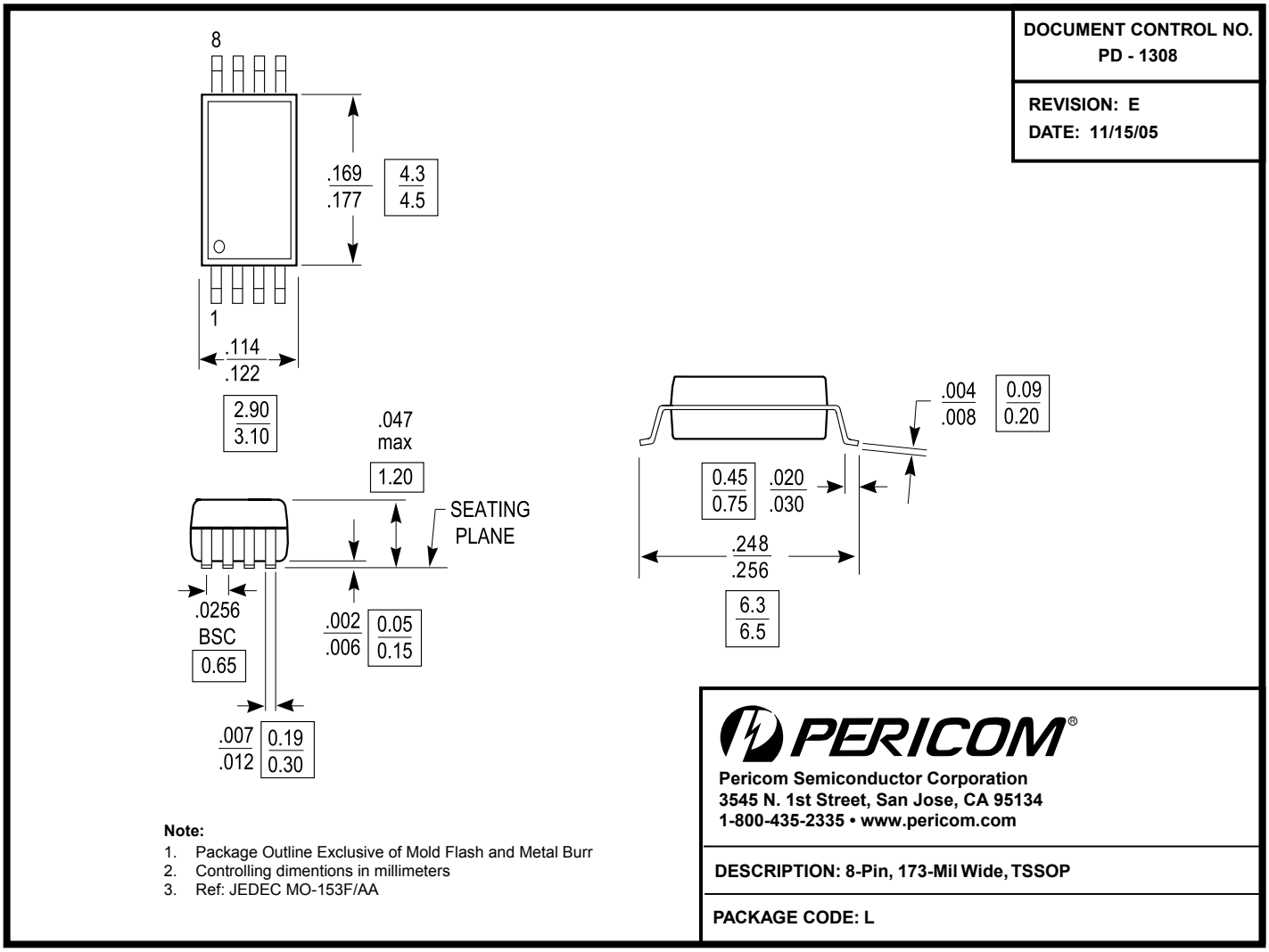
Packaging Mechanical: 8-pin SOIC (W)



Note:

• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Packaging Mechanical: 8-pin TSSOP (L)



Note:
• For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information(1,2,3)

Ordering Code	Package Code	Package Description
PI6C22405-1HWE	W	Pb-free & Green, 8-pin SOIC
PI6C22405-1HWIE	W	Pb-free & Green, 8-pin SOIC, Industrial temp range
PI6C22405-1HLE	L	Pb-free & Green, 8-pin TSSOP
PI6C22405-1HLIE	L	Pb-free & Green, 8-pin TSSOP, Industrial temp range

Notes:
1. Latest Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. Adding an X suffix = Tape/Reel