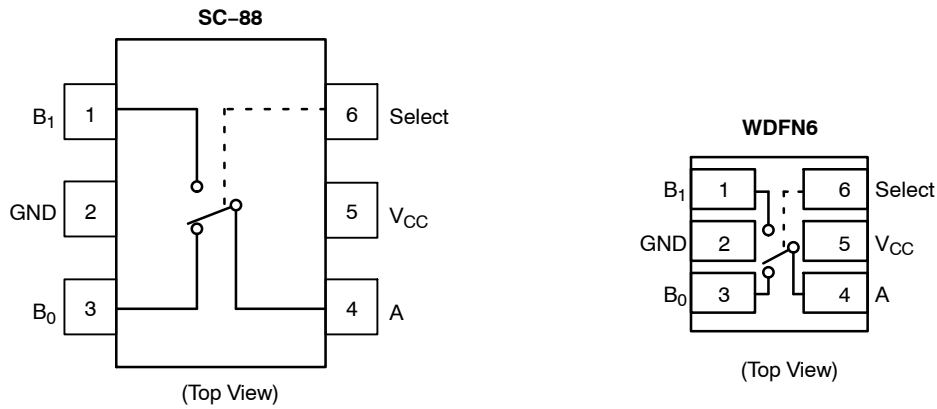


# NLASB3157



**Figure 1. Pin Assignment & Logic Diagram**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.5 to +7.0	V
DC Switch Voltage (Note 1)	$V_{IS}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Voltage (Note 1)	$V_{IN}$	-0.5 to + 7.0	V
DC Input Diode Current @ $V_{IN} < 0$ V	$I_{IK}$	-50	mA
DC Output Current	$I_{OUT}$	128	mA
DC $V_{CC}$ or Ground Current	$I_{CC}/I_{GND}$	+100	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Junction Temperature Under Bias	$T_J$	150	°C
Junction Lead Temperature (Soldering, 10 Seconds)	$T_L$	260	°C
Power Dissipation @ +85°C	$P_D$	180	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS (Note 2)

Characteristic	Symbol	Min	Max	Unit
Supply Voltage Operating	$V_{CC}$	1.65	5.5	V
Select Input Voltage	$V_{IN}$	0	5.5	V
Switch Input Voltage	$V_{IS}$	0	$V_{CC}$	V
Output Voltage	$V_{OUT}$	0	$V_{CC}$	V
Operating Temperature	$T_A$	-55	+125	°C
Input Rise and Fall Time Control Input $V_{CC} = 2.3$ V–3.6 V Control Input $V_{CC} = 4.5$ V–5.5 V	$t_r, t_f$	0 0	10 5.0	ns/V
Thermal Resistance	$\theta_{JA}$	–	350	°C/W

2. Select input must be held HIGH or LOW, it must not float.

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## DC ELECTRICAL CHARACTERISTICS – NLASB3157

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = –40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub>		V
V <sub>IL</sub>	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub>	V
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0–5.5		± 0.05	± 0.1		± 1	μA
I <sub>OFF</sub>	OFF State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	1.65–5.5		± 0.05	± 0.1		± 1	μA
R <sub>ON</sub>	Switch On Resistance (Note 3)	V <sub>IN</sub> = 0 V, I <sub>O</sub> = 30 mA	4.5		3.0			7.0	Ω
		V <sub>IN</sub> = 2.4 V, I <sub>O</sub> = –30 mA			5.0			12	
		V <sub>IN</sub> = 4.5 V, I <sub>O</sub> = –30 mA			7.0			15	
		V <sub>IN</sub> = 0 V, I <sub>O</sub> = 24 mA	3.0		4.0			9.0	Ω
		V <sub>IN</sub> = 3 V, I <sub>O</sub> = –24 mA			10			20	
		V <sub>IN</sub> = 0 V, I <sub>O</sub> = 8 mA	2.3		5.0			12	Ω
		V <sub>IN</sub> = 2.3 V, I <sub>O</sub> = –8 mA			13			30	
		V <sub>IN</sub> = 0 V, I <sub>O</sub> = 4 mA	1.65		6.5			20	Ω
		V <sub>IN</sub> = 1.65 V, I <sub>O</sub> = –4 mA			17			50	
I <sub>CC</sub>	Quiescent Supply Current All Channels ON or OFF	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0	5.5			1.0		10	μA
	Analog Signal Range		V <sub>CC</sub>	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V
R <sub>RANGE</sub>	On Resistance Over Signal Range (Note 3) (Note 7)	I <sub>A</sub> = –30 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	4.5					25	Ω
		I <sub>A</sub> = –24 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.0					50	
		I <sub>A</sub> = –8 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.3					100	
		I <sub>A</sub> = –4 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.65					300	
ΔR <sub>ON</sub>	On Resistance Match Between Channels (Note 3) (Note 4) (Note 5)	I <sub>A</sub> = –30 mA, V <sub>Bn</sub> = 3.15	4.5		0.15				Ω
		I <sub>A</sub> = –24 mA, V <sub>Bn</sub> = 2.1	3.0		0.2				
		I <sub>A</sub> = –8 mA, V <sub>Bn</sub> = 1.6	2.3		0.5				
		I <sub>A</sub> = –4 mA, V <sub>Bn</sub> = 1.15	1.65		0.5				
R <sub>flat</sub>	On Resistance Flatness (Note 3) (Note 4) (Note 6)	I <sub>A</sub> = –30 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	5.0		6.0				Ω
		I <sub>A</sub> = –24 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.3		12				
		I <sub>A</sub> = –8 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.5		28				
		I <sub>A</sub> = –4 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.8		125				

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

4. Parameter is characterized but not tested in production.

5. ΔR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> min measured at identical V<sub>CC</sub>, temperature and voltage levels.

6. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

7. Guaranteed by Design.

# NLASB3157

## AC ELECTRICAL CHARACTERISTICS – NLASB3157

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = –40°C to +85°C		Unit	Figure Number
				Min	Typ	Max	Min	Max		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Bus to Bus (Note 9)	V <sub>I</sub> = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					1.2 0.8 0.3	ns	Figures 2, 3
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time Turn On Time (A to B <sub>n</sub> )	V <sub>I</sub> = 2 × V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> = 0 V for t <sub>PZH</sub>	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 7.6 5.7	ns	Figures 2, 3
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time Turn Off Time (A Port to B Port)	V <sub>I</sub> = 2 × V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> = 0 V for t <sub>PHZ</sub>	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 5.3 3.8	ns	Figures 2, 3
t <sub>B–M</sub>	Break Before Make Time (Note 8)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4
Q	Charge Injection (Note 8)	C <sub>L</sub> = 0.1 nF, V <sub>GEN</sub> = 0 V R <sub>GEN</sub> = 0 Ω	5.0 3.3		7.0 3.0				pC	Figure 5
OIRR	Off Isolation (Note 10)	R <sub>L</sub> = 50 Ω f = 10 MHz	1.65–5.5		–57				dB	Figure 6
Xtalk	Crosstalk	R <sub>L</sub> = 50 Ω f = 10 MHz	1.65–5.5		–54				dB	Figure 7
BW	–3 dB Bandwidth	R <sub>L</sub> = 50 Ω	1.65–5.5		250				MHz	Figure 10
THD	Total Harmonic Distortion (Note 8)	R <sub>L</sub> = 600 Ω 0.5 V <sub>P–P</sub> f = 600 Hz to 20 kHz	5.0		0.011				%	

## CAPACITANCE – NLASB3157 (Note 11)

Symbol	Parameter	Test Conditions	Typ	Max	Unit	Figure Number
C <sub>IN</sub>	Select Pin Input Capacitance	V <sub>CC</sub> = 0 V	2.3		pF	
C <sub>IO–B</sub>	B Port Off Capacitance	V <sub>CC</sub> = 5.0 V	6.5		pF	Figure 8
C <sub>IOA–ON</sub>	A Port Capacitance when Switch is Enabled	V <sub>CC</sub> = 5.0 V	18.5		pF	Figure 9

8. Guaranteed by Design.

9. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

10. Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub>/V<sub>Bn</sub>].

11. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

APPENDIX A

DC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		1.65–1.95 2.3–5.5				0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub>		V
V <sub>IL</sub>	LOW Level Input Voltage		1.65–1.95 2.3–5.5					0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub>	V
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0–5.5		± 0.05	± 0.1		± 1	μA
I <sub>OFF</sub>	OFF State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	1.65–5.5		± 0.05	± 0.1		± 1	μA
R <sub>ON</sub>	Switch On Resistance (Note 12)	V <sub>IN</sub> = 0 V, I <sub>O</sub> = 30 mA V <sub>IN</sub> = 2.4 V, I <sub>O</sub> = -30 mA V <sub>IN</sub> = 4.5 V, I <sub>O</sub> = -30 mA	4.5		3.0 5.0 7.0			8.5 13.0 15.0	Ω
		V <sub>IN</sub> = 0 V, I <sub>O</sub> = 24 mA V <sub>IN</sub> = 3 V, I <sub>O</sub> = -24 mA	3.0		4.0 10			11 20	
		V <sub>IN</sub> = 0 V, I <sub>O</sub> = 8 mA V <sub>IN</sub> = 2.3 V, I <sub>O</sub> = -8 mA	2.3		5.0 13			12 30	
		V <sub>IN</sub> = 0 V, I <sub>O</sub> = 4 mA V <sub>IN</sub> = 1.65 V, I <sub>O</sub> = -4 mA	1.65		6.5 17			20 50	
I <sub>CC</sub>	Quiescent Supply Current All Channels ON or OFF	V <sub>IN</sub> = V <sub>CC</sub> or GND  I <sub>OUT</sub> = 0	5.5			1.0		10	μA
	Analog Signal Range		V <sub>CC</sub>	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V
R <sub>RANGE</sub>	On Resistance Over Signal Range (Note 12) (Note 14)	I <sub>A</sub> = -30 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	4.5					25	Ω
		I <sub>A</sub> = -24 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.0					50	
		I <sub>A</sub> = -8 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.3					100	
		I <sub>A</sub> = -4 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.65					300	

12. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

13. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

14. Guaranteed by Design.

\* For ΔR<sub>ON</sub>, R<sub>FLAT</sub>, Q, OIRR, Xtalk, BW, THD, and CIN see -40°C to 85°C section.

APPENDIX A

AC ELECTRICAL EXTENDED AUTOMOTIVE TEMPERATURE RANGE CHARACTERISTICS – NLVASB3157

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -55°C to +125°C		Unit	Figure Number
				Min	Typ	Max	Min	Max		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Bus to Bus (Note 16)	V <sub>I</sub> = OPEN	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5					1.2 0.8 0.3	ns	Figures 2, 3
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time Turn On Time (A to B <sub>n</sub> )	V <sub>I</sub> = 2 × V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> = 0 V for t <sub>PZH</sub>	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			23 13 6.9 5.2	7.0 3.5 2.5 1.7	24 14 9.0 7.0	ns	Figures 2, 3
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time Turn Off Time (A Port to B Port)	V <sub>I</sub> = 2 × V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> = 0 V for t <sub>PHZ</sub>	1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5			12.5 7.0 5.0 3.5	3.0 2.0 1.5 0.8	13 7.5 6.5 5.0	ns	Figures 2, 3
t <sub>B-M</sub>	Break Before Make Time (Note 15)		1.65–1.95 2.3–2.7 3.0–3.6 4.5–5.5				0.5 0.5 0.5 0.5		ns	Figure 4

15. Guaranteed by Design.

16. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

\* For ΔR<sub>ON</sub>, R<sub>FLAT</sub>, Q, OIRR, Xtalk, BW, THD, and CIN see -40°C to 85°C section.

# AC LOADING AND WAVEFORMS

NOTE: Input driven by 50  $\Omega$  source terminated in 50  $\Omega$   
 NOTE:  $C_L$  includes load and stray capacitance  
 NOTE: Input PRR = 1.0 MHz;  $t_W$  = 500 ns

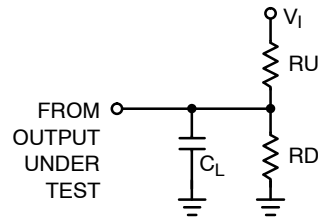


Figure 2. AC Test Circuit

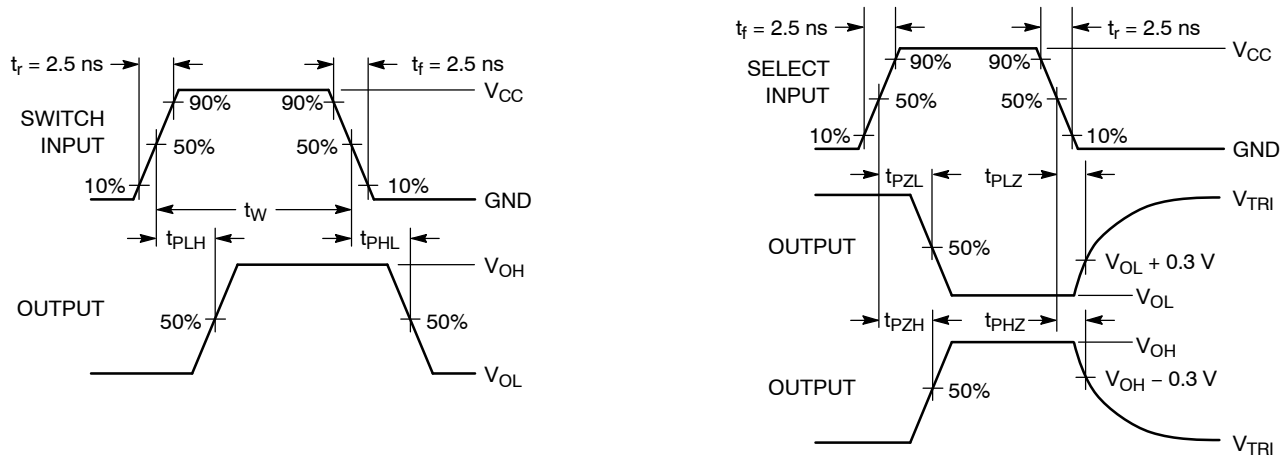


Figure 3. AC Waveforms



Figure 4. Break Before Make Interval Timing

# AC LOADING AND WAVEFORMS

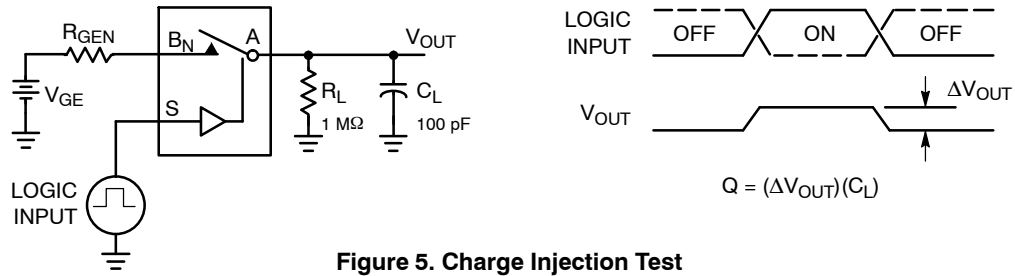


Figure 5. Charge Injection Test

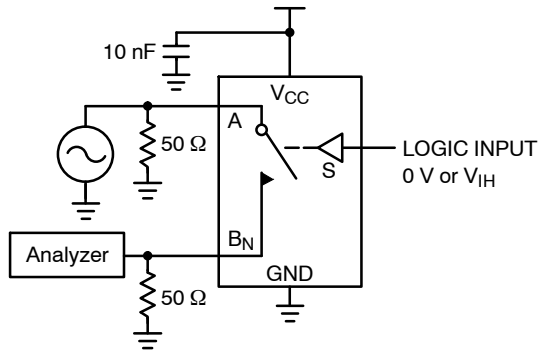


Figure 6. Off Isolation

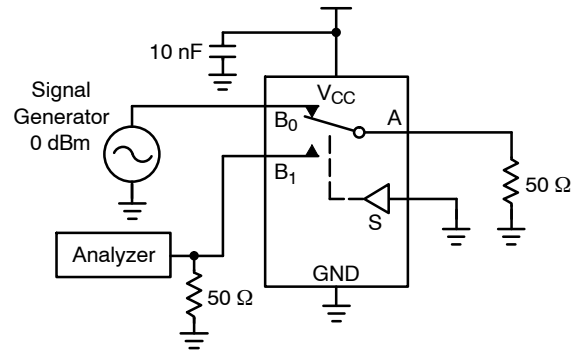


Figure 7. Crosstalk

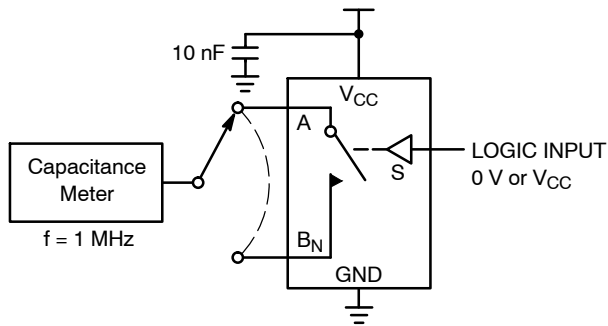


Figure 8. Channel Off Capacitance

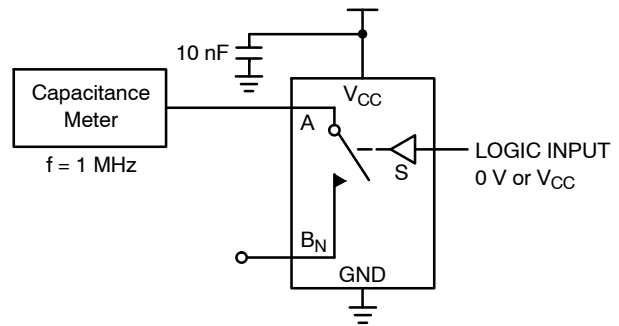


Figure 9. Channel On Capacitance

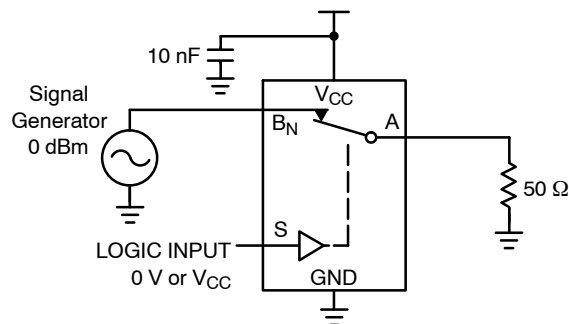


Figure 10. Bandwidth





