FAIRCHILD SEMICONDUCTOR®

February 2008

MM74HC125, MM74HC126 3-STATE Quad Buffers

Features

- Typical propagation delay: 13ns
- Wide operating voltage range: 2V–6V
- Low input current: 1µA maximum
- Low quiescent current: 80µA maximum (74HC)
- Fanout of 15 LS-TTL loads

General Description

The MM74HC125 and MM74HC126 are general purpose 3-STATE high speed non-inverting buffers utilizing advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM74HC125 require the 3-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM74HC126 require the control input to be low to put the output into high impedance.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Ordering Information

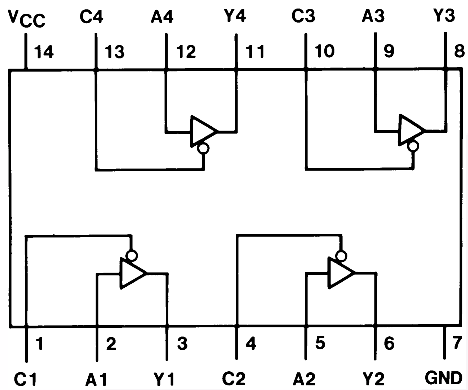
Order Number	Package Number	Package Description
MM74HC125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC125N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC126M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC126SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC126MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC126N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

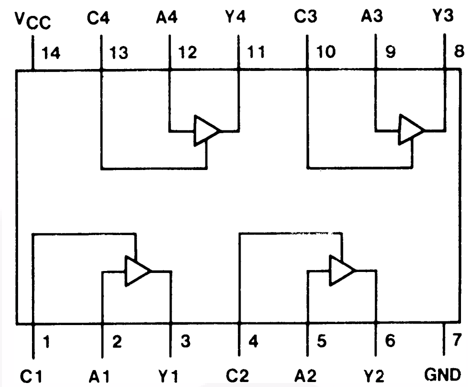
All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View (MM74HC125)



Top View (MM74HC126)

Truth Tables

Inputs		Output
A	**C**	**Y**
H	L	H
L	L	L
X	H	Z

MM74HC125

Inputs		Output
A	**C**	**Y**
H	H	H
L	H	L
X	L	Z

MM74HC126

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC}+1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	35mA
I_{CC}	DC V_{CC} or GND Current, per pin	±70mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:
1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics[3]

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$		$T_A = -40°C$ to 85°C	$T_A = -40°C$ to 125°C	Units
				Typ.	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0		1.5	1.5	1.5	V
			4.5		3.15	3.15	3.15	
			6.0		4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage		2.0		0.5	0.5	0.5	V
			4.5		1.35	1.35	1.35	
			6.0		1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT}\rvert \le 20\mu A$	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
			6.0	6.0	5.9	5.9	5.9	
		$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT}\rvert \le 6.0mA$	4.5	4.2	3.98	3.84	3.7	
		$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT}\rvert \le 7.8mA$	6.0	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT}\rvert \le 20\mu A$	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
			6.0	0	0.1	0.1	0.1	
		$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT}\rvert \le 6.0mA$	4.5	0.2	0.26	0.33	0.4	
		$V_{IN} = V_{IH}$ or V_{IL}, $\lvert I_{OUT}\rvert \le 7.8mA$	6.0	0.2	0.26	0.33	0.4	
I_{OZ}	Maximum 3-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or V_{IL}, $V_{OUT} = V_{CC}$ or GND, C_n = Disabled	6.0		±0.5	±5	±10	µA
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	6.0		8.0	80	160	µA

Note:

3. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $C_L = 45pF$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to HIGH Level	$R_L = 1k\Omega$	13	25	ns
t_{PHZ}	Maximum Output Disable Time from HIGH Level	$R_L = 1k\Omega$, $C_L = 5pF$	17	25	ns
t_{PZL}	Maximum Output Enable Time to LOW Level	$R_L = 1k\Omega$	18	25	ns
t_{PLZ}	Maximum Output Disable Time from LOW Level	$R_L = 1k\Omega$, $C_L = 5pF$	13	25	ns

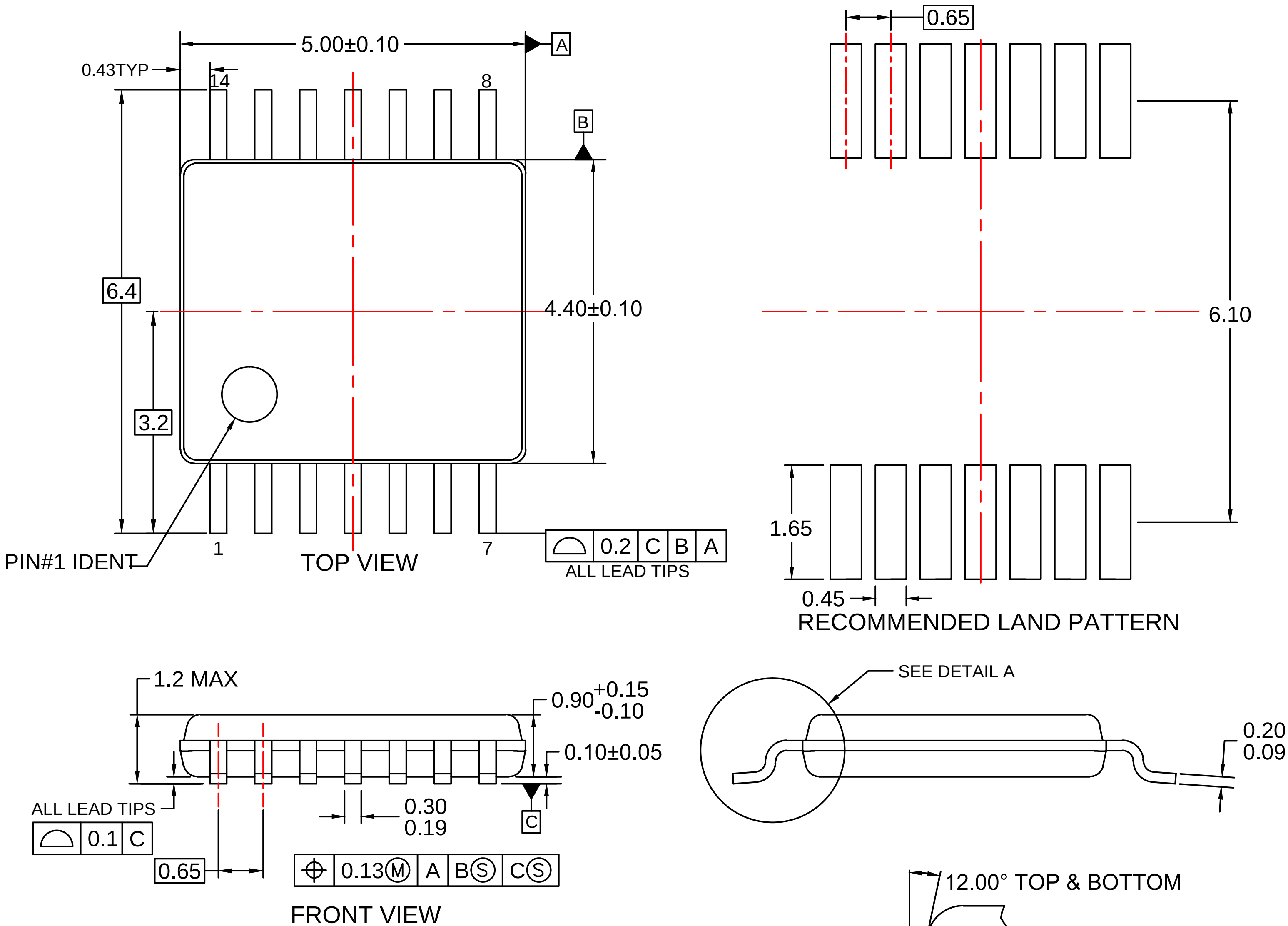
AC Electrical Characteristics

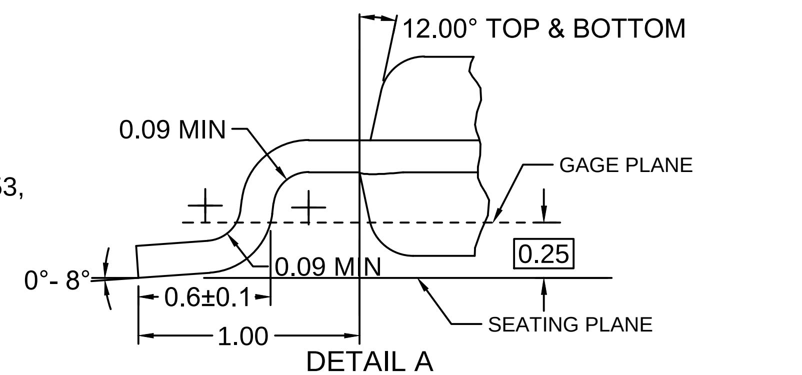
$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50pF$, $t_r = t_f = 6ns$ (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25°C$		$T_A = –40°C$ to 85°C	$T_A = –40°C$ to 125°C	Units
				Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	2.0		40	100	125	150	ns
		4.5		14	20	25	30	
		6.0		12	17	21	25	
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	2.0	$C_L = 150pF$	35	130	163	195	ns
		4.5		14	26	33	39	
		6.0		12	22	28	39	
t_{PZH}, t_{PZL}	Maximum Output Enable Time	2.0	$R_L = 1k\Omega$	25	125	156	188	ns
		4.5		14	25	31	38	
		6.0		12	21	26	31	
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	2.0	$R_L = 1k\Omega$	25	125	156	188	ns
		4.5		14	25	31	38	
		6.0		12	21	26	31	
t_{PZL}, t_{PZH}	Maximum Output Enable Time	2.0	$C_L = 150pF$, $R_L = 1k\Omega$	35	140	175	210	ns
		4.5		15	28	35	42	
		6.0		13	24	30	36	
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	2.0V	$C_L = 50pF$	30	60	75	90	ns
		4.5V		7	12	15	18	
		6.0V		6	10	13	15	
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (per gate)[4]		Enabled	45				pF
			Disabled	6				

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

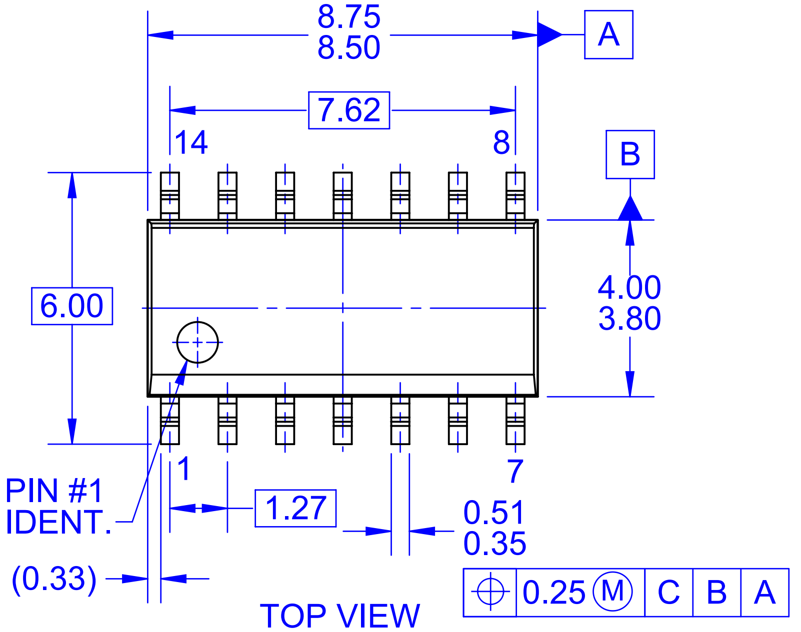
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

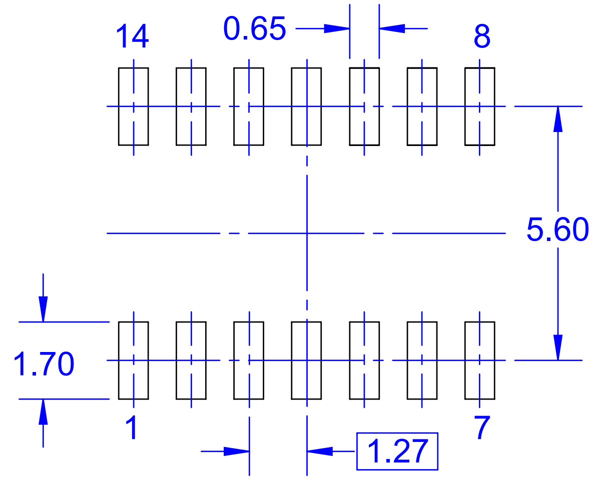
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

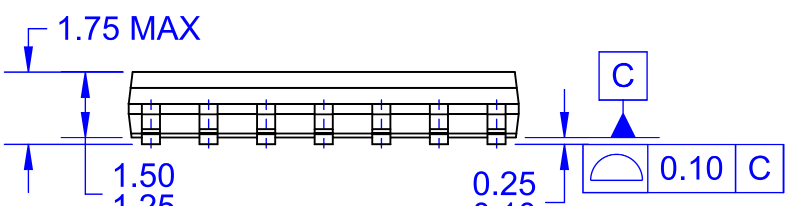
F. DRAWING FILE NAME: MKT-MTC14rev7.



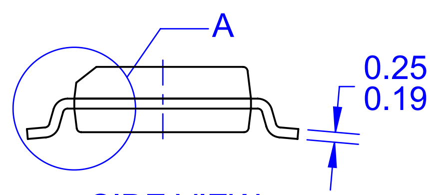
TOP VIEW



LAND PATTERN RECOMMENDATION



FRONT VIEW

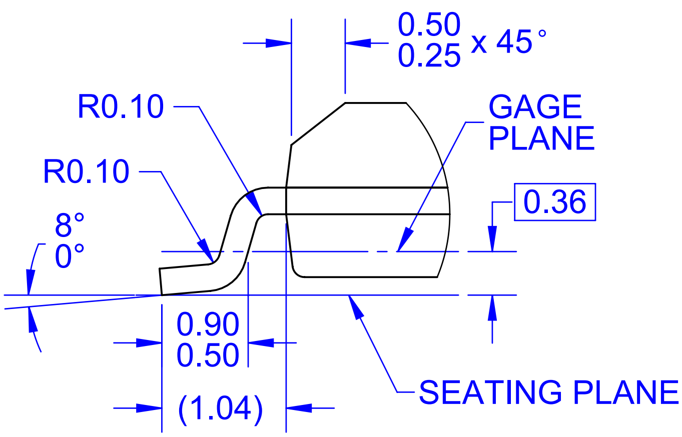


SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

FAIRCHILD ™



DETAIL A
SCALE 16 : 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative