ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	260	−	Vdc
Collector Cutoff Current (V_{CB} = 260 Vdc, I_E = 0)	I_{CBO}	−	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	−	5	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non−repetitive))	$I_{S/b}$	 4 1	 − −	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc) (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc)	h_{FE}	 75 75 75 75 45	 150 150 150 150 −	
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	−	3	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	30	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	600	pF

TYPICAL CHARACTERISTICS

PNP MJL1302A

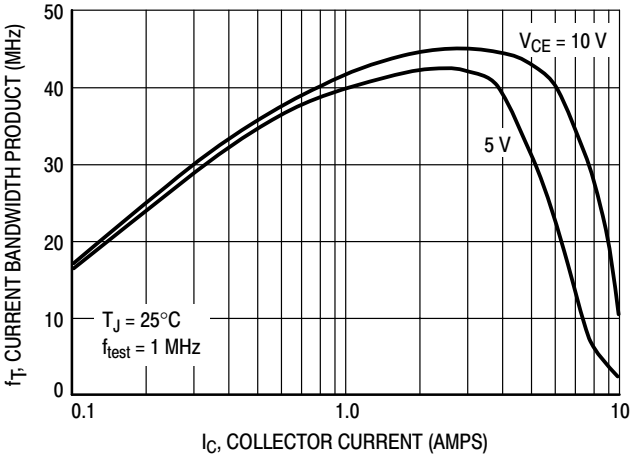

Figure 1. Typical Current Gain Bandwidth Product

NPN MJL3281A

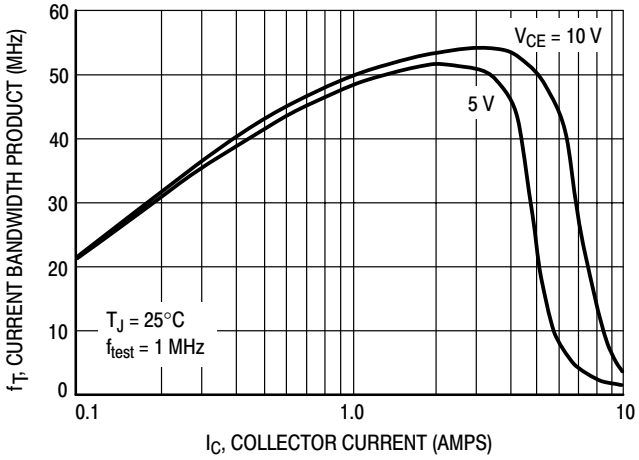

Figure 2. Typical Current Gain Bandwidth Product

PNP MJL1302A

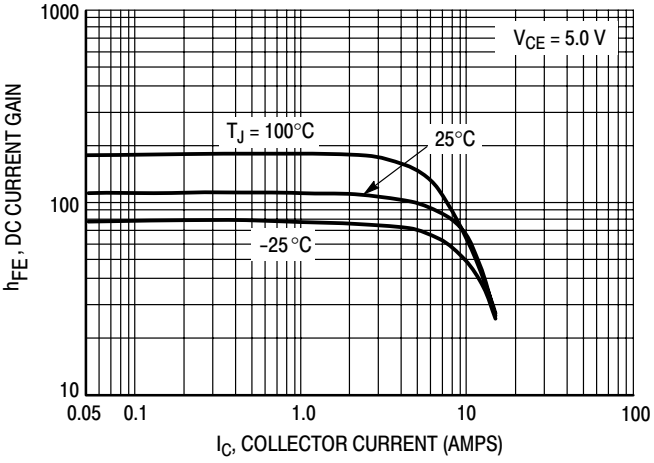

Figure 3. DC Current Gain

NPN MJL3281A

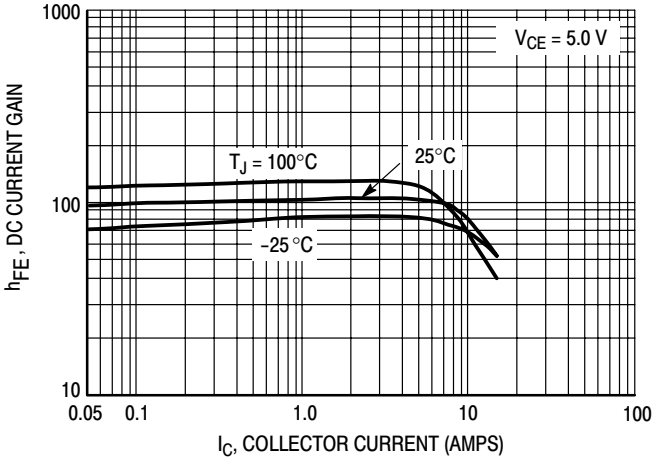

Figure 4. DC Current Gain

PNP MJL1302A

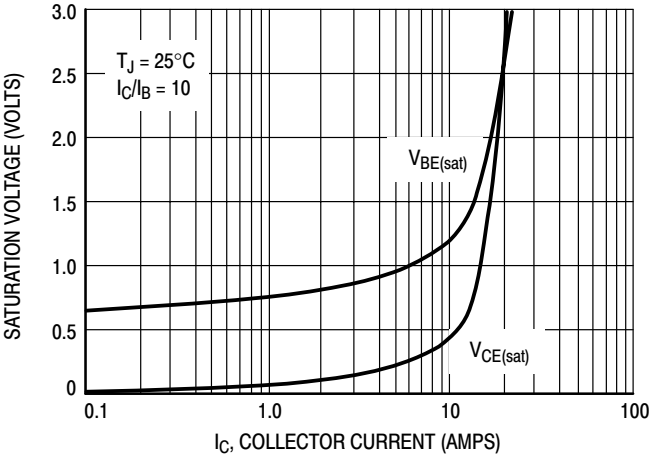

Figure 5. Typical Saturation Voltages

NPN MJL3281A

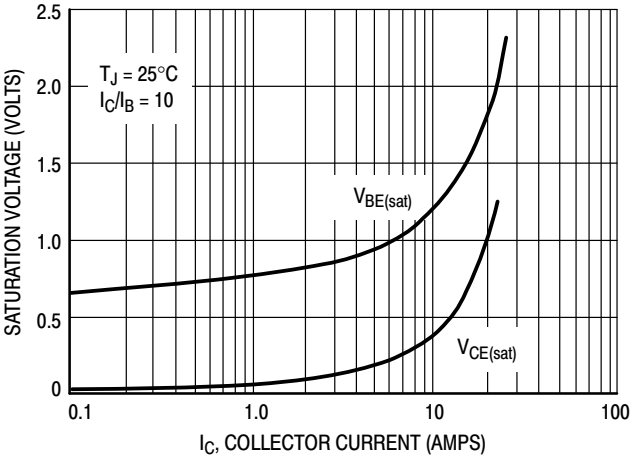

Figure 6. Typical Saturation Voltages

TYPICAL CHARACTERISTICS

PNP MJL1302A

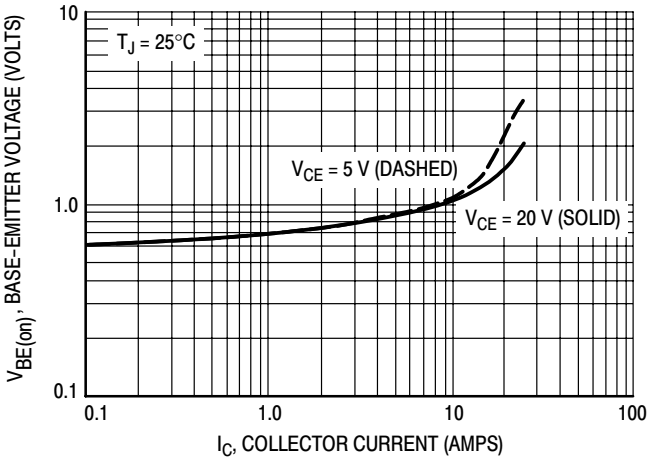

Figure 7. Typical Base−Emitter Voltage

NPN MJL3281A

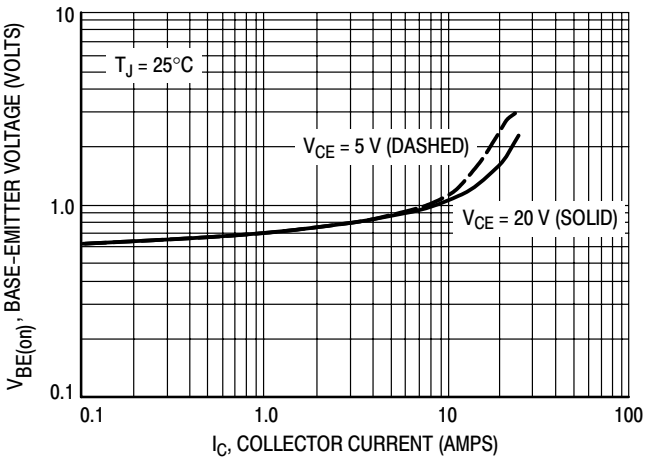

Figure 8. Typical Base−Emitter Voltage

PNP MJL1302A

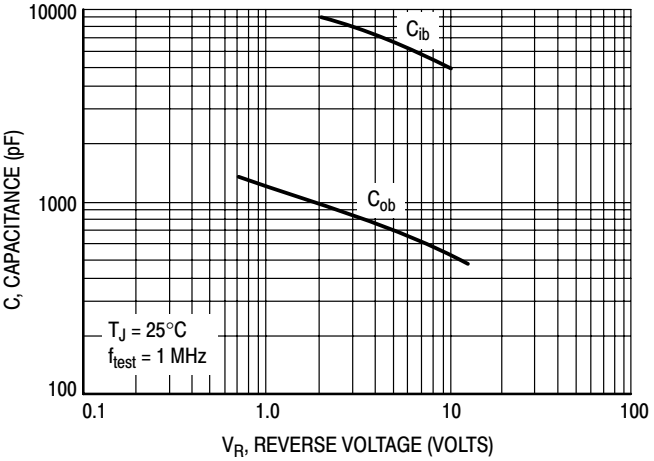

Figure 9. MJL1302A Typical Capacitance

NPN MJL3281A

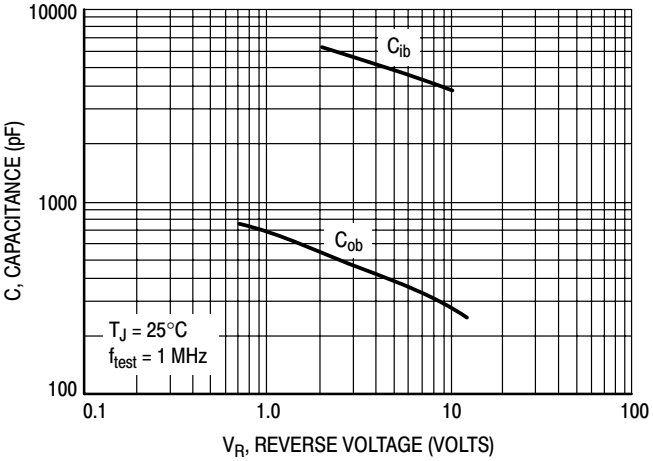

Figure 10. MJL3281A Typical Capacitance

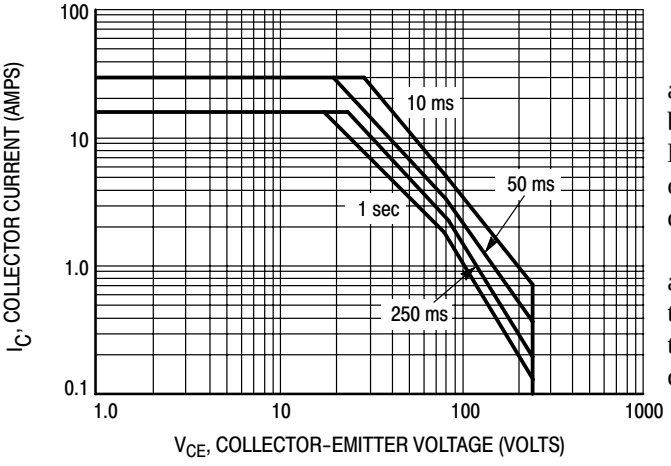

Figure 11. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

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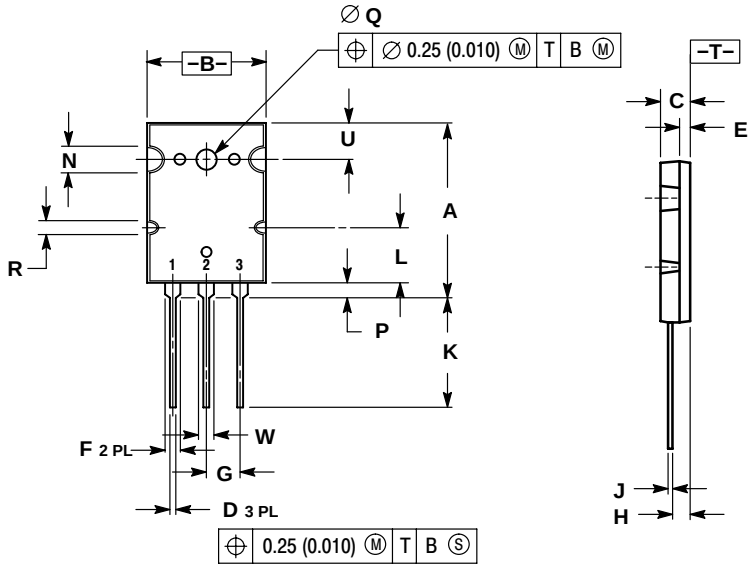

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.2 REF		0.411 REF	
N	4.35 REF		0.172 REF	
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.25 REF		0.089 REF	
U	6.3 REF		0.248 REF	
W	2.8	3.2	0.110	0.125

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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