Ordering Information

Device	**16-Lead QFN** *4.00x4.00mm body* *1.00mm height (max)* *0.65mm pitch*
MD1811	MD1811K6-G

-G indicates package is RoHS compliant ('Green')

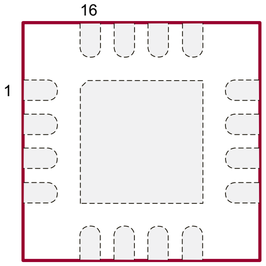
Absolute Maximum Ratings

Parameter	Value
V_{DD} - V_{SS}, Logic supply voltage	-0.5V to +13.5V
V_H, Output high supply voltage	V_L -0.5V to V_{DD}+0.5V
V_L, Output low supply voltage	V_{SS} -0.5V to V_H+0.5V
V_{SS}, Low side supply voltage	-7.0V to +0.5V
Logic input levels	V_{SS} -0.5V to GND +7.0V
Maximum junction temperature	+125°C
Storage temperature	-65°C to 150°C
Operating temperature	-20°C to +85°C
Package power dissipation	2.2W
Thermal resistance (θ_{JA})*	45°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* *1.0oz 4-layer 3x4" PCB*

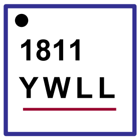
Pin Configuration



16-Lead QFN (K6)

(top view)

Product Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
___ = "Green" Packaging

Package may or may not include the following marks: Si or

16-Lead QFN (K6)

DC Electrical Characteristics *(V_H = V_{DD} = 12V, V_L = V_{SS} = GND = 0V, V_{OE} = 3.3V, T_A = 25°C)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}-V_{SS}	Logic supply voltage	4.5	-	13	V	2.5V ≤ V_{DD} ≤13V
V_{SS}	Low side supply voltage	-5.5	-	0	V	--
V_H	Output high supply voltage	V_{SS} +2.0	-	V_{DD}	V	--
V_L	Output low supply voltage	V_{SS}	-	V_{DD} -2.0	V	--
I_{DDQ}	V_{DD} quiescent current	-	0.8	-	mA	No input transitions, OE = 1
I_{HQ}	V_H quiescent current	-		10	μA	
I_{DD}	V_{DD} average current	-	8.0	-	mA	One channel on at 5.0Mhz, No load
I_H	V_H average current	-	26	-	mA	
V_{IH}	Input logic voltage high	V_{OE} -0.3	-	5.0	V	For logic inputs INA, INB, INC, and IND
V_{IL}	Input logic voltage low	0	-	0.3	V	
I_{IH}	Input logic current high	-	-	1.0	μA	
I_{IL}	Input logic current low	-	-	1.0	μA	
V_{IH}	OE Input logic voltage high	1.7	-	5.0	V	For logic input OE
V_{IL}	OE Input logic voltage low	0	-	0.3	V	
R_{IN}	Input logic impedance to GND	10	20	30	KΩ	
C_{IN}	Logic input capacitance	-	5.0	10	pF	---

Outputs *($V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{OE} = 3.3V$, $T_A = 25°C$)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
R_{SINK}	Output sink resistance	-	-	12.5	Ω	$I_{SINK} = 50mA$
R_{SOURCE}	Output source resistance	-	-	12.5	Ω	$I_{SOURCE} = 50mA$
I_{SINK}	Peak output sink current	-	2.0	-	A	--
I_{SOURCE}	Peak output source current	-	2.0	-	A	--

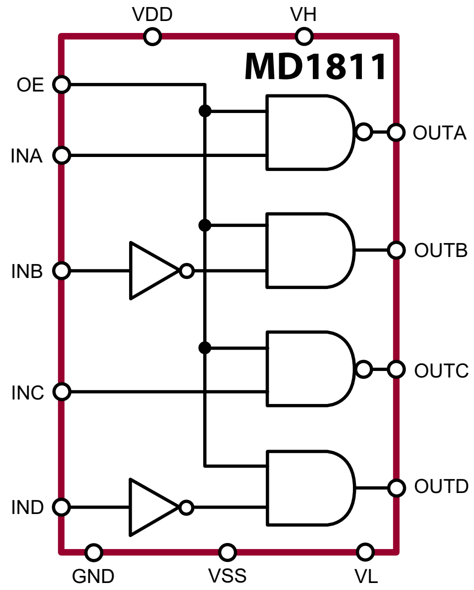
AC Electrical Characteristics *($V_H = V_{DD} = 12V$, $V_L = V_{SS} = GND = 0V$, $V_{OE} = 3.3V$, $T_A = 25°C$)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{irf}	Input or OE rise & fall time	-	-	10	ns	Logic input edge speed requirement
t_{PLH}	Propagation delay when output is from low to high	-	7.0	-	ns	$C_{LOAD} = 1000pF$, see timing diagram Input signal rise/fall time 2ns
t_{PHL}	Propagation delay when output is from high to low	-	7.0	-	ns	
t_r	Output rise time	-	6.0	-	ns	
t_f	Output fall time	-	6.0	-	ns	
$\| t_r - t_f \|$	Rise and fall time matching	-	1.0	-	ns	For each channel
$\| t_{PLH} - t_{PHL} \|$	Propagation low to high and high to low matching	-	1.0	-	ns	
Δt_{dm}	Propagation delay matching	-	±2.0	-	ns	Device to device delay match
t_{OE}	Output enable time	-	9.0	-	ns	---

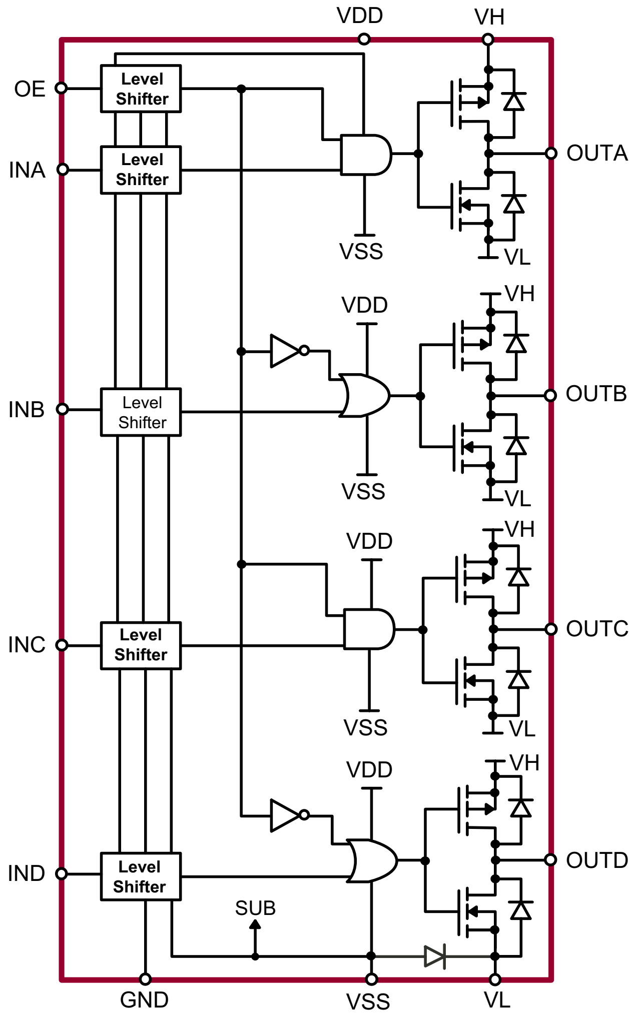
Logic Truth Table

Logic Inputs			Output	
OE	**INA**	**INB**	**OUTA**	**OUTB**
H	L	L	V_H	V_H
H	L	H	V_H	V_L
H	H	L	V_L	V_H
H	H	H	V_L	V_L
L	X	X	V_H	V_L
OE	**INC**	**IND**	**OUTC**	**OUTD**
H	L	L	V_H	V_H
H	L	H	V_H	V_L
H	H	L	V_L	V_H
H	H	H	V_L	V_L
L	X	X	V_H	V_L

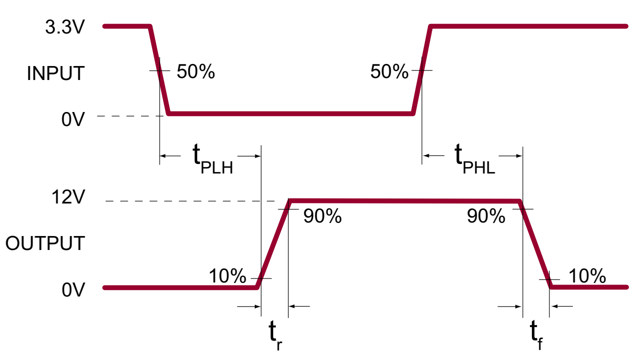
Simplified Block Diagram

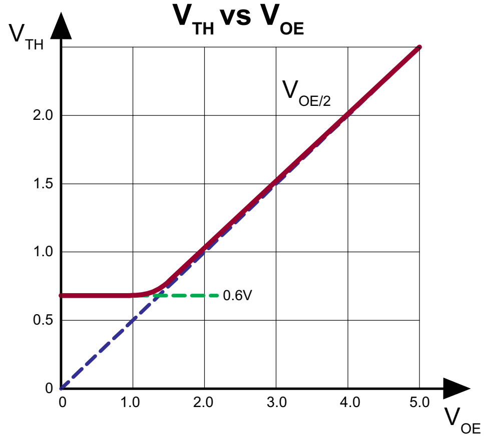


Detailed Block Diagram



Timing Diagram and V_{TH} / V_{OE} Curve





Application Information

For proper operation of the MD1811, low inductance bypass capacitors should be used on the various supply pins. The GND pin should be connected to the logic ground. The INA, INB INC, IND, and OE pins should be connected to a logic source with a swing of GND to OE, where OE is 1.8 to 5.0V. Good trace practices should be followed corresponding to the desired operating speed. The internal circuitry of the MD1811 is capable of operating up to 100MHz, with the primary speed limitation being the loading effects of the load capacitance. Because of this speed and the high transient currents that result with capacitive loads, the bypass capacitors should be as close to the chip pins as possible. Unless the load specifically requires bipolar drive, the VSS and VL pins should have low inductance feed-through connections directly to a ground plane. If these voltages are not zero, then they need bypass capacitors in a manner similar to the positive power supplies. The power connection VDD should have a ceramic bypass capacitor to the ground plane with short leads and decoupling components to prevent resonance in the power leads.

The voltages of VH and VL decide the output signal levels. These two pins can draw fast transient currents of up to 2.0A, so they should be provided with an appropriate bypass capacitor located next to the chip pins. A ceramic capacitor of up to 1.0μF may be appropriate, with a series ferrite bead to prevent resonance in the power supply lead coming to the capacitor. Pay particular attention to minimizing trace lengths, current loop area and using sufficient trace width to reduce inductance. Surface mount components are highly recommended. Since the output impedance of this driver is very low, in some cases it may be desirable to add a small series resistance in series with the output signal to obtain better waveform transitions at the load terminals. This will of course reduce the output voltage slew rate at the terminals of a capacitive load.

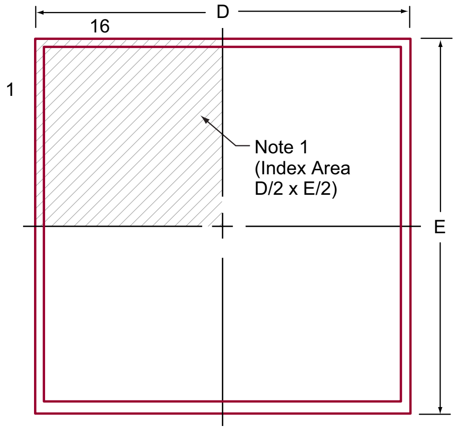
Pay particular attention that parasitic couplings are minimized from the output to the input signal terminals. The parasitic feedback may cause oscillations or spurious waveform shapes on the edges of signal transitions. Since the input operates with signals down to 1.8V even small coupled voltages may cause problems. Use of a solid ground plane and good power and signal layout practices will prevent this problem. Be careful that a circulating ground return current from a capacitive load cannot react with common inductance to cause noise voltages in the input logic circuitry.

Pin Description

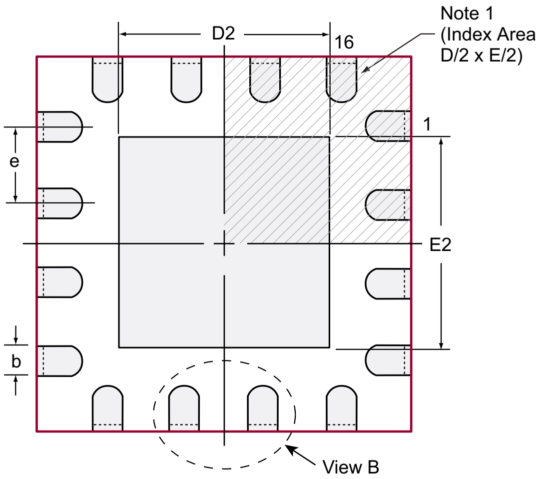
Pin #	Function	Description
1	INB	Logic input. Input logic low will cause the output to swing to VH. Input logic high will cause the output to swing to VL. Keep all logic inputs low until IC powered up.
2	VL	Supply voltage for N-channel output stage.
3	GND	Logic input ground reference.
4	VL	Supply voltage for N-channel output stage.
5	INC	Logic input. Input logic low will cause the output to swing to VH. Input logic high will cause the output to swing to VL. Keep all logic inputs low until IC powered up.
6	IND	
7	VSS	Low side supply voltage. VSS is also connected to the IC substrate. It is required to connect to the most negative potential of voltage supplies and powered-up first.
8	OUTD	Output driver. Swings from VH to VL. Intended to drive the gate of an externel N-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTD will swing to VL turning off the external N-channel MOSFET.
9	OUTC	Output driver. Swings from VH to VL. Intended to drive the gate of an externel P-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTC will swing to VH turning off the external P-channel MOSFET.
10, 11	VH	Supply voltage for P-channel output stage.
12	OUTB	Output driver. Swings from VH to VL. Intended to drive the gate of an externel N-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTB will swing to VL turning off the external N-channel MOSFET.
13	OUTA	Output driver. Swings from VH to VL. Intended to drive the gate of an externel P-channel MOSFET via a series capacitor. When OE is low, the output is disabled. OUTA will swing to VH turning off the external P-channel MOSFET.
14	VDD	High side supply voltage.
15	INA	Logic input. Input logic low will cause the output to swing to VH. Input logic high will cause the output to swing to VL. Keep all logic inputs low until IC powered up.
16	OE	Output-Enable logic input. When OE is high, $(V_{OE}+V_{GND})/2$ sets the logic threshold level for inputs, When OE is low, OUTA and OUTC are at VH, OUTB and OUTD are at VL, regardless of the inputs INA, INB, INC or IND. Keep OE low until IC powered up.
Substrate		The IC substrate is internally connected to the thermal pad. Thermal Pad and VSS must be connected externally.

16-Lead QFN Package Outline (K6)

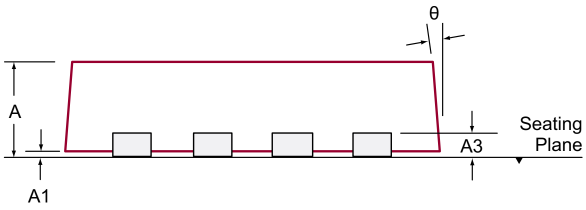
4.00x4.00mm body, 1.00mm height (max), 0.65mm pitch



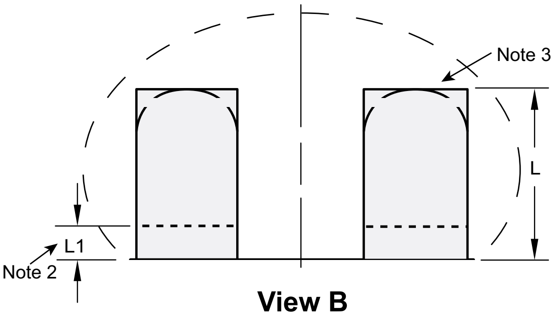
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.85*	2.50	3.85*	2.50	0.65 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.30	4.00	2.65	4.00	2.65		0.40†	-	-
	MAX	1.00	0.05		0.35	4.15*	2.80	4.15*	2.80		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VGGC-2, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-16QFNK64X4P065, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)