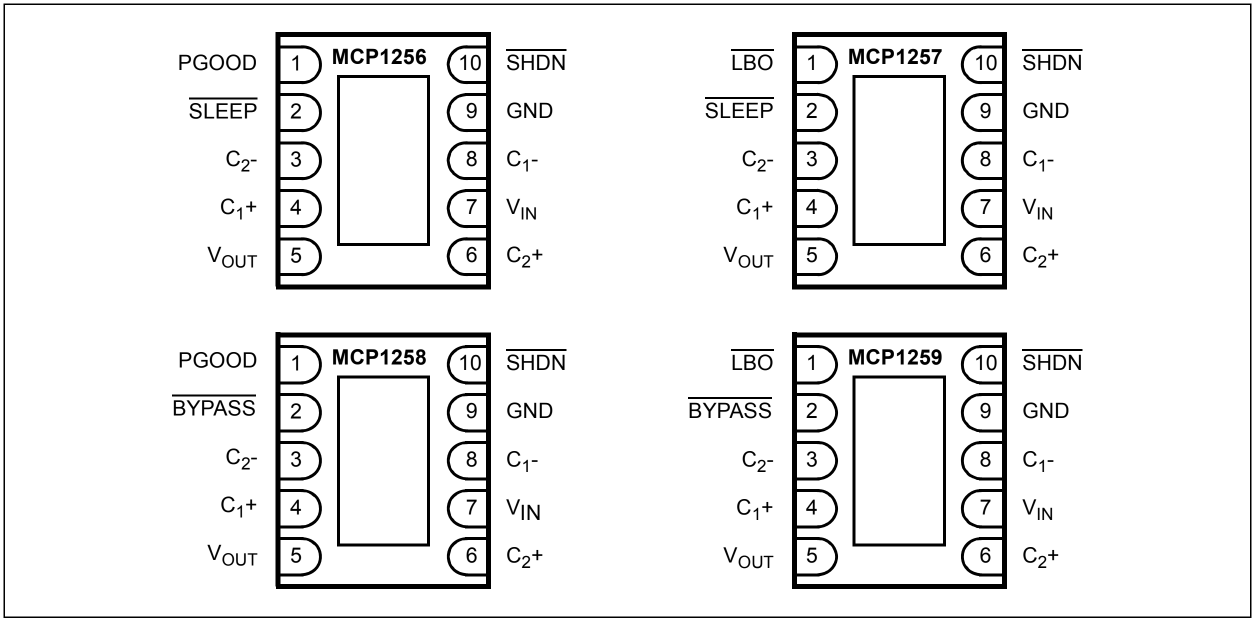
Package Pinouts



Functional Block Diagram

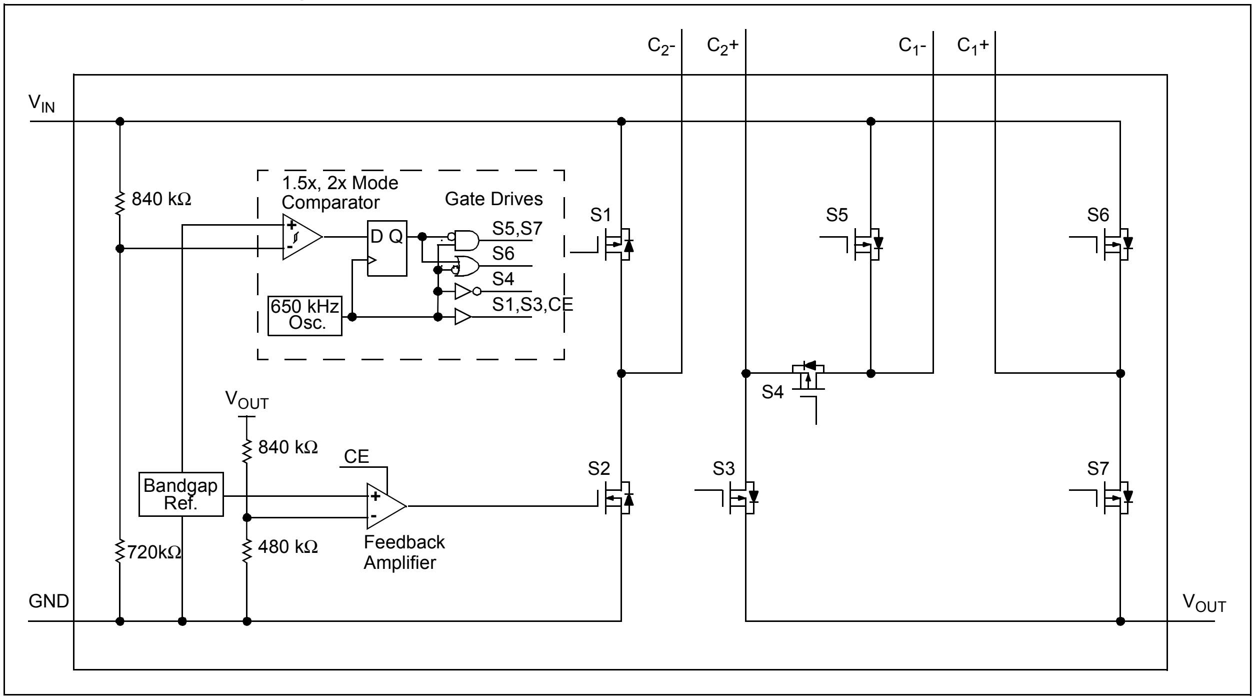


TABLE 1: SWITCH LOGIC

Mode	Phase	Oscillator	Q	S1	S2(CE)	S3	S4	S5	S6	S7
1.5x	Charging	H	L	H	H	H	L	H	L	H
1.5x	Transfer	L	L	L	L	L	H	L	H	L
2x	Charging	H	H	H	H	H	L	L	H	L
2x	Transfer	L	H	L	L	L	H	L	H	L
BYPASS	—	—	—	H	L	H	H	H	L	L

Legend: L is Logic Low, H is Logic High

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Power Supply Voltage, V_{IN}..3.8V

Voltage on Any Pin w.r.t. GND .... -0.3V to (V_{IN}+0.3V)

Output Short Circuit Duration ....continuous

Storage Temperature Range.........................-65°C to +150°C

Ambient Temperature with Power Applied ....-55°C to +125°C

Maximum Junction Temperature.................................+150°C

ESD protection on all pins

Human Body Model (1.5 kΩ in Series with 100 pF).......≥ 2 kV

Machine Model (200 pF, No Series Resistance).............200V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{IN} = 1.8V to 3.6V, $\overline{SHDN}$ = V_{IN}, C_{IN} = C_{OUT} = 10 µF, C_1 = C_2 = 1 µF, I_{OUT} = 10 mA, T_J = -40°C to +125°C. Typical values are at T_J = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
ALL DEVICES						
Supply Voltage	V_{IN}	1.8	—	3.6	V	
Output Voltage	V_{OUT}	—	3.3	—	V	
Output Voltage Accuracy	V_{OUT}	-3.0	±0.5	+3.0	%	I_{OUT} = 10 mA to $I_{OUT(MAX)}$
Output Current	$I_{OUT(MAX)}$	30	—	—	mA	$1.8V \le V_{IN} < 2.0V$
		70	—	—	mA	$2.0V \le V_{IN} < 2.2V$
		100	—	—	mA	$2.2V \le V_{IN} \le 3.6V$
Short Circuit Current	I_{SC}	—	150	—	mA	V_{OUT} = 0V, V_{IN} = 1.8V to 3.6V
Power Efficiency	η	—	84.5	—	%	V_{IN} = 1.8V, I_{OUT} = 10 mA
		—	84.5	—	%	V_{IN} = 1.8V, I_{OUT} = 50 mA
		—	76.4	—	%	V_{IN} = 2.0V, I_{OUT} = 10 mA
		—	80.1	—	%	V_{IN} = 2.0V, I_{OUT} = 50 mA
		—	64.0	—	%	V_{IN} = 2.4V, I_{OUT} = 10 mA
		—	67.1	—	%	V_{IN} = 2.4V, I_{OUT} = 50 mA
		—	67.5	—	%	V_{IN} = 2.4V, I_{OUT} = 100 mA
		—	69.7	—	%	V_{IN} = 2.8V, I_{OUT} = 10 mA
		—	76.0	—	%	V_{IN} = 2.8V, I_{OUT} = 50 mA
		—	76.7	—	%	V_{IN} = 2.8V, I_{OUT} = 100 mA
		—	65.0	—	%	V_{IN} = 3.0V, I_{OUT} = 10 mA
		—	71.0	—	%	V_{IN} = 3.0V, I_{OUT} = 50 mA
		—	71.6	—	%	V_{IN} = 3.0V, I_{OUT} = 100 mA
Shutdown Input - $\overline{SHDN}$						
$\overline{SHDN}$ Input Voltage Low	$V_{IL(\overline{SHDN})}$	—	—	0.4	V	
$\overline{SHDN}$ Input Voltage High	$V_{IH(\overline{SHDN})}$	1.4	—	—	V	
$\overline{SHDN}$ Input Leakage Current	$I_{LK(\overline{SHDN})}$	—	0.001	0.1	µA	
$\overline{SHDN}$ Quiescent Current	I_Q	—	0.25	2	µA	$V_{\overline{SHDN}}$ = 0V, T_J = +25°C
Thermal Shutdown						
Thermal Shutdown Threshold	T_J	—	160	—	°C	
Thermal Shutdown Hysteresis	$T_{J(HYS)}$	—	15	—	°C	

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{IN} = 1.8V to 3.6V, $\overline{\text{SHDN}}$ = V_{IN}, C_{IN} = C_{OUT} = 10 µF, C_1 = C_2 = 1 µF, I_{OUT} = 10 mA, T_J = -40°C to +125°C. Typical values are at T_J = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
MCP1256 and MCP1257 Devices						
SLEEP Mode Input - $\overline{\text{SLEEP}}$						
$\overline{\text{SLEEP}}$ Input Voltage Low	$V_{IL(\overline{SLEEP})}$	—	—	0.4	V	
$\overline{\text{SLEEP}}$ Input Voltage High	$V_{IH(\overline{SLEEP})}$	1.4	—	—	V	
$\overline{\text{SLEEP}}$ Input Leakage Current	$I_{LK(\overline{SLEEP})}$	—	0.001	0.1	µA	
$\overline{\text{SLEEP}}$ Quiescent Current	I_Q	—	10	20	µA	$V_{\overline{SLEEP}}$ = 0V, I_{OUT} = 0 mA
MCP1256 and MCP1258 Devices						
Power-Good Output - PGOOD						
PGOOD Threshold	V_{TH}	—	93	—	%	Percent of V_{OUT} Falling
PGOOD Hysteresis	V_{HYS}	—	110	—	mV	V_{OUT} Rising
PGOOD Output Low Voltage	V_{OL}	—	25	100	mV	I_{SINK} = 0.5 mA, V_{IN} = 1.8V
PGOOD Input Leakage Current	$I_{LK(PGOOD)}$	—	0.02	1	µA	V_{PGOOD} = V_{IN}
MCP1257 and MCP1259						
Low-Battery Output - $\overline{\text{LBO}}$						
$\overline{\text{LBO}}$ Threshold	V_{TH}	—	1.95	—	V	V_{IN} Falling
$\overline{\text{LBO}}$ Hysteresis	V_{HYS}	—	240	—	mV	V_{IN} Rising
$\overline{\text{LBO}}$ Output Low Voltage	V_{OL}	—	25	100	mV	I_{SINK} = 0.5 mA, V_{IN} = 1.8V
$\overline{\text{LBO}}$ Input Leakage Current	$I_{LK(\overline{LBO})}$	—	0.02	1	µA	$V_{\overline{LBO}}$ = V_{IN}
MCP1258 and MCP1259						
BYPASS Mode Input - $\overline{\text{BYPASS}}$						
$\overline{\text{BYPASS}}$ Input Voltage Low	$V_{IL(\overline{BYPASS})}$	—	—	0.4	V	
$\overline{\text{BYPASS}}$ Input Voltage High	$V_{IH(\overline{BYPASS})}$	1.4	—	—	V	
$\overline{\text{BYPASS}}$ Input Leakage Current	$I_{LK(\overline{BYPASS})}$	—	0.001	0.1	µA	
$\overline{\text{BYPASS}}$ Quiescent Current	I_Q	—	0.25	2	µA	$V_{\overline{BYPASS}}$ = 0V, I_{OUT} = 0 mA, T_J = +25°C
$\overline{\text{BYPASS}}$ Input-to-Output Impedance	R_{BYPASS}	—	1.5	—	Ω	V_{IN} = 2.4V

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{IN} = 1.8V to 3.6V, $\overline{SHDN}$ = V_{IN}, C_{IN} = C_{OUT} = 10 µF, C_1 = C_2 = 1 µF, I_{OUT} = 10 mA, T_J = -40°C to +125°C. Typical values are at T_J = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
ALL DEVICES						
Internal Oscillator Frequency	F_{OSC}	—	650	—	kHz	
Output Voltage Ripple, Normal Operation	V_{RIP}	—	5	—	mVp-p	C_{OUT} = 10 µF, I_{OUT} = 10 mA
		—	20	—	mVp-p	C_{OUT} = 10 µF, I_{OUT} = 100 mA
		—	12	—	mVp-p	C_{OUT} = 2.2 µF, I_{OUT} = 10 mA
		—	55	—	mVp-p	C_{OUT} = 2.2 µF, I_{OUT} = 100 mA
V_{OUT} Wake-up Time From Shutdown	T_{WKUP}	—	175	—	µs	V_{IN} = 3.0V, I_{OUT} = 10 mA, $\overline{SHDN}$ = $V_{IH(MIN)}$, V_{OUT} from 0 to 90% Nominal Regulated Output Voltage
MCP1256 and MCP1257						
Output Voltage Ripple, SLEEP Mode	V_{RIP}	—	40	—	mVp-p	C_{OUT} = 10 µF, I_{OUT} = 0.1 mA
		—	60	—	mVp-p	C_{OUT} = 10 µF, I_{OUT} = 4 mA
		—	40	—	mVp-p	C_{OUT} = 2.2 µF, I_{OUT} = 0.1 mA
		—	60	—	mVp-p	C_{OUT} = 2.2 µF, I_{OUT} = 4 mA
MCP1258 and MCP1259						
V_{OUT} Wake-up Time From BYPASS	T_{WKUP}	—	150	—	µs	V_{IN} = 3.0V, I_{OUT} = 10 mA, $\overline{SHDN}$ = $V_{IH(MIN)}$, V_{OUT} from 0 to 90% Nominal Regulated Output Voltage

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits apply for V_{IN} = 1.8V to 3.6V, $\overline{SHDN}$ = V_{IN}, C_{IN} = C_{OUT} = 10 µF, C_1 = C_2 = 1 µF, I_{OUT} = 10 mA, T_J = -40°C to +125°C. Typical values are at T_J = +25°C.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_J	-40	—	+125	°C	
Operating Temperature Range	T_J	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 10-Lead, MSOP	θ_{JA}	—	200	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection
Thermal Resistance, 10-Lead, DFN 3 mm x 3 mm	θ_{JA}	—	57	—	°C/W	4-Layer JC51-7 Standard Board, Natural Convection

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

NOTE: Unless otherwise indicated, $C_{IN} = C_{OUT} = 10\ \mu F$, $C_1 = C_2 = 1\ \mu F$, $I_{OUT} = 10\ mA$, and $T_A = +25°C$.

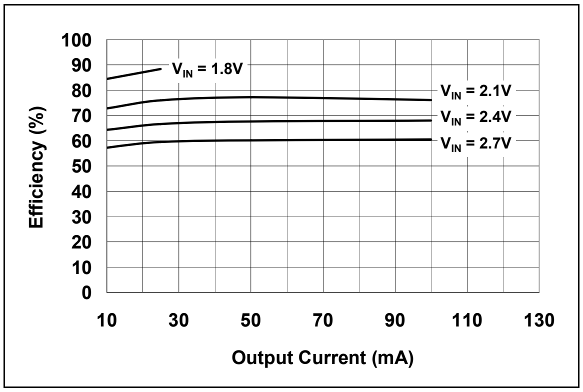


FIGURE 2-1: *Efficiency (η) vs. Output Current (I_{OUT}).*

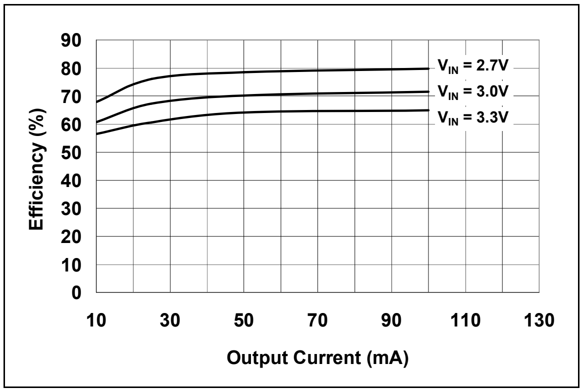


FIGURE 2-2: *Efficiency (η) vs. Output Current (I_{OUT}).*

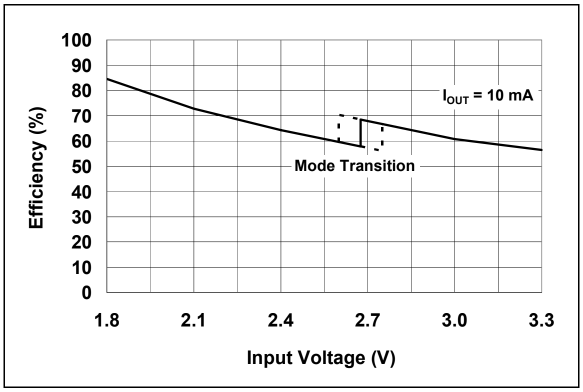


FIGURE 2-3: *Efficiency (η) vs. Supply Voltage (V_{IN}).*

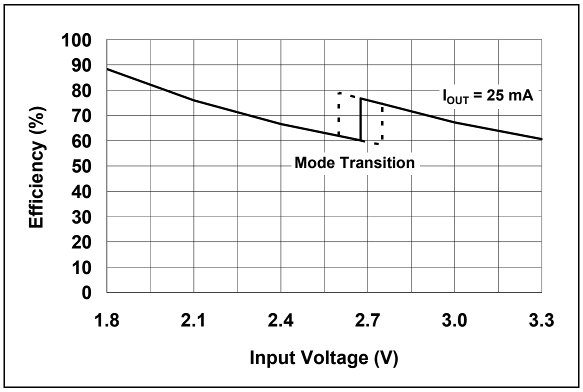


FIGURE 2-4: *Efficiency (η) vs. Supply Voltage (V_{IN}).*

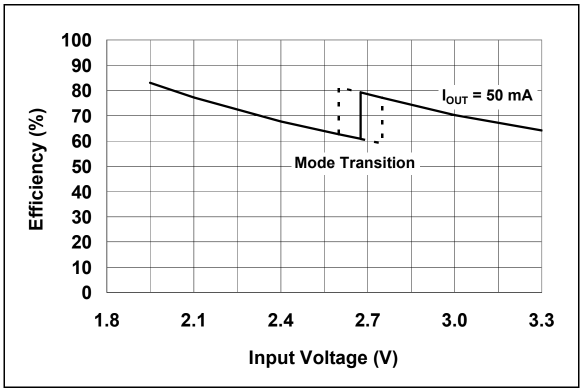


FIGURE 2-5: *Efficiency (η) vs. Supply Voltage (V_{IN}).*

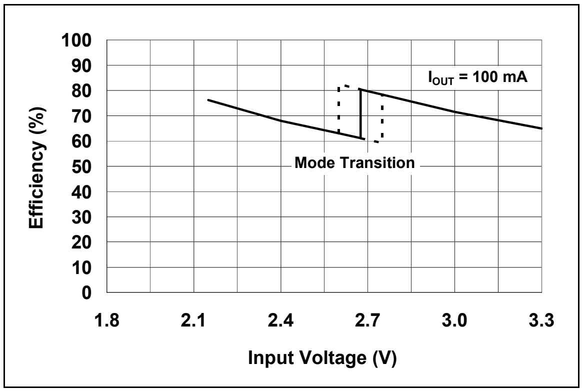


FIGURE 2-6: *Efficiency (η) vs. Supply Voltage (V_{IN}).*

TYPICAL PERFORMANCE CURVES (CONTINUED)

NOTE: Unless otherwise indicated, $C_{IN} = C_{OUT} = 10\ \mu F$, $C_1 = C_2 = 1\ \mu F$, $I_{OUT} = 10\ mA$, and $T_A = +25°C$.

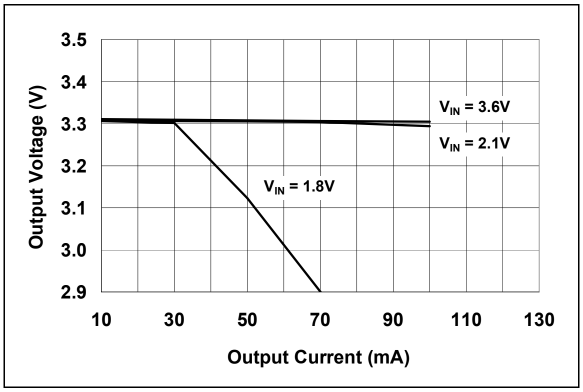


FIGURE 2-7: *Output Voltage (V_{OUT}) vs. Output Current (I_{OUT}).*

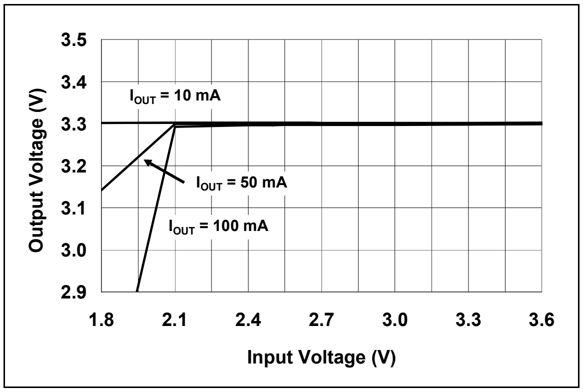


FIGURE 2-8: *Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}).*

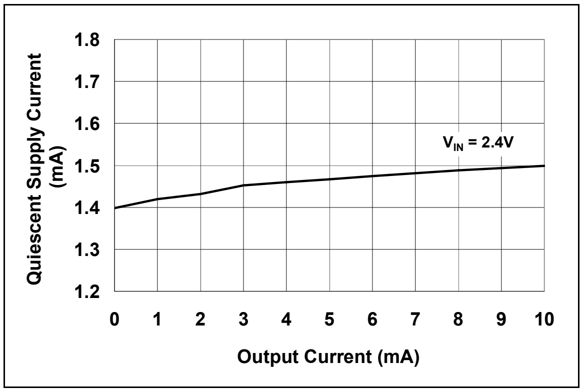


FIGURE 2-9: *Quiescent Supply Current (I_Q) vs. Output Current (I_{OUT}) - Normal Mode.*

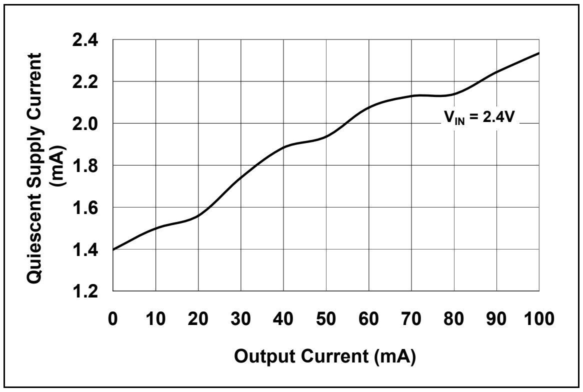


FIGURE 2-10: *Quiescent Supply Current (I_Q) vs. Output Current (I_{OUT}) - Normal Mode.*

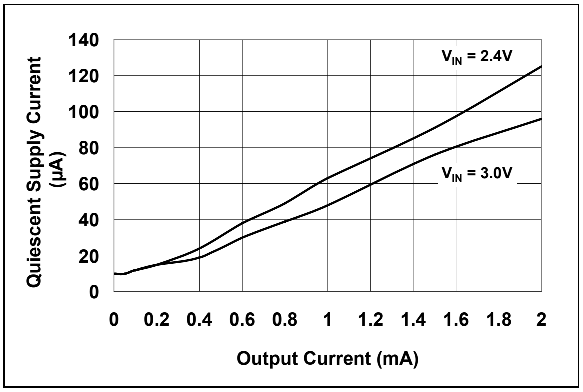


FIGURE 2-11: *Quiescent Supply Current (I_Q) vs. Output Current (I_{OUT}) - SLEEP Mode.*

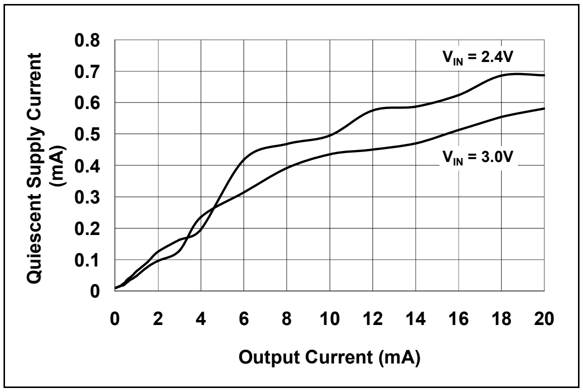


FIGURE 2-12: *Quiescent Supply Current (I_Q) vs. Output Current (I_{OUT}) - SLEEP Mode.*

TYPICAL PERFORMANCE CURVES (CONTINUED)

NOTE: Unless otherwise indicated, $C_{IN} = C_{OUT} = 10\ \mu F$, $C_1 = C_2 = 1\ \mu F$, $I_{OUT} = 10\ mA$, and $T_A = +25°C$.

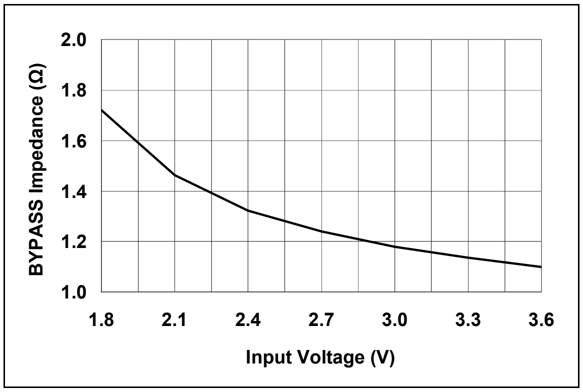


FIGURE 2-13: *BYPASS Impedance (R_{BYPASS}) vs. Supply Voltage (V_{IN}).*

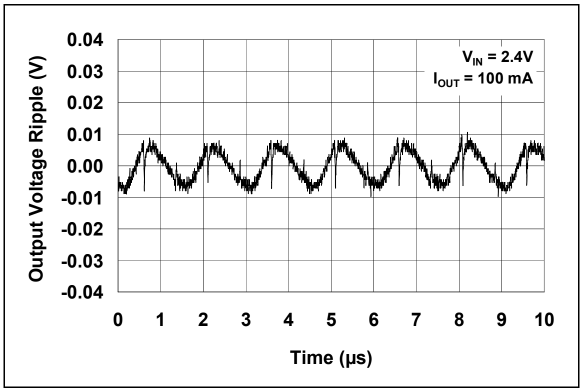


FIGURE 2-16: *Output Voltage Ripple vs. Time - Normal 2x Mode.*

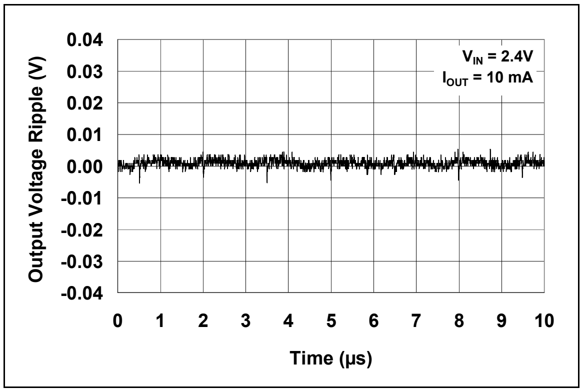


FIGURE 2-14: *Output Voltage Ripple vs. Time - Normal 2x Mode.*

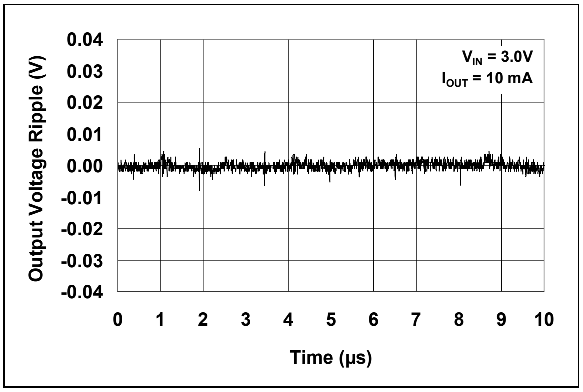


FIGURE 2-17: *Output Voltage Ripple vs. Time - Normal 1.5x Mode.*

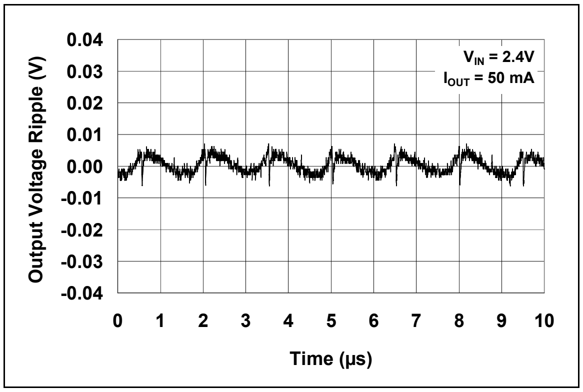


FIGURE 2-15: *Output Voltage Ripple vs. Time - Normal 2x Mode.*

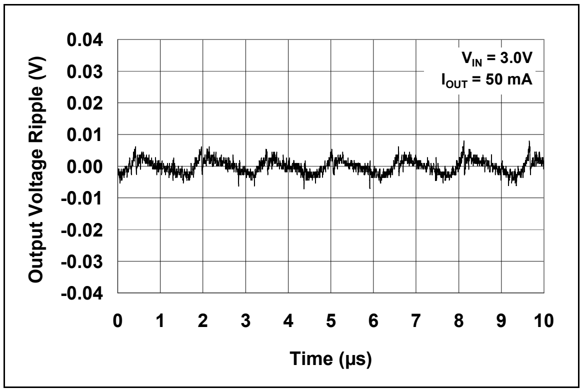


FIGURE 2-18: *Output Voltage Ripple vs. Time - Normal 1.5x Mode.*

TYPICAL PERFORMANCE CURVES (CONTINUED)

NOTE: Unless otherwise indicated, $C_{IN} = C_{OUT} = 10\ \mu F$, $C_1 = C_2 = 1\ \mu F$, $I_{OUT} = 10\ mA$, and $T_A = +25°C$.

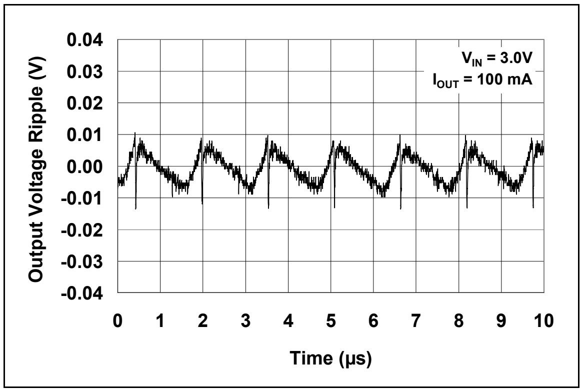


FIGURE 2-19: *Output Voltage Ripple vs. Time - Normal 1.5x Mode.*

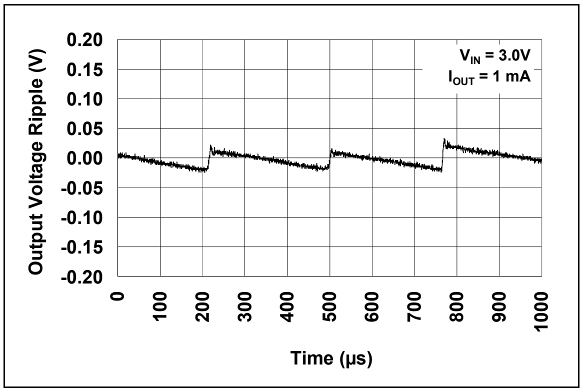


FIGURE 2-22: *Output Voltage Ripple vs. Time - SLEEP Mode.*

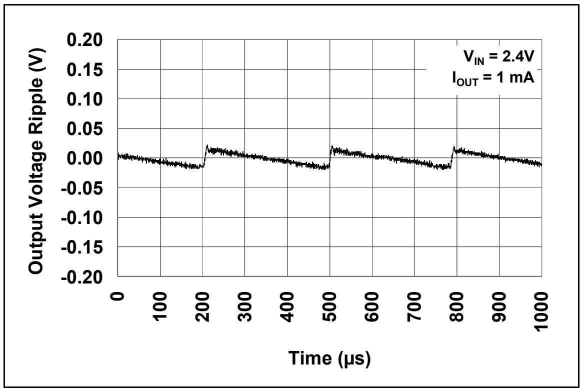


FIGURE 2-20: *Output Voltage Ripple vs. Time - SLEEP Mode.*

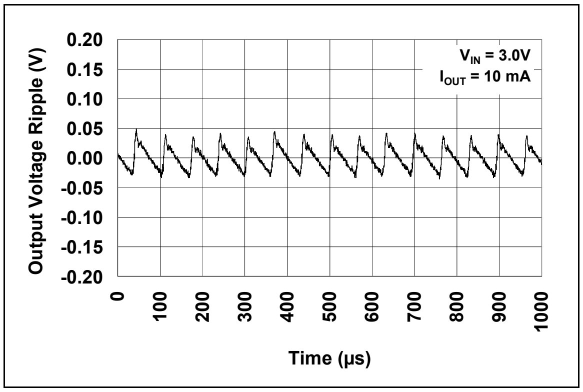


FIGURE 2-23: *Output Voltage Ripple vs. Time - SLEEP Mode.*

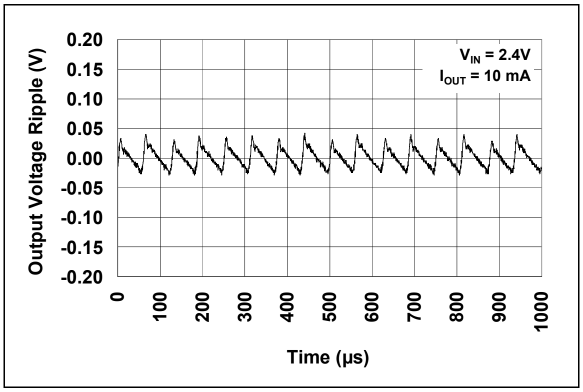


FIGURE 2-21: *Output Voltage Ripple vs. Time - SLEEP Mode.*

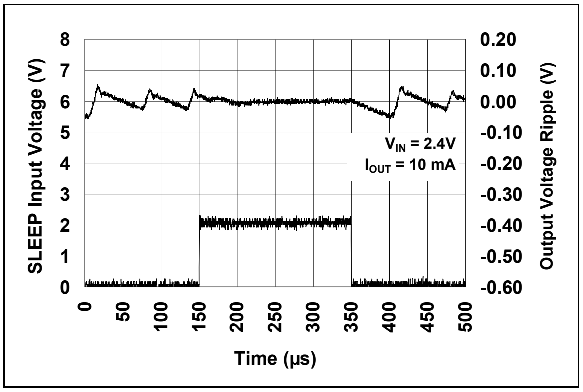


FIGURE 2-24: *Output Voltage Ripple vs. Time - Mode Transition: SLEEP Mode-to-Normal 2x Mode-to-SLEEP Mode.*

TYPICAL PERFORMANCE CURVES (CONTINUED)

NOTE: Unless otherwise indicated, $C_{IN} = C_{OUT} = 10\ \mu F$, $C_1 = C_2 = 1\ \mu F$, $I_{OUT} = 10\ mA$, and $T_A = +25°C$.

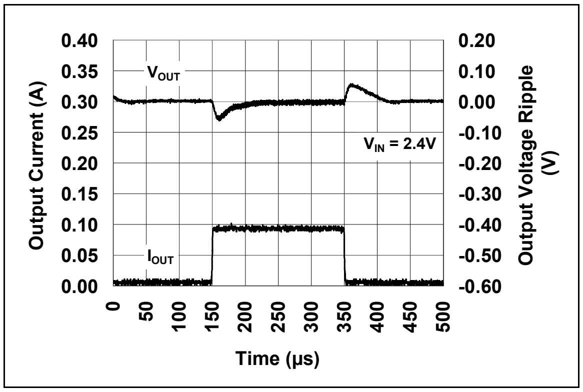


FIGURE 2-25: *Load Transient Response - Normal 2x Mode.*

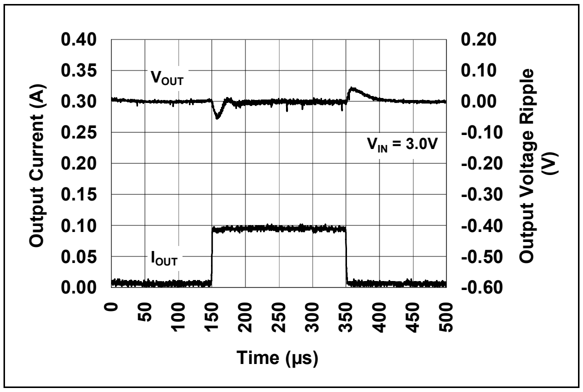


FIGURE 2-26: *Load Transient Response - Normal 1.5x Mode.*

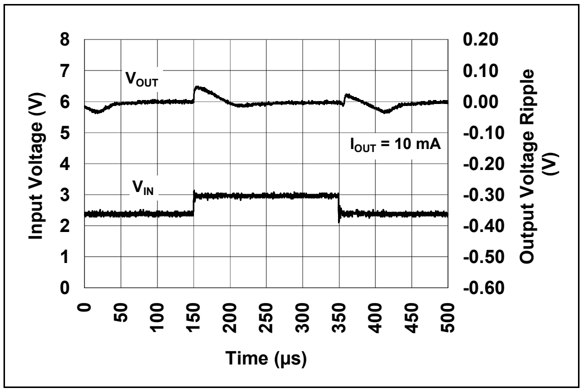


FIGURE 2-27: *Line Transient Response.*

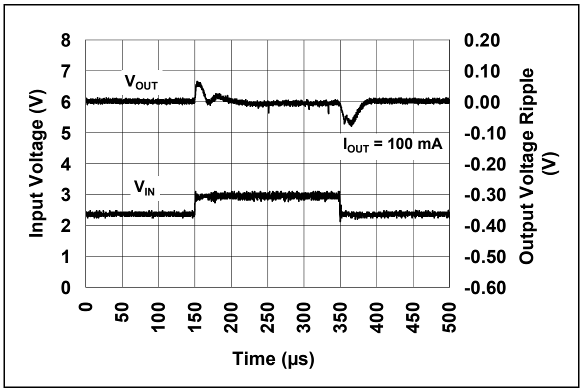


FIGURE 2-28: *Line Transient Response.*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.		Symbol	Function
DFN	MSOP		
1	1	PGOOD $\overline{\text{LBO}}$	Power-Good Indication Open-Drain Output Pin: MCP1256 and MCP1258 Low-Battery Indication Open-Drain Output Pin: MCP1257 and MCP1259
2	2	$\overline{\text{SLEEP}}$ $\overline{\text{BYPASS}}$	Active Low SLEEP Mode Input Pin: MCP1256 and MCP1257 Active Low BYPASS Mode Input Pin: MCP1258 and MCP1259
3	3	C2-	Flying Capacitor Negative Pin
4	4	C1+	Flying Capacitor Positive Pin
5	5	V_{OUT}	Regulated 3.3V Output Voltage
6	6	C2+	Flying Capacitor Positive Pin
7	7	V_{IN}	Power Supply Input Voltage
8	8	C1-	Flying Capacitor Negative Pin
9	9	GND	0V Reference
10	10	$\overline{\text{SHDN}}$	Active Low SHUTDOWN Mode Input Pin

3.1 Status Indication (PGOOD, $\overline{\text{LBO}}$)

3.1.1 POWER-GOOD OUTPUT PIN (PGOOD)

MCP1256/8: PGOOD is high impedance when the output voltage is in regulation. A logic low is asserted when the output falls 7% (typical) below the nominal value. The PGOOD output remains low until V_{OUT} is within 3% (typical) of its nominal value. On start-up, this pin indicates when the output voltage reaches its final value. PGOOD is high impedance when $\overline{\text{SHDN}}$ is low or when $\overline{\text{BYPASS}}$ is low (MCP1258).

3.1.2 LOW-BATTERY OUTPUT PIN ($\overline{\text{LBO}}$)

MCP1257/9: $\overline{\text{LBO}}$ is high impedance when the input voltage is above the low-battery threshold voltage. A logic low is asserted when the input falls below the low-battery threshold voltage. The $\overline{\text{LBO}}$ output remains low until V_{IN} is above the low-battery threshold voltage plus the low-battery hysteresis voltage. $\overline{\text{LBO}}$ is high impedance when $\overline{\text{SHDN}}$ is low or when $\overline{\text{BYPASS}}$ is low (MCP1259).

3.2 Mode Selection ($\overline{\text{SLEEP}}$, $\overline{\text{BYPASS}}$)

3.2.1 ACTIVE LOW SLEEP MODE ($\overline{\text{SLEEP}}$)

MCP1256/7: A logic low signal applied to this pin places the device into a SLEEP mode of operation. In this mode, the device maintains regulation. SLEEP mode performs pulse skip operation reducing the current draw of the device at the expense of increased output voltage ripple.

3.2.2 ACTIVE LOW BYPASS MODE ($\overline{\text{BYPASS}}$)

MCP1258/9: A logic low signal applied to this pin places the device into a BYPASS mode of operation. In this mode, the input supply voltage is connected directly to the output.

3.3 Flying Capacitor Negative (C2-)

A 1 µF ceramic flying capacitor is recommended.

3.4 Flying Capacitor Positive (C1+)

A 1 µF ceramic flying capacitor is recommended.

3.5 Regulated Output Voltage (V_{OUT})

Regulated 3.3V output. Bypass to GND with a minimum of 2.2 µF.

3.6 Flying Capacitor Positive (C2+)

A 1 µF ceramic flying capacitor is recommended.

3.7 Power Supply Input Voltage (V_{IN})

A supply voltage of 1.8V to 3.6V is recommended. Bypass to GND with a minimum of 1 µF.

3.8 Flying Capacitor Negative (C1-)

A 1 µF ceramic flying capacitor is recommended.

3.9 0V Reference (GND)

Connect to negative terminal of and input supply.

3.10 Device Shut Down ($\overline{\text{SHDN}}$)

A logic low signal applied to this pin disables the device. A logic high signal applied to this pin allows normal operation.

4.0 DEVICE OVERVIEW

The MCP1256/7/8/9 devices are positive regulated charge pumps that accept an input voltage from +1.8V to +3.6V and convert it to a regulated 3.3V output voltage. The MCP1256/7/8/9 provide a low-cost, compact and simple solution for step-up DC/DC conversions, primarily in battery applications, that do not want to use switching regulator solutions because of EMI noise and inductor size.

The MCP1256/7/8/9 are designed to offer the highest possible efficiency under common operating conditions, i.e. $V_{IN} = 2.4V$ or $2.8V$, $V_{OUT} = 3.3V$, $I_{OUT} = 100$ mA. A fixed switching frequency, 650 kHz typically, allows for easy external filtering.

The MCP1256/7 provide a unique SLEEP mode feature which reduces the current drawn from the input supply while maintaining a regulated bias on external peripherals. SLEEP mode can substantially increase battery run-time in portable applications.

The MCP1258/9 provide a unique BYPASS mode feature which virtually eliminates the current drawn from the input supply by the device while maintaining an unregulated bias on external peripherals. BYPASS connects the input supply voltage to the output. All remaining functions of the device are shutdown. BYPASS mode can substantially increase battery run-time in portable applications.

The devices supply up to 100 mA of output current for input voltages, V_{IN}, greater than or equal to 2.2V. The devices are available in small 10-Pin MSOP or DFN packages with an operating junction temperature range of -40°C to +125°C.

4.1 Theory of Operation

The MCP1256/7/8/9 devices employ a switched capacitor charge pump to boost an input supply, V_{IN}, to a regulated 3.3V output voltage. Refering to the Functional Block Diagram, the devices perform conversion and regulation in two phases: charge and transfer. When the devices are not in shutdown, SLEEP or BYPASS, the two phases are continuously cycled through.

Charge transfers charge from the input supply to the flying capacitors, C_1 and C_2, connected to pins C_1+, C_1-, C_2+ and C_2-, respectively. During this phase, switches S4 and S6 are closed. Switch S2 controls the amount of charge transferred to the flying capacitors. The amount of charge is determined by a sample and hold error amplifier with feedback from the output voltage at the beginning of the phase.

Once the first phase (charge) is complete, transfer is initiated. The second phase transfers the energy from the flying capacitors to the output. The MCP1256/7/8/9 devices autonomously switch between 1.5x mode and 2x mode. This determines whether the flying capacitors are placed in parallel (1.5x mode), or remain in series (2x mode), when the energy is transferred to the output. The transfer mode determines which switches are closed for the transfer.

Both phases occur in one clock period of the internal oscillator. When the second phase (transfer) has been completed, the cycle repeats.

4.2 Power Efficiency

The power efficiency, η, is determined by the mode of operation, 1.5x mode or 2x mode. Equation 4-1 and Equation 4-2 are used to approximate the power efficiency with any significant amount of output current. At light loads, the device quiescent current must be taken into consideration.

EQUATION 4-1:

$$\eta_{1.5x} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times 1.5 \times I_{OUT}} = \frac{V_{OUT}}{V_{IN} \times 1.5}$$

EQUATION 4-2:

$$\eta_{2x} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times 2 \times I_{OUT}} = \frac{V_{OUT}}{V_{IN} \times 2}$$

4.3 Shutdown Mode ($\overline{\text{SHDN}}$)

Driving $\overline{\text{SHDN}}$ low places the MCP1256/7/8/9 in a low-power Shutdown mode. This disables the charge-pump switches, oscillator and control logic, reducing the quiescent current to 0.25 µA (typical). The PGOOD output and $\overline{\text{LBO}}$ are in a high impedance state during shutdown.

4.4 SLEEP Mode ($\overline{\text{SLEEP}}$)

The MCP1256/7 provide a unique SLEEP mode feature. SLEEP mode reduces the current drawn from the input supply while maintaining a regulated bias on external peripherals. SLEEP mode can substantially increase battery run-time in portable applications.

The regulation control is referred to as a bang-bang control due to the output being regulated around a fixed reference with some hysteresis. As a result, some amount of peak-to-peak ripple will be observed at the output independent of load current. The frequency of the output ripple, however, will be influenced heavily by the load current and output capacitance.

4.5 BYPASS Mode ($\overline{\text{BYPASS}}$)

The MCP1258/9 provide a unique BYPASS mode feature which virtually eliminates the current drawn from the input supply by the device, while maintaining an unregulated bias on external peripherals. BYPASS connects the input supply voltage to the output. All remaining functions of the device are shutdown. BYPASS mode can substantially increase battery run-time in portable applications.

4.6 Power-Good Output (PGOOD)

For the MCP1256/8 devices, the PGOOD output is an open-drain output that sinks current when the regulator output voltage falls below $0.93V_{OUT}$ (typical). If the regulator output voltage falls below $0.93V_{OUT}$ (typical) for less than 200 µs and then recovers, glitch immunity circuits prevent the PGOOD signal from transitioning low. A 10 kΩ to 1 MΩ pull-up resistor from PGOOD to V_{OUT} may be used to provide a logic output. If not used, connect PGOOD to GND or leave unconnected.

PGOOD is high impedance when the output voltage is in regulation. A logic low is asserted when the output falls 7% (typical) below the nominal value. The PGOOD output remains low until V_{OUT} is within 3% (typical) of its nominal value. On start-up, this pin indicates when the output voltage reaches its final value. PGOOD is high impedance when SHDN is low or when BYPASS is low (MCP1258).

4.7 Low-Battery Output (LBO)

For the MCP1257/9 devices, the LBO output is an open-drain output that sinks current when the input voltage falls below a preset threshold. If the input voltage falls below the preset threshold for less than 200 µs and then recovers, glitch immunity circuits prevent the LBO signal from transitioning low. A 10 kΩ to 1 MΩ pull-up resistor from LBO to V_{OUT} may be used to provide a logic output. If not used, connect LBO to GND or leave unconnected.

LBO is high impedance when the input voltage is above the low-battery threshold voltage. A logic low is asserted when the input falls below the low-battery threshold voltage. The LBO output remains low until V_{IN} is above the low-battery threshold voltage plus the low-battery hysteresis voltage. LBO is high impedance when SHDN is low or when BYPASS is low (MCP1259).

4.8 Soft-Start and Short-Circuit Protection

The MCP1256/7/8/9 devices feature fold back short-circuit protection. This circuitry provides an internal soft-start function by limiting inrush current during startup and also limits the output current to 150 mA (typical), if the output is short-circuited to GND. The internal soft-start circuitry requires approximately 175 µs, typical, from either initial power-up, release from Shutdown, or release from BYPASS (MCP1258/9) for the output voltage to be in regulation.

4.9 Thermal Shutdown

The MCP1256/7/8/9 devices feature thermal shutdown with temperature hysteresis. When the die temperature exceeds 160°C, the device shuts down. When the die cools by 15°C, the MCP1256/7/8/9 automatically turns back on again. If high die temperature is caused by output overload and the load is not removed, the device will turn on and off resulting in a pulsed output.

5.0 APPLICATIONS

5.1 Capacitor Selection

The style and value of capacitors used with the MCP1256/7/8/9 family determine several important parameters, such as output voltage ripple and charge pump strength. To minimize noise and ripple, it is recommended that low ESR (0.1Ω) capacitors be used for both C_{IN} and C_{OUT}. These capacitors should be ceramic and should be 10 µF or higher for optimum performance.

If the source impedance to V_{IN} is very low, up to several megahertz, C_{IN} may not be required. Alternatively, a somewhat smaller value of C_{IN} may be substituted for the recommended 10 µF, but will not be as effective in preventing ripple on the V_{IN} pin.

The value of C_{OUT} controls the amount of output voltage ripple present on V_{OUT}. Increasing the size of C_{OUT} will reduce output ripple at the expense of a slower turn-on time from shutdown and a higher inrush current.

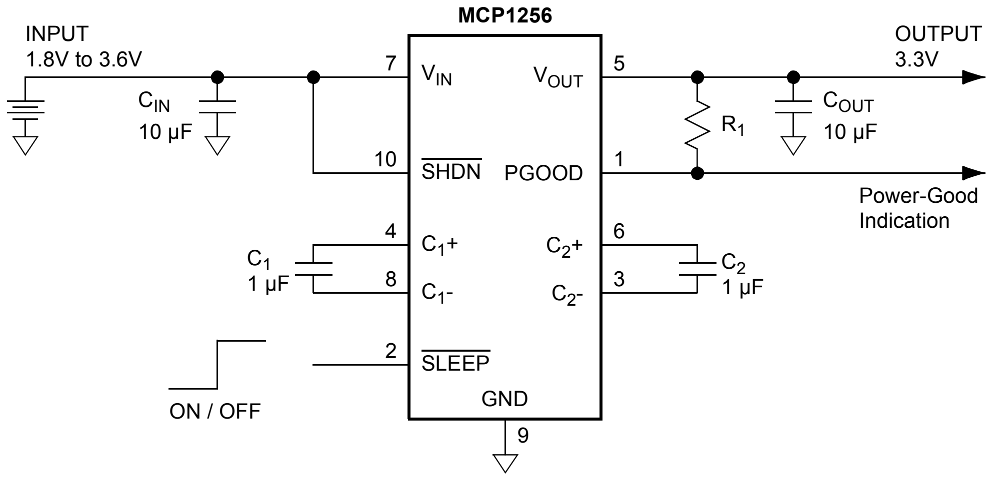
The flying capacitors (C_1 and C_2) control the strength of the charge pump and in order to achieve the maximum rated output current (100 mA), it is necessary to have at least 1 µF of capacitance for the flying capacitor. A smaller flying capacitor delivers less charge per clock cycle to the output capacitor resulting in lower available output current.

5.2 PCB Layout Issues

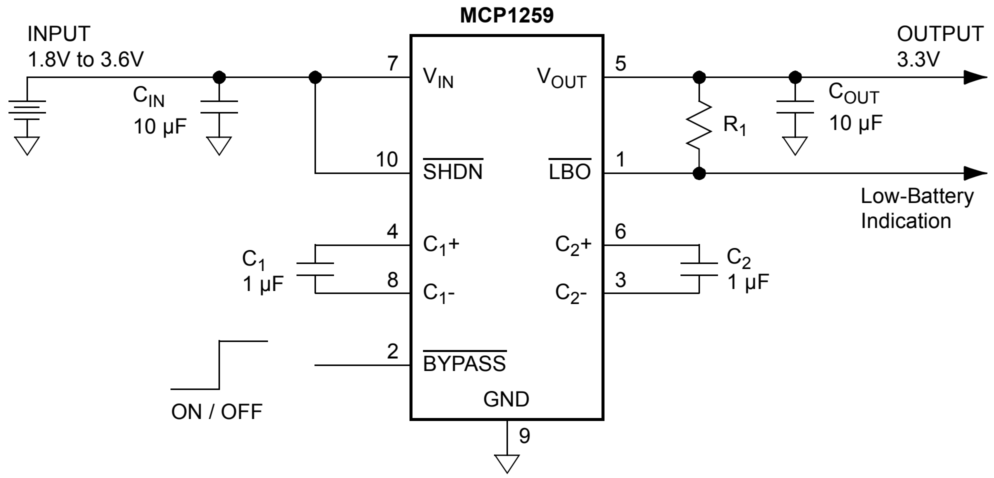
The MCP1256/7/8/9 devices transfer charge at high switching frequencies producing fast, high peak, transient currents. As a result, any stray inductance in the component layout will produce unwanted noise in the system. Proper board layout techniques are required to ensure optimum performance.

6.0 TYPICAL APPLICATION CIRCUITS

The MCP1256/7/8/9 devices are inductorless, positive regulated, switched capacitor DC/DC converters. Typical application circuits are depicted in Figure 6-1.



Typical Application with Power-Good Indication



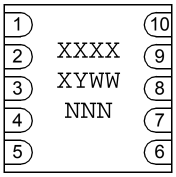
Typical Application with Low-Battery Indication

FIGURE 6-1: *Typical Application Circuits.*

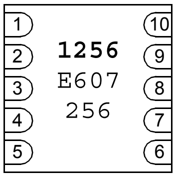
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

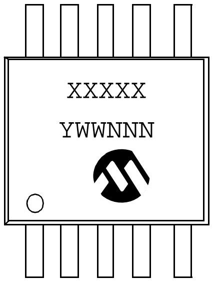
10-Lead DFN



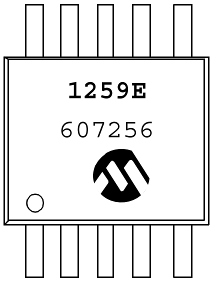
Example:



10-Lead MSOP



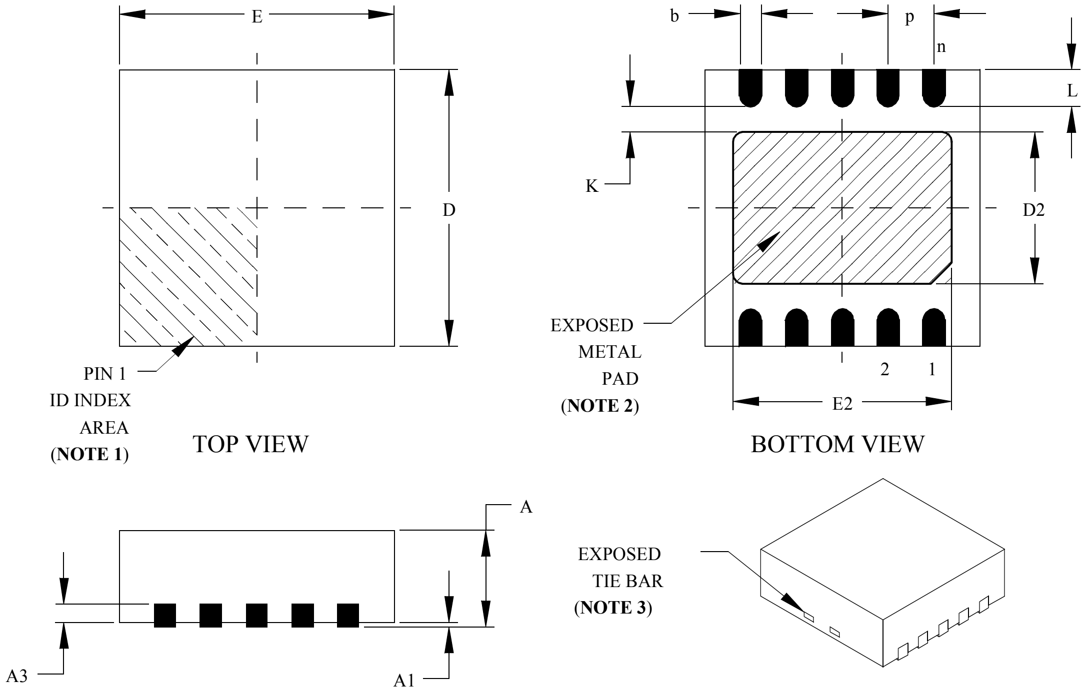
Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Dual-Flat No-Lead Package (MF) 3x3x0.9 mm Body (DFN) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		10			10	
Pitch	e		.020 BSC			0.50 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Lead Thickness	A3		.008 REF.			0.20 REF.	
Overall Length	E	.112	.118	.124	2.85	3.00	3.15
Exposed Pad Length **(Note 3)**	E2	.082	.094	.096	2.08	2.39	2.45
Overall Width	D	.112	.118	.124	2.85	3.00	3.15
Exposed Pad Width **(Note 3)**	D2	.051	.065	.067	1.30	1.65	1.70
Lead Width	b	.008	.010	.015	0.18	0.25	0.30
Contact Length §	L	.012	.016	.020	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	.008	—	—	0.20	—	—

* Controlling Parameter

§ Significant Characteristic

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Exposed pad varies according to die attach paddle size.

3. Package may have one or more exposed tie bars at ends.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

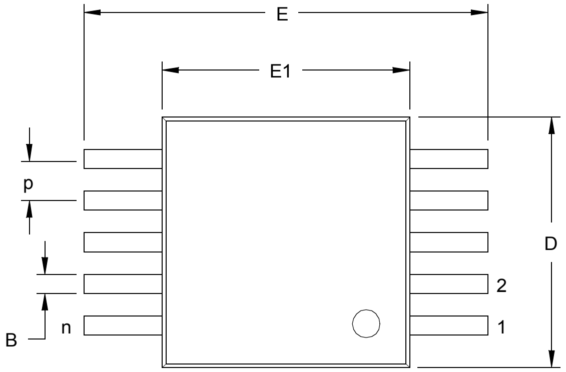
REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

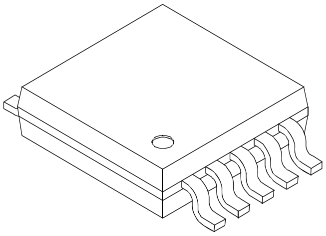
JEDEC equivalent: Not Registered

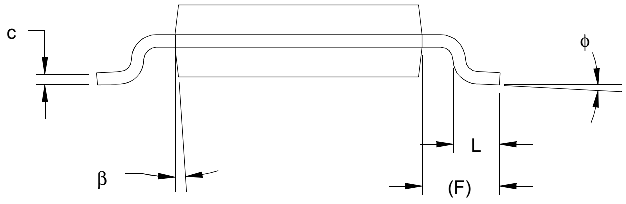
Drawing No. C04-063

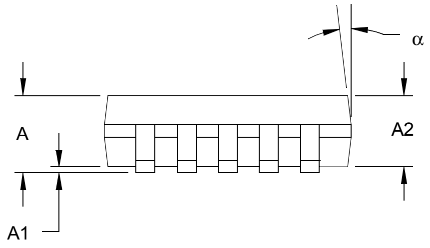
Revised 09-12-05

10-Lead Plastic Micro Small Outline Package (UN) (MSOP)









Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		10			10	
Pitch	p	.020 BSC			0.50 BSC		
Overall Height	A			.043	–	–	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000		.006	0.00		0.15
Overall Width	E	.193 BSC			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint	F	.037 REF			0.95 REF		
Foot Angle	φ	0°	–	8°	0°	–	8°
Lead Thickness	c	.003	–	.009	0.08	–	0.23
Lead Width	B	.006	.009	.012	0.15	0.23	0.30
Mold Draft Angle Top	α	5°	–	15°	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°	5°	–	15°

* Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254 mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC Equivalent: MO-187 BA
Drawing No. C04-021

Revised 09-16-05

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2006)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**X**	**/XX**
Device	**Temperature Range**	**Package**

Device	MCP1256:	Positive Regulated Charge Pump with SLEEP Mode and Power-Good Indication
	MCP1256T:	Positive Regulated Charge Pump with SLEEP Mode and Power-Good Indication, Tape and Reel
	MCP1257:	Positive Regulated Charge Pump with SLEEP Mode and Low-Battery Indication
	MCP1257T:	Positive Regulated Charge Pump with SLEEP Mode and Low-Battery Indication, Tape and Reel
	MCP1258:	Positive Regulated Charge Pump with BYPASS Mode and Power-Good Indication
	MCP1258T:	Positive Regulated Charge Pump with BYPASS Mode and Power-Good Indication, Tape and Reel
	MCP1259:	Positive Regulated Charge Pump with BYPASS Mode and Low-Battery Indication
	MCP1259T:	Positive Regulated Charge Pump with BYPASS Mode and Low -Battery Indication, Tape and Reel
Temperature Range	E	= -40°C to +125°C
Package	MF	= Dual Flat, No Lead (3x3 mm body), 10-Lead
	UN	= Plastic Micro Small Outline (MSOP), 10-Lead

Examples:

a)	MCP1256-EMF:	E-Temp, DFN package
b)	MCP1256T-EMF:	Tape and Reel, E-Temp, DFN package
c)	MCP1256-EUN:	E-Temp, MSOP package
d)	MCP1256T-EUN:	Tape and Reel, E-Temp, MSOP package

a)	MCP1257-EMF:	E-Temp, DFN package
b)	MCP1257T-EMF:	Tape and Reel, E-Temp, DFN package
c)	MCP1257-EUN:	E-Temp, MSOP package
d)	MCP1257T-EUN:	Tape and Reel, E-Temp, MSOP package

a)	MCP1258-EMF:	E-Temp, DFN package
b)	MCP1258T-EMF:	Tape and Reel, E-Temp, DFN package
c)	MCP1258-EUN:	E-Temp, MSOP package
d)	MCP1258T-EUN:	Tape and Reel, E-Temp, MSOP package

a)	MCP1259-EMF:	E-Temp, DFN package
b)	MCP1259T-EMF:	Tape and Reel, E-Temp, DFN package
c)	MCP1259-EUN:	E-Temp, MSOP package
d)	MCP1259T-EUN:	Tape and Reel, E-Temp, MSOP package

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