1 Orderable Parts

Table 1. Device Variations

Part Number [1]	Temperature (T_A)	Package	Boost Switch Current Limit I_{BOOST_LIMIT} (A)			Switching Frequency f_S (kHz)			Slope Compensation V_{SLOPE} (V/µs)		
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
MC34845EP	-40 to 85 °C	24 QFN-EP	1.9	2.1	2.3	540	600	660	-	0.52	-
MC34845AEP			1.9	2.1	2.3	1080	1200	1320	-	0.73	-
MC34845BEP			2.1	2.35	2.6	270	300	330	-	0.22	-
MC34845CEP			1.9	2.1	2.3	540	600	660	-	0.52	-
MC34845DEP			2.1	2.35	2.6	270	300	330	-	0.22	-

Notes
1. To order parts in Tape and Reel, add the R2 suffix to the part number.

INTERNAL BLOCK DIAGRAM

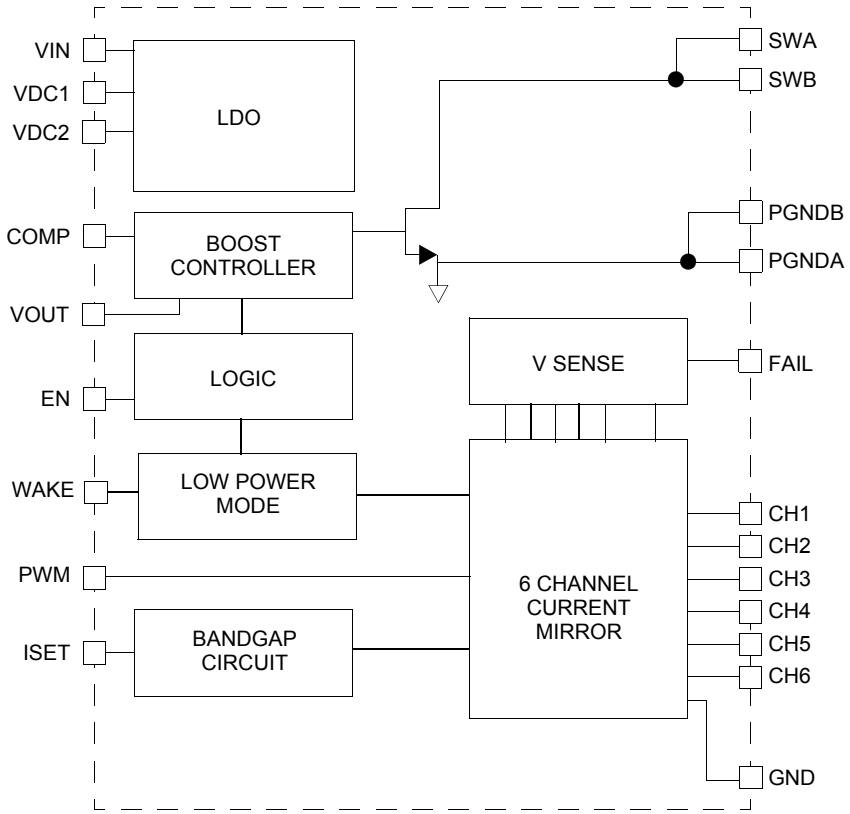


Figure 2. 34845 Simplified Internal Block Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Maximum Pin Voltages	V_{MAX}		V
SWA, SWB, VOUT		-0.3 to 65	
CH1, CH2, CH3, CH4, CH5, CH6 (Off state)		-0.3 to 45	
CH1, CH2, CH3, CH4, CH5, CH6 (On state)		-0.3 to 20	
FAIL		-0.3 to 7.0	
OVP		-0.3 to 7.75	
COMP, ISET		-0.3 to 2.7	
PWM, WAKE		-0.3 to 5.5	
EN, VIN		-0.3 to 24	
Maximum LED Current per Channel	I_{LED_MAX}	33	mA
ESD Voltage[2]	V_{ESD}		V
Human Body Model (HBM)		±2000	
Machine Model (MM)		±200	
THERMAL RATINGS			
Operating Ambient Temperature Range	T_A	-40 to 85	°C
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_S	-40 to 150	°C
Peak Package Reflow Temperature During Reflow[3], [4]	T_{PPRT}	Note 4	°C
Thermal Resistance Junction to Ambient[5]	$T_{\theta JA}$	36	°C/W
Thermal Resistance Junction to Case[6]	$T_{\theta JC}$	3.1	°C/W
Power Dissipation[5]	P_D		W
T_A = 25°C		3.4	
T_A = 85°C		1.8	

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (AEC-Q100-2) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
5. Per JEDEC51-8 Standard for Multilayer PCB.
6. Theoretical thermal resistance is from the die junction to the exposed pad.

STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS

Table 3. Static and Dynamic Electrical Characteristics

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40°C ≤ T_A ≤ 85°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY					
Supply Voltage	V_{IN}	5.0	10	21	V
Supply Current when in Shutdown Mode EN = Low, PWM = Low	$I_{SHUTDOWN}$	-	2.0	10	μA
Supply Current when Operational Mode Boost = Pulse Skipping, Channels = 1% of Duty Cycle EN = High, PWM = Low	$I_{OPERATIONAL}$	-	5.0	6.5	mA
Under-voltage Lockout V_{IN} Rising	UVLO	4.0	-	4.4	V
Under-voltage Hysteresis V_{IN} Falling	$UVLO_{HYST}$	-	0.25	-	V
VDC1 Voltage[7] C_{VDC1} = 2.2 μF	V_{DC1}	2.4	2.5	2.6	V
VDC2 Voltage[7] (V_{IN} between 7.0 and 21 V) C_{VD2C} = 2.2 μF	V_{DC2}	5.7	6.0	6.3	V
BOOST					
Output Voltage Range[8] VIN = 5.0 V VIN = 21 V	 V_{OUT1} V_{OUT2}	 8.0 24	 - -	 43 60	V
Boost Switch Current Limit 34845, 34845A, 34845C 34845B, 34845D	I_{BOOST_LIMIT}	 1.9 2.1	 2.1 2.35	 2.3 2.6	A
Boost Switch Current Limit Timeout	t_{BOOST_TIME}	-	10	-	ms
RDSON of Internal FET I_{DRAIN}= 1.0 A	R_{DSON}	-	300	520	mΩ
Boost Switch Off state Leakage Current $V_{SWA,SWB}$ = 60 V	I_{BOOST_LEAK}	-	-	1.0	μA
Feedback pin Off-state Leakage Current V_{OUT} = 60 V	$VOUT_{LEAK}$	-	-	500	μA
Peak Boost Efficiency[9] V_{OUT} = 33 V, RL = 330 Ω	EFF_{BOOST}	-	90	-	%

Notes

7. This output is for internal use only and not to be used for other purposes.
8. Minimum and maximum output voltages are dependent on Min/Max duty cycle condition.
9. Boost efficiency test is performed under the following conditions: f_{SW} = 600 kHz, V_{IN} = 12 V, V_{OUT} = 33 V and R_L = 330 Ω. The following external components are used: L = 10 μH DCR = 0.1 Ω, C_{OUT} = 3x1 μF (ceramic), Schottky diode V_F = 0.35 V.

Table 3. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40°C ≤ T_A ≤ 85°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BOOST (CONTINUED)					
Line Regulation V_{IN} = 7.0 V to 21 V, I_{CH} = 30 mA	I_{LED}/V_{IN}	-0.2	-	0.2	%/V
Load Regulation V_{LED} = 24 V to 40 V (all Channels), I_{CH} = 30 mA	I_{LED}/V_{LED}	-0.2	-	0.2	%/V
Minimum Duty Cycle	D_{MIN}	-	10	15	%
Maximum Duty Cycle	D_{MAX}	88	90	-	%
OVP Internally Fixed Value (no external voltage resistor divider)	V_{OVP_INT}	56	60	64	V
OVP Programming Range[10] (set through an external resistor divider)	V_{OVP_EXT}	15	-	60	V
OVP Reference Voltage	V_{REF_OVP}	6.3	6.9	7.5	V
OVP Sink Current	I_{SINK_OVP}	-	0.2	-	µA
Switching Frequency 34845, 34845C 34845A 34845B, 34845D	f_S	 540 1080 270	 600 1200 300	 660 1320 330	kHz
Soft Start Time (Fs=600 kHz, 100% PWM duty)	t_{SS}	-	3.0	-	ms
Soft Start VOUT Overshoot (Fs=600 kHz, 100% PWM duty)	SS_V_{OUT}	-	-	OVP	V
Boost Switch Rise Time	$BOOST\_t_R$	-	8.0	-	ns
Boost Switch Fall Time	$BOOST\_t_F$	-	6.0	-	ns
Current sense Amplifier Gain	A_{CSA}	-	9.0	-	
OTA Transconductance	G_M	-	200	-	µS
Transconductance Sink and Source Current Capability	I_{SS}	-	100	-	µA
Slope Compensation 34845, 34845C 34845A 34945B, 34845D	V_{SLOPE}	 - - -	 0.52 0.73 0.22	 - - -	V/µs

Notes
10. The OVP level must be set 5.0 V above the worst-case LED string voltage.

Table 3. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40°C ≤ T_A ≤ 85°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LED DRIVER					
LED Driver Sink Current	I_{LED}				mA
R_{ISET} = 51 kΩ 0.1%, PWM = 3.3 V		2.88	3.0	3.12	
R_{ISET} = 5.1 kΩ 0.1%, PWM = 3.3 V		29.4	30	30.6	
ISET Pin Voltage	V_{ISET}				V
R_{ISET} = 5.1 kΩ 0.1%		2.011	2.043	2.074	
Regulated Minimum Voltage Across LED Drivers	V_{MIN}				V
Pulse Width > 400ns		0.675	0.75	0.825	
LED Current Channel to Channel Tolerance	$I_{TOLERANCE}$				%
10 mA ≤ I_{LED} ≤ 30 mA		-2.0	-	2.0	
3.0 mA ≤ I_{LED} < 10 mA		-4.0	-	4.0	
Off State leakage Current, All Channels	I_{CH_LEAK}				µA
V_{CH} = 45 V		-	-	1.0	
LED Channels Rise and Fall Time	t_R/t_F	-	50	75	ns
LED Open Protection, Channel Disabled if $V_{CH} \leq O_{FDV}$	O_{FDV}	-	-	0.55	V
LED Short Protection Voltage, Channel Disabled if $V_{CH} \geq S_{FDV}$	S_{FDV}				V
(channel on time ≥ 10 µs)		6.5	7.0	7.5	
FAIL PIN					
Off State Leakage Current	I_{FAIL_LEAK}				µA
V_{FAIL} = 5.5 V		-	-	5.0	
On State Voltage Drop	V_{OL}				V
I_{SINK} = 4.0 mA		-	-	0.4	
OVER-TEMPERATURE SHUTDOWN					
Over-temperature Threshold (shutdown mode)	$OTT_{SHUTDOWN}$				°C
Rising		150	165	-	
Hysteresis		-	25	-	
PWM INPUT					
PWM Dimming Mode LED Current Control	$PWM_{CONTROL}$				%
PWM = 3.3 V, f_{PWM} = 600 Hz 10% duty;		9.9	10	10.1	
PWM = 3.3 V, f_{PWM} = 600 Hz 50% duty		49.5	50	50.5	
PWM = 3.3 V, f_{PWM} = 600 Hz 100% duty		-	100	-	
Input Minimum Pulse PWM Pin (V_{PWM}=3.3 V)	t_{PWM_IN}				µs
Start-up (Wake Mode)		1.6	-	-	
Operational (Wake Mode)		-	0.2	-	
Start-up (Enable Mode)		0.4	-	-	
Operational (Enable Mode)		-	0.2	-	
Input Frequency Range for PWM Pin	f_{PWM}	DC	-	100	kHz
WAKE					
Shutdown Mode Timeout	$t_{SHUTDOWN}$	27	30	33	ms

Table 3. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40°C ≤ T_A ≤ 85°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS (PWM)					
Input Low Voltage	V_{ILL}	-0.3	-	0.5	V
Input High Voltage	V_{IHL}	1.5	-	5.5	V
Input Current	I_{SINK}	-1.0	-	1.0	µA
LOGIC INPUTS (EN)					
Input Low Voltage	V_{ILL}	-0.3	-	0.5	V
Input High Voltage	V_{IHL}	2.1	-	21	V
Input Current (V_{EN} = 12 V)	I_{SINK}	-	6.0	10	µA
LOGIC INPUTS (WAKE)					
Input Low Voltage	V_{ILL}	-0.3	-	0.5	V
Input High Voltage	V_{IHL}	2.1	-	5.5	V
Input Current	I_{SINK}	-1.0	-	1.0	µA

PIN CONNECTIONS

TRANSPARENT
TOP VIEW

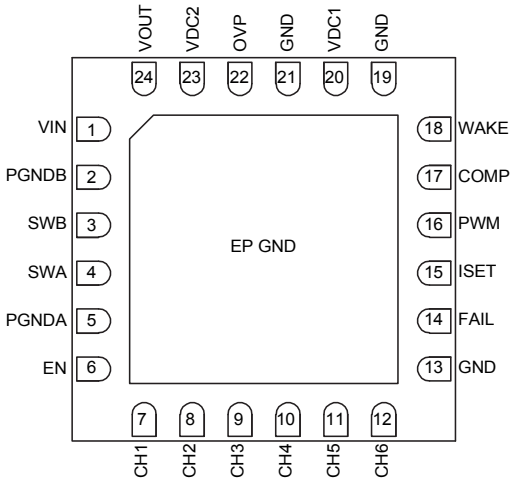


Figure 3. 34845 Pin Connections

Table 4. 34845 Pin Definitions

Pin Number	Pin Name	Definition
1	VIN	Main voltage supply Input. IC Power input supply voltage, is used internally to produce internal voltage regulation for logic functioning, and also as an input voltage for the boost regulator.
2	PGNDB	Power ground. This is the ground terminal for the internal Boost FET.
3	SWB	Boost switch node connection B. Switching node of boost converter.
4	SWA	Boost switch node connection A. Switching node of boost converter.
5	PGNDA	Power ground. This is the ground terminal for the internal Boost FET.
6	EN	Enable pin (active high, internal pull-down).
7 - 12	CH1 - CH6	LED string connections 1 to 6. LED current drivers. Each line has the capability of driving up to 30 mA.
13, 19, 21	GND	Ground Reference for all internal circuits other than the Boost FET. The Exposed Pad (EP) should be used for thermal heat dissipation.
14	FAIL	Fault detected pin (open drain): No Failure = Low-impedance pull-down Failure = High-impedance When a fault situation is detected, this pin goes into high impedance.
15	ISET	LED current setting. The maximum current is set using a resistor from this pin to GND.
16	PWM	External PWM control signal.
17	COMP	Boost compensation component connection. This passive terminal is used to compensate the boost converter. Add a capacitor and a resistor in series to GND to stabilize the system as well as a shunt capacitor.
18	WAKE	Low power consumption mode for single wire control. This is achieved by connecting the WAKE and PWM pins together and grounding the ENABLE (EN) pin.
20	VDC1	2.5 V internal voltage decoupling. This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground.
22	OVP	External boost over-voltage setting. Requires a resistor divider from VOUT to GND. If no external OVP setting is desired, this pin should be grounded.
23	VDC2	6.0 V internal voltage decoupling. This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground.
24	VOUT	Boost voltage output feedback.
EP	EP	Ground and thermal enhancement pad

FUNCTIONAL DESCRIPTION

INTRODUCTION

LED backlighting has been popular for use in small LCD displays for many years. This technology is now rapidly replacing the incumbent Cold Cathode Fluorescent Lamp (CCFL) in mid-size displays such as those used use in notebooks, monitors and industrial/ consumer displays. LEDs offer a number of advantages compared to the CCFL, including lower power, thinner, longer lifetime, low voltage drive, accurate wide-range dimming control and advanced architectures for improved image quality. LEDs are also void of hazardous materials such as mercury which is used in CCFL.

LED backlights use different architecture depending on the size of the display and features required. For displays in the 10” to 17” + range such as those used in notebooks, edge-lit backlights offer very thin designs down to 2mm or less. The efficiency of the LED backlight also extends battery life in portable equipment compared to CCFL. In large size panels, direct backlights support advanced architectures such as local dimming, in which power consumption and contrast ratio are drastically improved. Edge lighting can also be used in large displays when low cost is the driving factor.

The 34845 targets mid size panel applications in the 10” to 17” + range with edge-lit backlights. The device supports LED currents up to 30mA and supports up to six strings of LEDs. This enables backlights up to 10W to be driven from a single device. The device includes a boost converter to deliver the required LED voltage from either a 2 or 3 cell Li-ion battery, or a direct 12V input supply. The current drivers match the current between devices to provide superior uniformity across the display. The 34845 provides for a wide range of PWM dimming from a direct PWM control input.

FUNCTIONAL DEVICE OPERATION

POWER SUPPLY

The 34845 supports 5.0V to 21V at the VIN input pin. Two internal regulators generate internal rails for internal operation. Both rails are de-coupled using capacitors on the VDC1 and VDC2 pins.

The VIN, VDC1, and VDC2 supplies each have their own UVLO mechanisms. When any voltage is below the UVLO threshold, the device stops operating. All UVLO comparators have hysteresis to ensure constant on/off cycling does not occur.

The power up sequence for applying VIN respect to the ENABLE and PWM signals is important since the 34845 device will behave differently depending on how the sequence of these signals is applied. For the case where VIN is applied before the ENABLE and PWM signals, the device will have no limitation in terms of how fast the VIN ramp should be. However for the case where the PWM and ENABLE signals are applied before VIN, the ramp up time of VIN between 0V and 5V should be no longer than 2ms. Figures 4 and 5 illustrate the two different power up conditions.

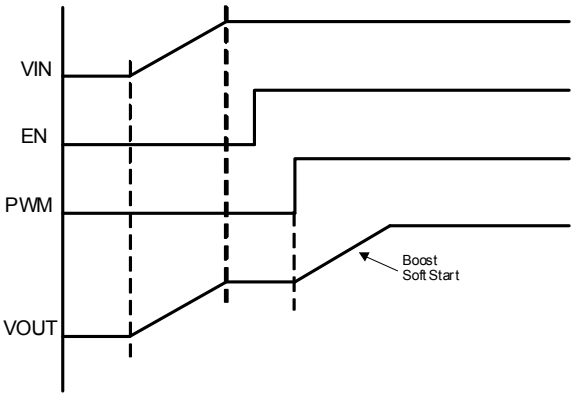


Figure 4. Power up sequence case 1, VIN applied before the ENABLE and PWM signals. No limitation for VIN ramp up time.

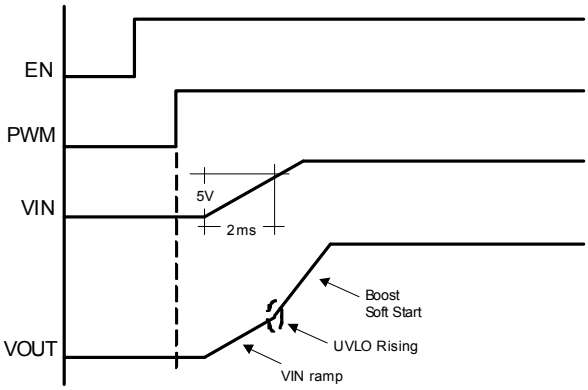


Figure 5. Power up sequence case 2, VIN applied after the ENABLE and PWM signals. VIN ramp up time between 0V and 5V should be not higher than 2ms

BOOST CONVERTER

The boost converter uses a Dynamic Headroom Control (DHC) loop to automatically set the output voltage needed to drive the LED strings. The DHC is designed to operate under specific pulse width conditions in the LED drivers. It operates for pulse widths higher than 400 ns. If the pulse widths are shorter than specified, the DHC circuit will not operate and the voltage across the LED drivers will increase to a value given by the OVP, minus the total LED voltage in the LED string. It is therefore imperative to select the proper OVP level to avoid exceeding the max off state voltage of the LED drivers (45V).

The boost operates in current mode and is compensated externally through a type 2 network on the COMP pin. A modification of the compensation network is suggested to minimize the amplitude of the ripple at V_{OUT}. The details of the suggested compensation network are shown in Figures 10 and 11.

An integrated 2.0A minimum FET supplies the required output current. An Over-current Protection circuit limits the output current cycle-by-cycle to I_{OCP}. If the condition exists longer than 10 ms, then the device will shut down. The frequency of the boost converter is internally set to 300 kHz, 600 kHz or 1.2 MHz, depending on the device's version.

The boost also includes a soft start circuit. Each time the IC comes out of shutdown mode, the soft start period lasts for t_{SS}.

Over-voltage Protection is also included. The device has an internally fixed OVP value of 60V (typical) which serves as a secondary fault protection mechanism, in the event the externally programmed OVP fails (i.e. resistor divider opens up). While the internal 60V OVP detector can be used exclusively without the external OVP network, this is only recommended for applications where the LED string voltage approaches 55 V or more. The OVP level can be set by using an external resistor divider connected between the output voltage and ground with its output connected to the OVP pin. The OVP can be set up to 60V by varying the resistor divider to match the OVP internal reference of 6.9V (typical).

LED DRIVER

The six channel LED driver provides current matching for six LED strings to within ±2% maximum. The current in the strings is set using a resistor tied to GND from the ISET pin. The LED current level is given by the equation: RSET = 153/ ILED. The accuracy of the RSET resistor should be 0.1% for best performance.

LED ERROR DETECT

If an LED is open, the output voltage ramps to the OVP level. If there is still no current in the LED string, the LED channel is turned off and the output voltage ramps back down to normal operating level.

If LEDs are shorted and the voltage in any of the channels is greater than the SFDV threshold (7.0 V typical), then the device will turn off that channel. However if the on-time of the channels is less than 10 μs, the SFDV circuit will not disable any of the channels, regardless of the voltage across them.

All the LED errors can be cleared by recycling the EN pin or applying a complete power-on-reset (POR).

WAKE OPERATION

The WAKE pin provides the means to set the device for low power consumption (shutdown mode) without the need of an extra logic signal for enable. This is achieved by connecting the WAKE and PWM pins together, and tying the EN pin to ground. In this configuration, the PWM signal is used to control the LED channels, while allowing low power consumption by setting the device into its shutdown mode every time the PWM signal is kept low for longer time than the WAKE time out of 27 ms.

OVER-TEMPERATURE SHUTDOWN AND TEMPERATURE CONTROL CIRCUITS

The 34845 includes over-temperature protection. If the internal temperature exceeds the over-temp threshold $OTT_{SHUTDOWN}$, then the device shuts down all functions. Once the temperature falls below the low level threshold, the device is re-enabled.

FAIL PIN

The FAIL pin is at its low-impedance state when no error is detected. However, if an error such as an LED channel open or boost over-current is detected, the FAIL pin goes into high-impedance. Once a failure is detected, the FAIL pin can be cleared by recycling the EN pin or applying a complete power-on-reset (POR). If the detected failure is an Over-current time-out, the EN pin or a POR must be cycled/executed to restart the part.

TYPICAL PERFORMANCE CURVES

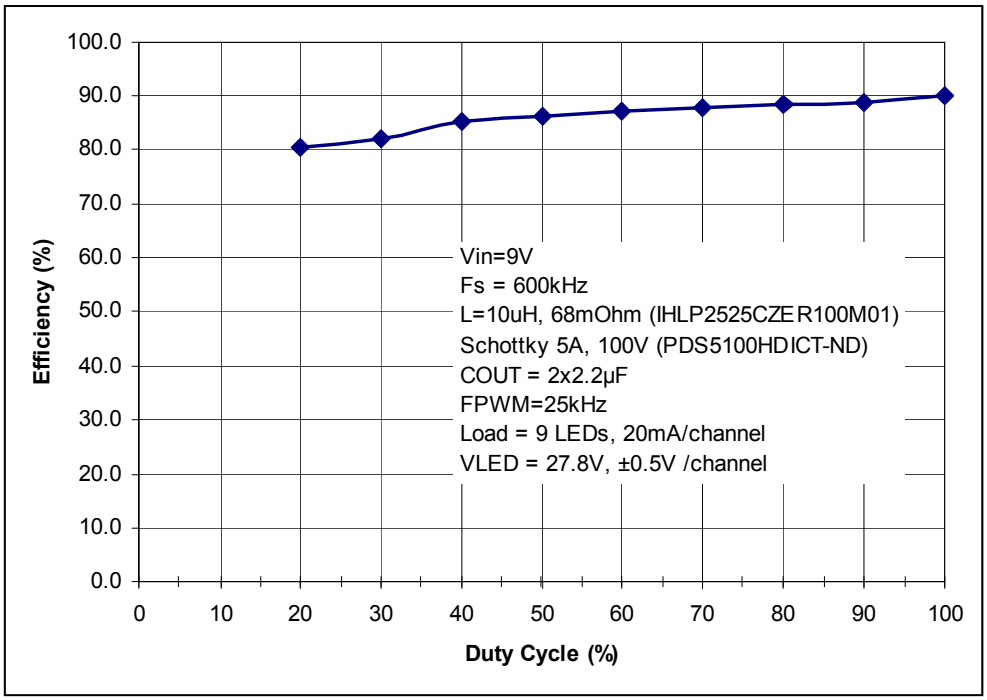


Figure 6. Typical System Efficiency vs Duty Cycle (FPWM=25kHz)

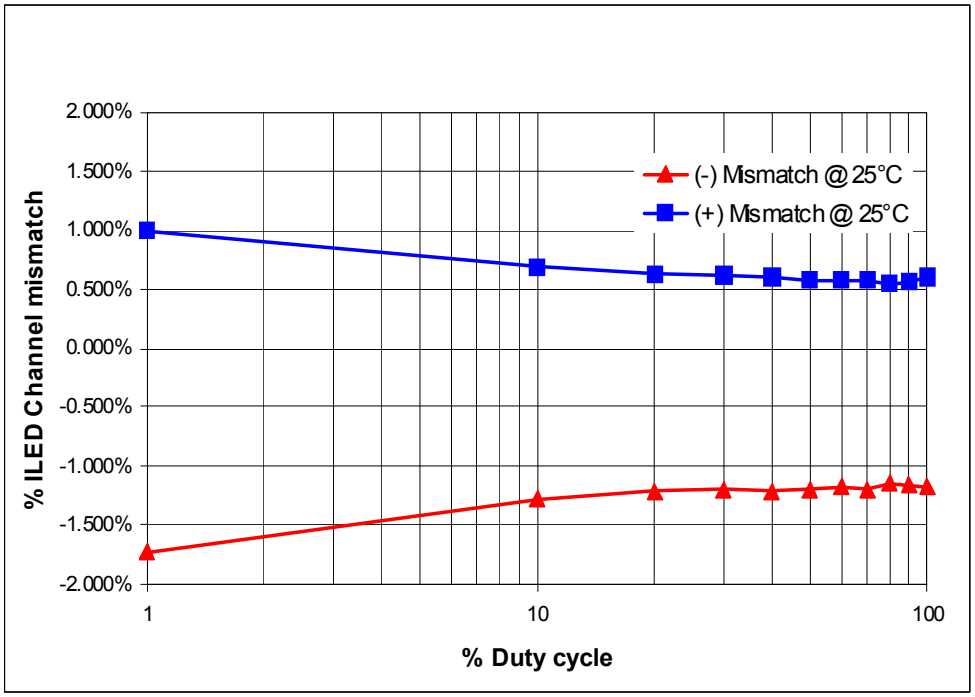


Figure 7. Typical ILED Dimming Linearity (FPWM=25kHz)

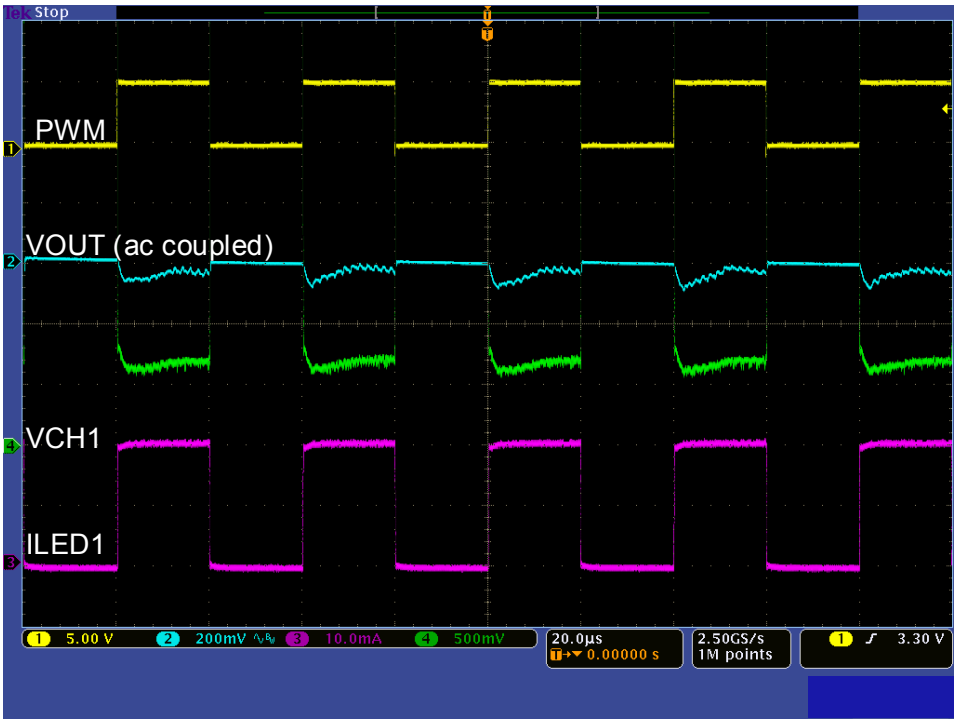


Figure 8. Typical Operating Waveforms (FPWM=25kHz, 50% duty)

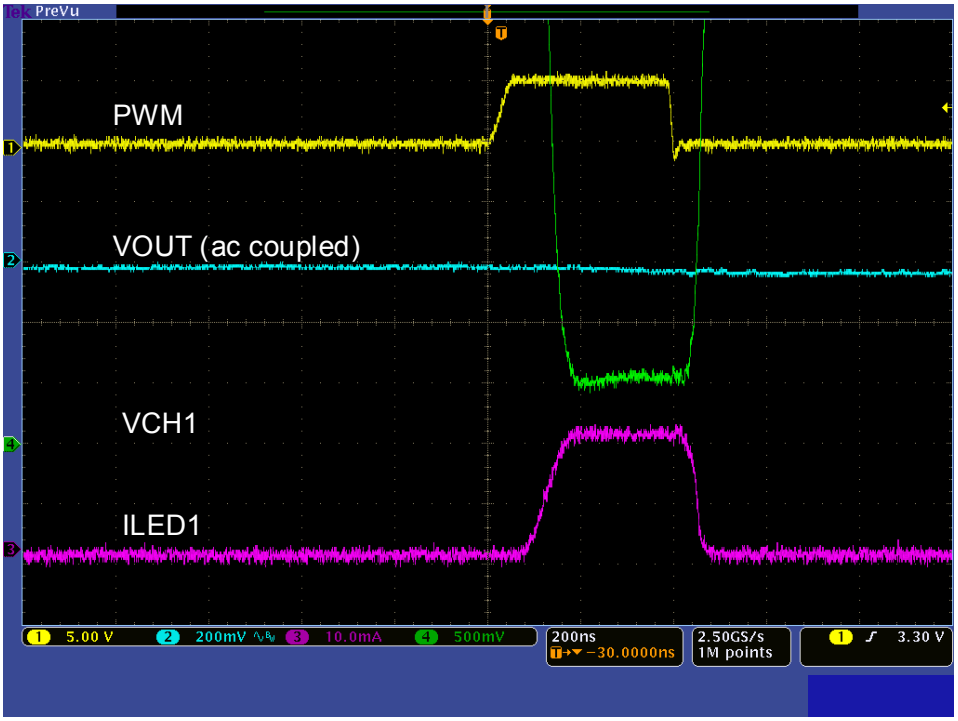


Figure 9. Low Duty Dimming Operation Waveforms (FPWM=25 kHz, 1% duty)

TYPICAL APPLICATIONS

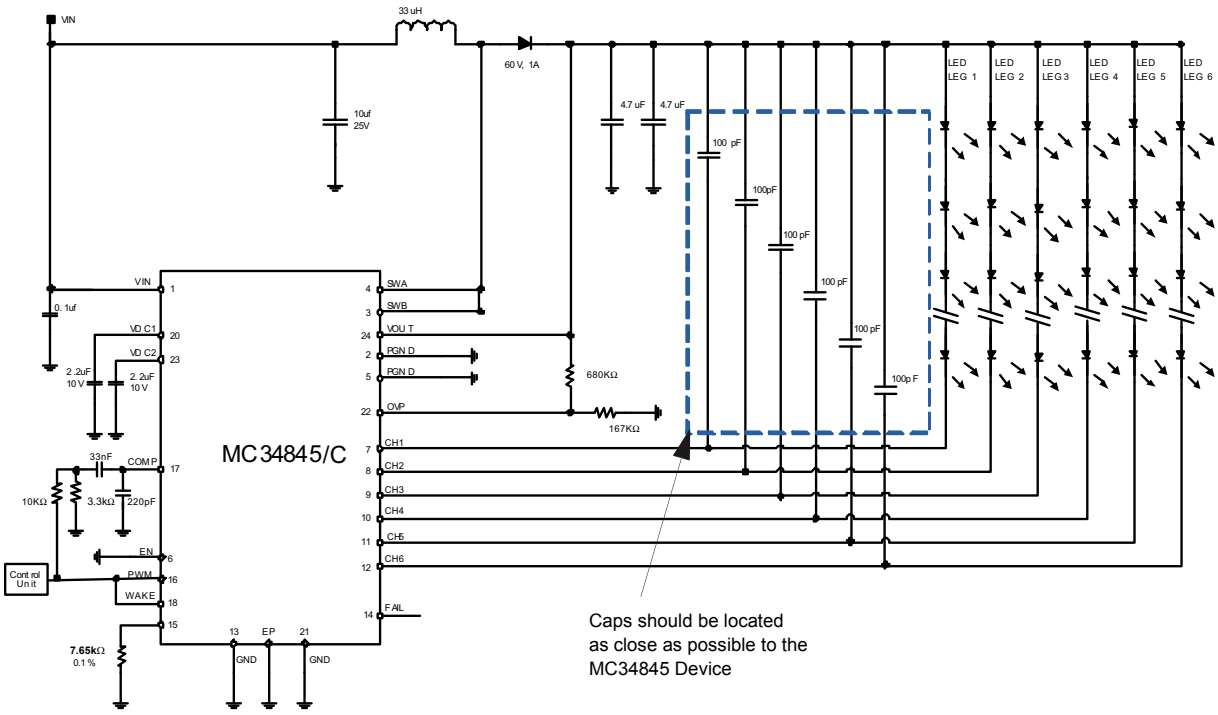


Figure 10. Typical Application Circuit for Single Wire Control, f_S = 600 KHz (V_{IN} = 9.0V, I_{LED}/channel = 20 mA/channel, 10 LEDs/channel, OVP = 35V, V_{PWM} = 3.3V)

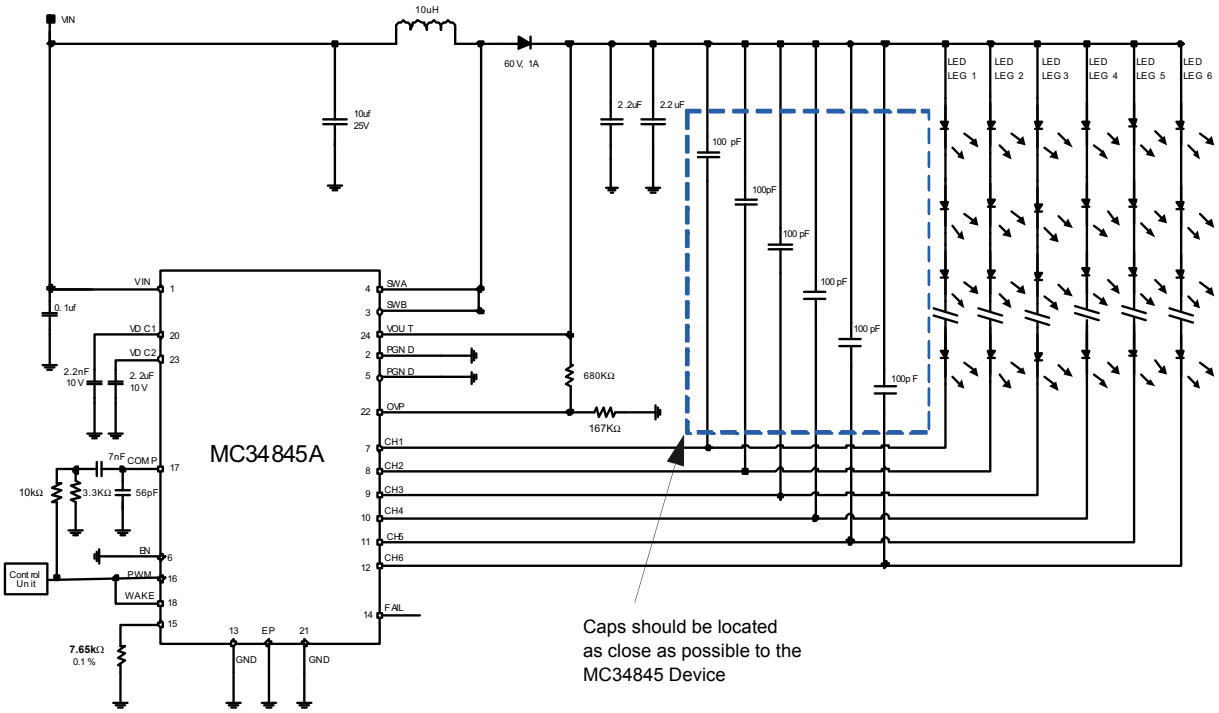


Figure 11. Typical Application Circuit for Single Wire Control, f_S = 1.2 MHz (V_{IN} = 9.0V, I_{LED} = 20 mA/channel, 10 LEDs/channel, OVP = 35V, V_{PWM} = 3.3V)

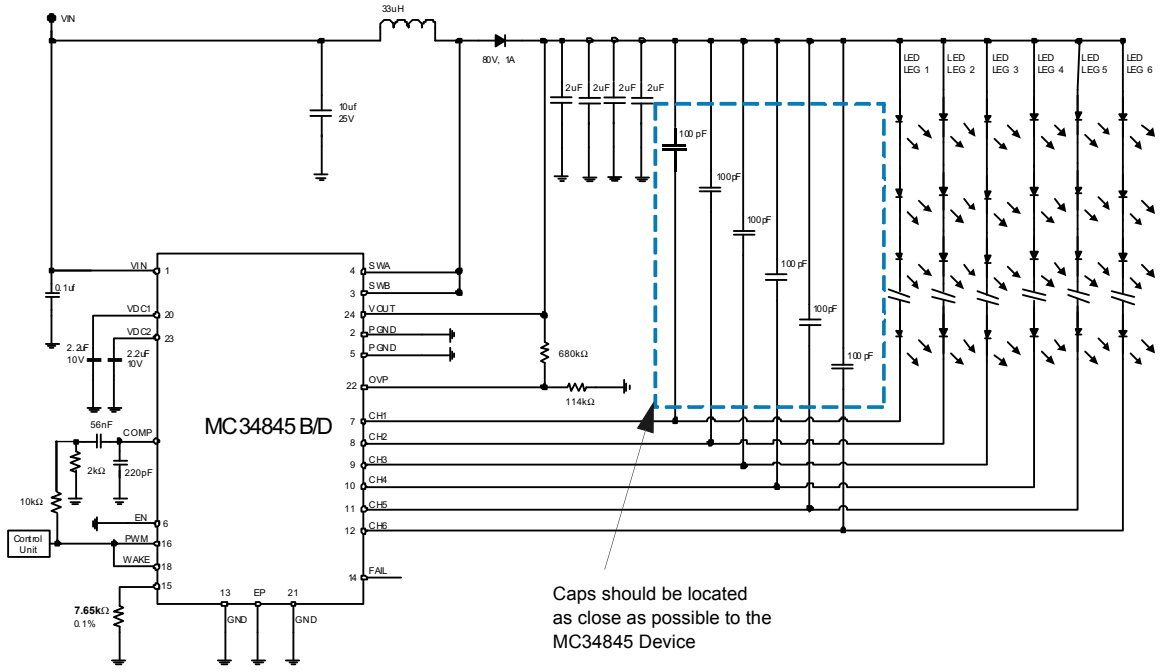


Figure 12. Typical Application Circuit for Single Wire Control, f_S = 300 kHz (V_{IN} = 8.0V, I_{LED} = 20 mA/channel, 14 LEDs/channel, OVP = 49V, V_{PWM} = 3.3V)

COMPONENTS CALCULATION

The following formulas are intended for the calculation of all external components related with the boost converter and network compensation.

In order to calculate the Duty Cycle, the internal losses of the MOSFET and Diode should be taken into consideration:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_{SW}}$$

The average input current depends directly on the output current when the internal switch is off.

$$I_{IN-AVG} = \frac{I_{OUT}}{1 - D}$$

Inductor

For calculating the Inductor, consider the losses of the internal switch and winding resistance of the inductor:

$$L = \frac{(V_{IN} - V_{SW} - (I_{IN-AVG} \times R_{INDUCTOR})) \times D}{I_{IN-AVG} \times r \times F_{SW}}$$

It is important to look for an inductor rated at least for the maximum input current:

$$I_{IN-MAX} = I_{IN-AVG} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times F_{SW} \times V_{OUT}}$$

Input Capacitor

The input capacitor should handle at least the following RMS current.

$$I_{RMS-C_{IN}} = \left(\frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times F_{SW} \times V_{OUT}}\right) \times 0.3$$

Output Capacitor

For the output capacitor selection the transconductance should be taken in consideration.

$$C_{OUT} = \frac{R_{COMP} \times 5 \times G_M \times I_{OUT} \times L}{(1 - D) \times V_{OUT} \times 0.35}$$

The output voltage ripple (ΔV_{OUT}) depends on the ESR of the Output capacitor. For a low output voltage ripple, it is recommended to use ceramic capacitors that have a very low ESR. Since ceramic capacitor are costly, electrolytic or tantalum capacitors can be mixed with ceramic capacitors for a less expensive solution.

$$ESR_{C_{OUT}} = \frac{V_{OUT} \times \Delta V_{OUT} \times F_{SW} \times L}{V_{OUT} \times (1 - D)}$$

The output capacitor should at least handle the following RMS current.

$$I_{RMS-C_{OUT}} = I_{OUT} \times \sqrt{\frac{D}{1 - D}}$$

Network Compensation

Since this Boost converter is current controlled, a Type II compensation is needed.

Note that before calculating the network compensation, all boost converter components need to be known.

For this type of compensation it is recommended to push out the Right Half Plane Zero to higher frequencies where it will not significantly affect the overall loop.

$$f_{RHPZ} = \frac{V_{OUT} \times (1 - D)^2}{I_{OUT} \times 2\pi \times L}$$

The crossover frequency must be set much lower than the location of the Right half plane zero:

$$f_{CROSS} = \frac{f_{RHPZ}}{5}$$

Since our system has a fixed slope compensation, R_{COMP} should be fixed for all configurations, i.e. R_{COMP} = 2 Kohm

C_{COMP1} and C_{COMP2} should be calculated as follows:

$$C_{COMP1} = \frac{2}{\pi \times f_{CROSS} \times R_{COMP}}$$

$$C_{COMP2} = \frac{2G_M}{6.28 \times F_{SW}}$$

The recommended values of these capacitors for an acceptable performance of the system in different operating conditions are Ccomp1=33nF and Ccomp2=220pF.

In order to improve the transient response of the boost a resistor network can be implemented from the PWM pin to ground with a connection to the compensation network. This configuration should inject a 1V signal to the COMP pin and the equivalent Thevenin resistance of the divider should be close to R_{COMP}, (i.e. for 2k COMP resistor, R_{COMP} = 3.3k and R_{SHUNT} = 10k. See Figure 10, Figure 11 and Figure 12 for implementation guidelines.

If a faster transient response is needed, a higher voltage (e.g. 1.3V) should be injected to the COMP pin; so the resistor divider should be modified accordingly but keeping the equivalent Thevenin resistance of the divider close to R_{COMP}.

Variable definition

D = Duty cycle
V_{OUT} = Output voltage
V_D = Diode voltage
V_{IN} = Input voltage
V_{SW} = Internal switch voltage drop.
ΔV_{OUT} = Output voltage ripple
I_{IN-AVG} = Average input current = I_{L-AVG}
I_{OUT} = Output current
I_{IN-MAX} = Maximum input current
r = Current ripple ratio at the inductor = $\Delta I_L / I_{L-AVG}$
$I_{RMS-CIN}$= RMS current for the input capacitor
$I_{RMS-COUT}$= RMS current for output capacitor
L = Inductor.
$R_{INDUCTOR}$= Inductor winding resistor
F_{SW}= Boost switching frequency
C_{OUT} = Output capacitor
R_{COMP} = Compensation resistor
G_M= OTA transconductance
ESR_{COUT}= ESR of the output capacitor
f_{RHPZ}= Right half plane zero frequency
f_{CROSS}= Crossover frequency
C_{COMP1}= Compensation capacitor
C_{COMP2}= Shunt compensation capacitor

Component Suggestions

The Component Suggestions only apply to the conditions shown. Therefore, adjustments are necessary for different application conditions.

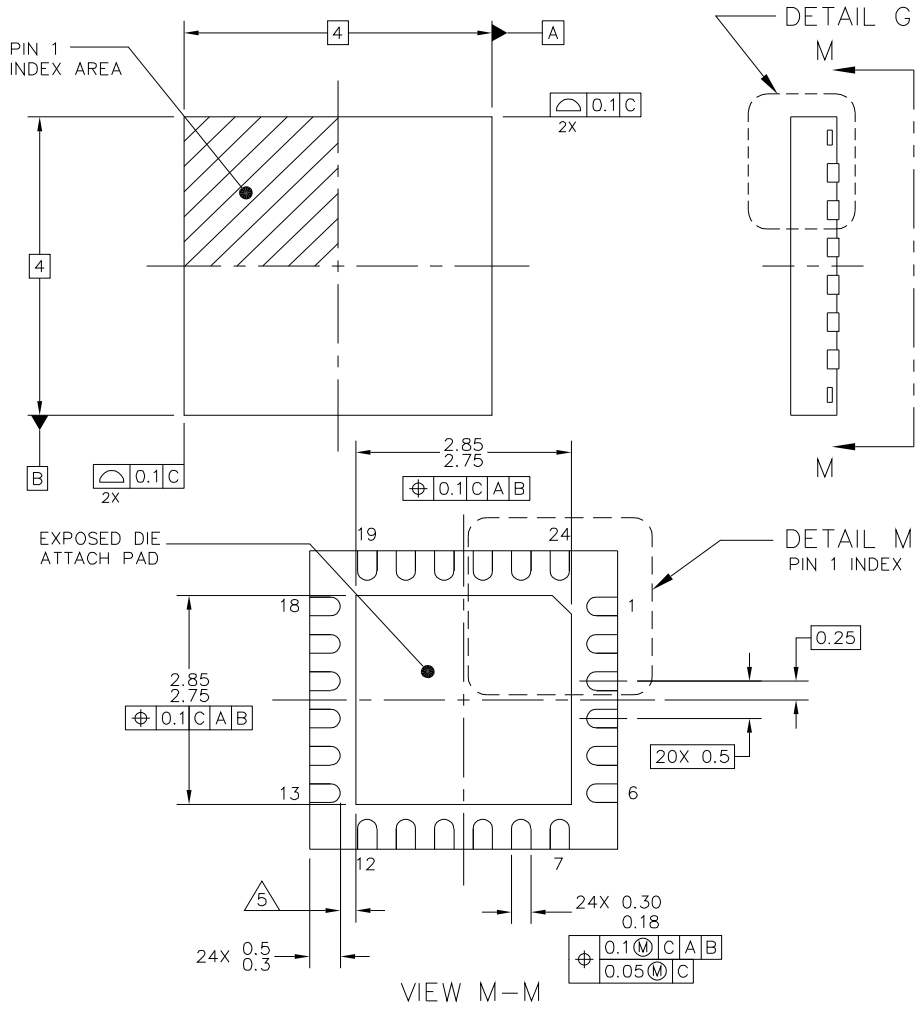
Table 5. Component Suggestion Table

Application Case	Vin(min)	Vin(Max)	Vo(max)	VOVP	fBoost	ILED per channel	Rovp_upper	Rovp_lower	L(min)	L(min) Continuous mode	Cin(min)	Cout(min)	Rcomp at $V_{PWM=3.3V}$	Rshunt at $V_{PWM=3.3V}$	Ccomp1	Ccomp2
1	9V	12V	30V	35V	600kHz	20mA	680kOhm	167kOhm	22uH	33uH	1x10uF; X7R; 25V	2 x 4.7uF; X7R; 50V	3.3kOhm	10kOhm	33nF	220pF
2	6V	12V	43V	48V	300kHz	23mA	680kOhm	114kOhm	22uH	33uH	1x10uF; X7R; 25V	4 x 2.2uF; X7R; 100V	2kOhm	16kOhm	56nF	220pF
									Isat min = 2.6A							

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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	CASE NUMBER: 2084–02	15 JUL 2009
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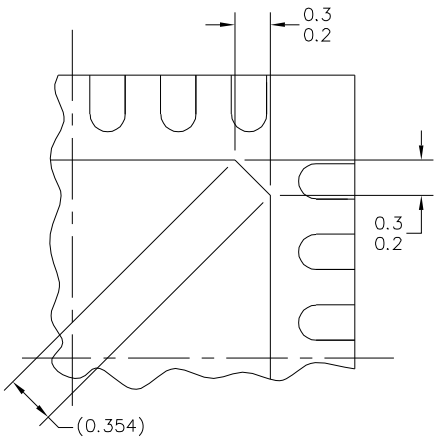
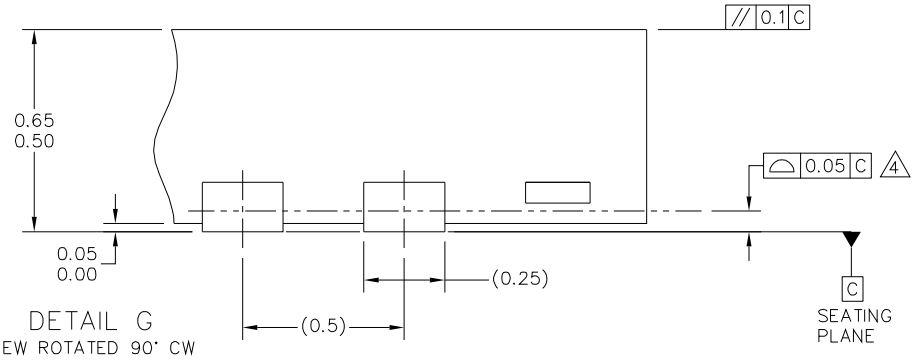
34845



DETAIL M
PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

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REVISION HISTORY

Revision	Date	Description of Changes
6.0	12/2011	• Changed the max rating for the OVP pin from 7.0V to 7.75V in the Absolute Maximum Ratings Table on page 4. • Updated Freescale form and style.
7.0	6/2014	• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph.

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