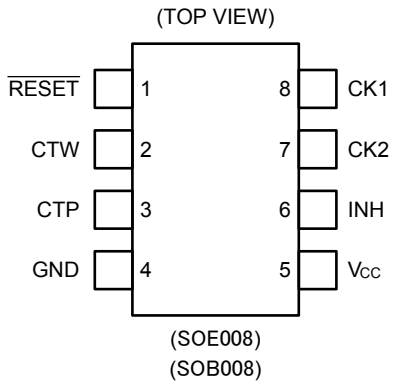
Contents

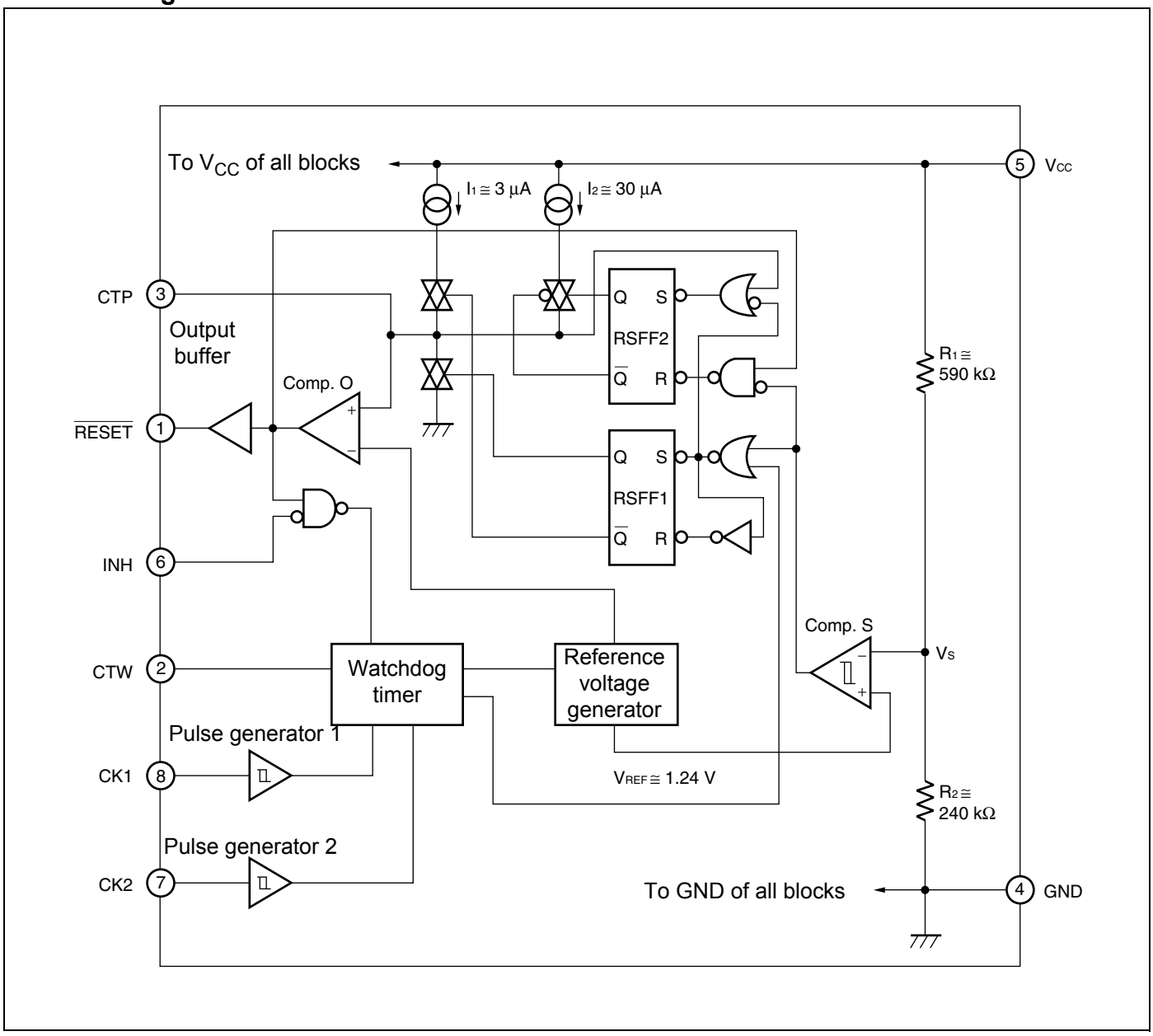
1. Pin Assignment



2. Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$\overline{\text{RESET}}$	Outputs reset	5	V_{CC}	Power supply
2	CTW	Sets monitoring time	6	INH	Inhibits watchdog timer function
3	CTP	Sets power-on reset hold time	7	CK2	Inputs clock 2
4	GND	Ground	8	CK1	Inputs clock 1

3. Block Diagram



4. Block Functions

1. Comp. S

Comp. S is a comparator with hysteresis to compare the reference voltage with a voltage (V_S) that is the result of dividing the power voltage (V_{CC}) by resistors R_1 and R_2. When V_S falls below 1.24 V, a reset signal is output. This function enables the MB3793 to detect an abnormality within 1 µs when the power is cut or falls abruptly.

2. Comp. O

Comp. O is a comparator to control the reset signal ($\overline{RESET}$) output and compares the threshold voltage with the voltage at the CTP terminal for setting the power-on reset hold time. When the voltage at the CTP terminal exceeds the threshold voltage, resetting is canceled.

3. Reset Output Buffer

Since the reset ($\overline{RESET}$) output buffer has CMOS organization, no pull-up resistor is needed.

4. Pulse Generator

The pulse generator generates pulses when the voltage at the CK1 and CK2 input clock terminals changes to High from Low level (positive-edge trigger) and exceeds the threshold voltage; it sends the clock signal to the watchdog timer.

5. Watchdog Timer

The watchdog timer can monitor two clock pulses. Short-circuit the CK1 and CK2 clock terminals to monitor a single clock pulse.

6. Inhibition Terminal

The inhibition (INH) terminal forces the watchdog timer on/off. When this terminal is High level, the watchdog timer is stopped.

7. Flip-flop Circuit

The flip-flop circuit RSFF1 controls charging and discharging of the power-on reset hold time setting capacity (C_{TP}). The flip-flop circuit RSFF2 switches the charging accelerator for charging C_{TP} during resetting on/off. This circuit only functions during resetting and does not function at power-on reset.

5. Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit
			Min	Max	
Power voltage*		V_{CC}	-0.3	+7	V
Input voltage*	CK1	V_{CK1}	-0.3	+7	V
	CK2	V_{CK2}			
	INH	V_{INH}			
Reset output voltage (direct current)	$\overline{RESET}$	I_{OL} I_{OH}	-10	+10	mA
Power dissipation (Ta ≤ +85°C)		P_D	—	200	mW
Storage temperature		Tstg	-55	+125	°C

*: The power voltage is based on the ground voltage (0 V).

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.Do not exceed any of these ratings.

6. Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CC}	1.2	5.0	6.0	V
Reset ($\overline{RESET}$) output current	I_{OL} I_{OH}	-5	—	+5	mA
Power-on reset hold time setting capacity	C_{TP}	0.001	0.1	10	µF
Watchdog timer monitoring time setting capacity	C_{TW}	0.001	0.1	1	µF
Watchdog timer monitoring time	t_{WD}	0.1	—	1500	ms
Operating ambient temperature	Ta	-40	+25	+85	°C

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

7. Electrical Characteristics

7.1 DC Characteristics

(V_{CC} = +5 V, Ta = +25°C)

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Power current	I_{CC1}	Watchdog timer operation*1		—	27	50	µA
	I_{CC2}	Watchdog timer halt*2		—	25	45	
Detection voltage	V_{SL}	V_{CC} falling	Ta = +25°C	4.10	4.20	4.30	V
			Ta = -40 to +85°C	4.05	4.20	4.35	
	V_{SH}	V_{CC} rising	Ta = +25°C	4.20	4.30	4.40	V
			Ta = -40 to +85°C	4.15	4.30	4.45	
Detection voltage hysteresis difference	V_{SHYS}	V_{SH} - V_{SL}		50	100	150	mV
CK input threshold voltage	V_{CIH}	—		(1.4)	1.9	(2.5)	V
	V_{CIL}	—		(0.8)	1.3	(1.8)	V
CK input hysteresis	V_{CHYS}	—		(0.4)	0.6	(0.8)	V
INH input voltage	V_{IIH}	—		3.5	—	V_{CC}	V
	V_{IIL}	—		0	0	0.8	V
Input current (CK1,CK2,INH)	I_{IH}	V_{CK} = V_{CC}		—	0	1.0	µA
	I_{IL}	V_{CK} = 0 V		-1.0	0	—	µA
Reset output voltage	V_{OH}	$I_{\overline{RESET}}$ = -5 mA		4.5	4.75	—	V
	V_{OL}	$I_{\overline{RESET}}$ = +5 mA		—	0.12	0.4	V
Reset-output minimum power voltage	V_{CCL}	$I_{\overline{RESET}}$ = +50 µA		—	0.8	1.2	V

*1: At clock input terminals CK1 and CK2, the pulse input frequency is 1 kHz and the pulse amplitude is 0 V to V_{CC}.

*2: Inhibition input is at High level.

7.2 AC Characteristics

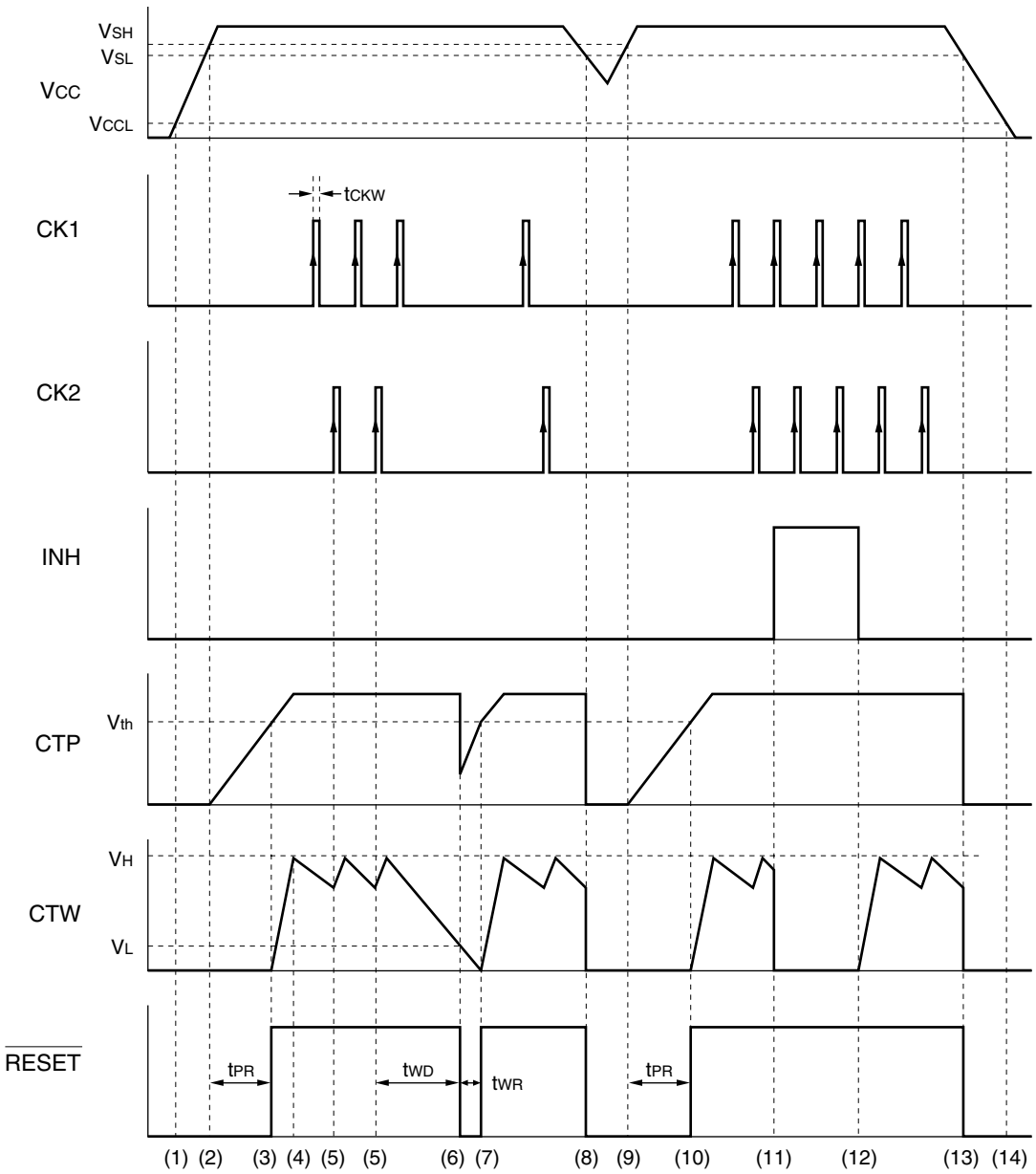
(V_{CC} = +5 V, Ta = +25°C)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Power-on reset hold time		t_{PR}	C_{TP} = 0.1 µF	80	130	180	ms
Watchdog timer monitoring time		t_{WD}	C_{TW} = 0.01 µF C_{TP} = 0.1 µF	7.5	15	22.5	ms
Watchdog timer reset time		t_{WR}	C_{TP} = 0.1µF	5	10	15	ms
CK input pulse duration		t_{CKW}	—	500	—	—	ns
CK input pulse cycle		t_{CKT}	—	20	—	—	µs
Reset ($\overline{\text{RESET}}$) output transition time	Rising	tr*	C_L = 50 pF	—	—	500	ns
	Falling	tf*	C_L = 50 pF	—	—	500	ns

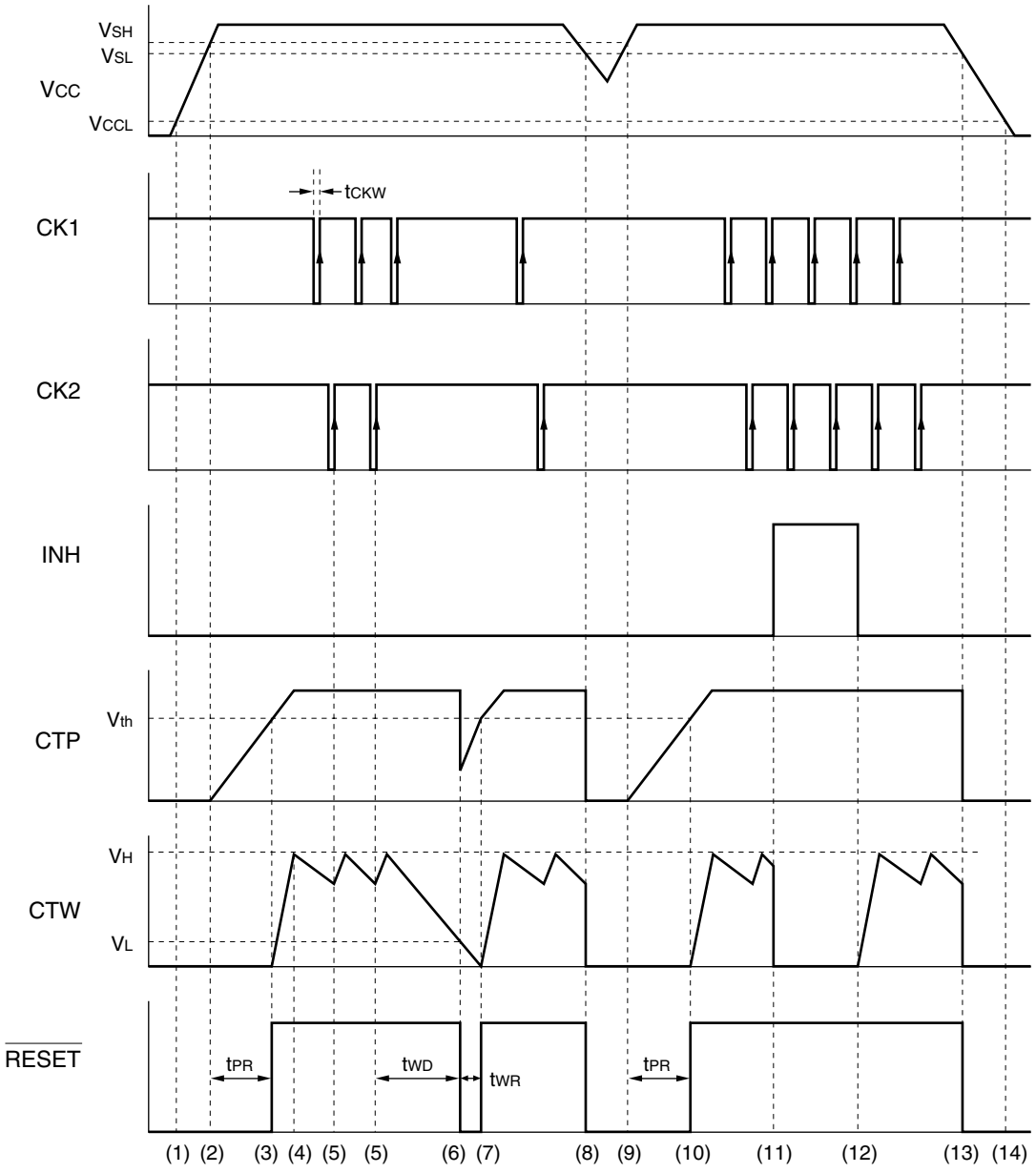
*: The voltage range is 10% to 90% at testing the reset output transition time.

8. Timing Diagram

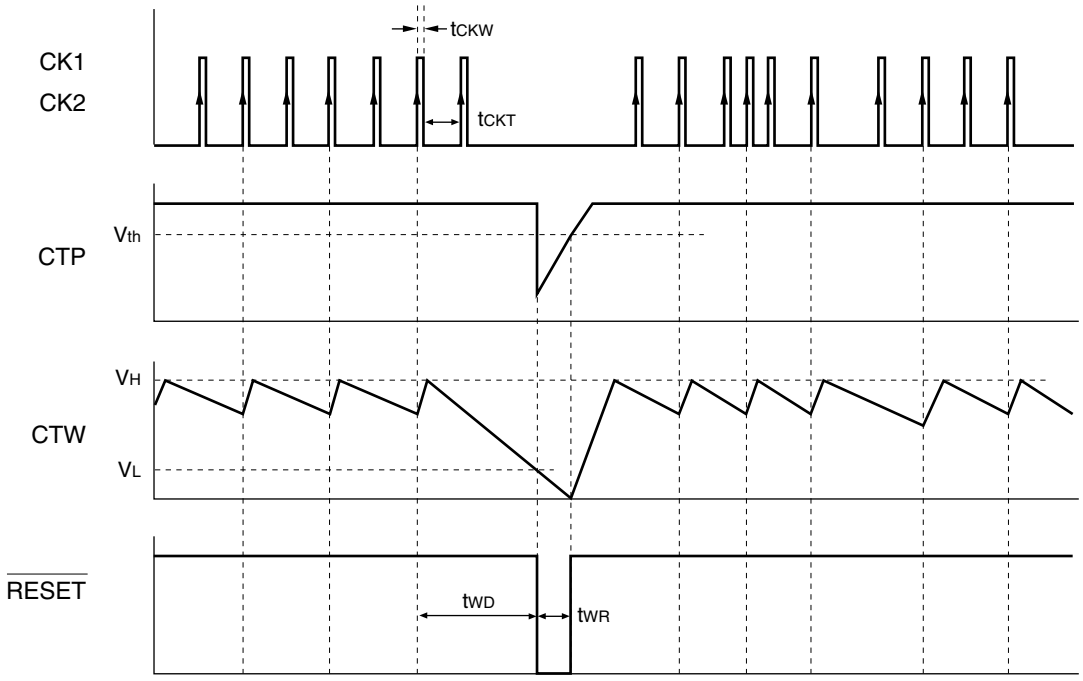
8.1 Basic Operation (Positive Clock Pulse)



8.2 Basic Operation (Negative Clock Pulse)

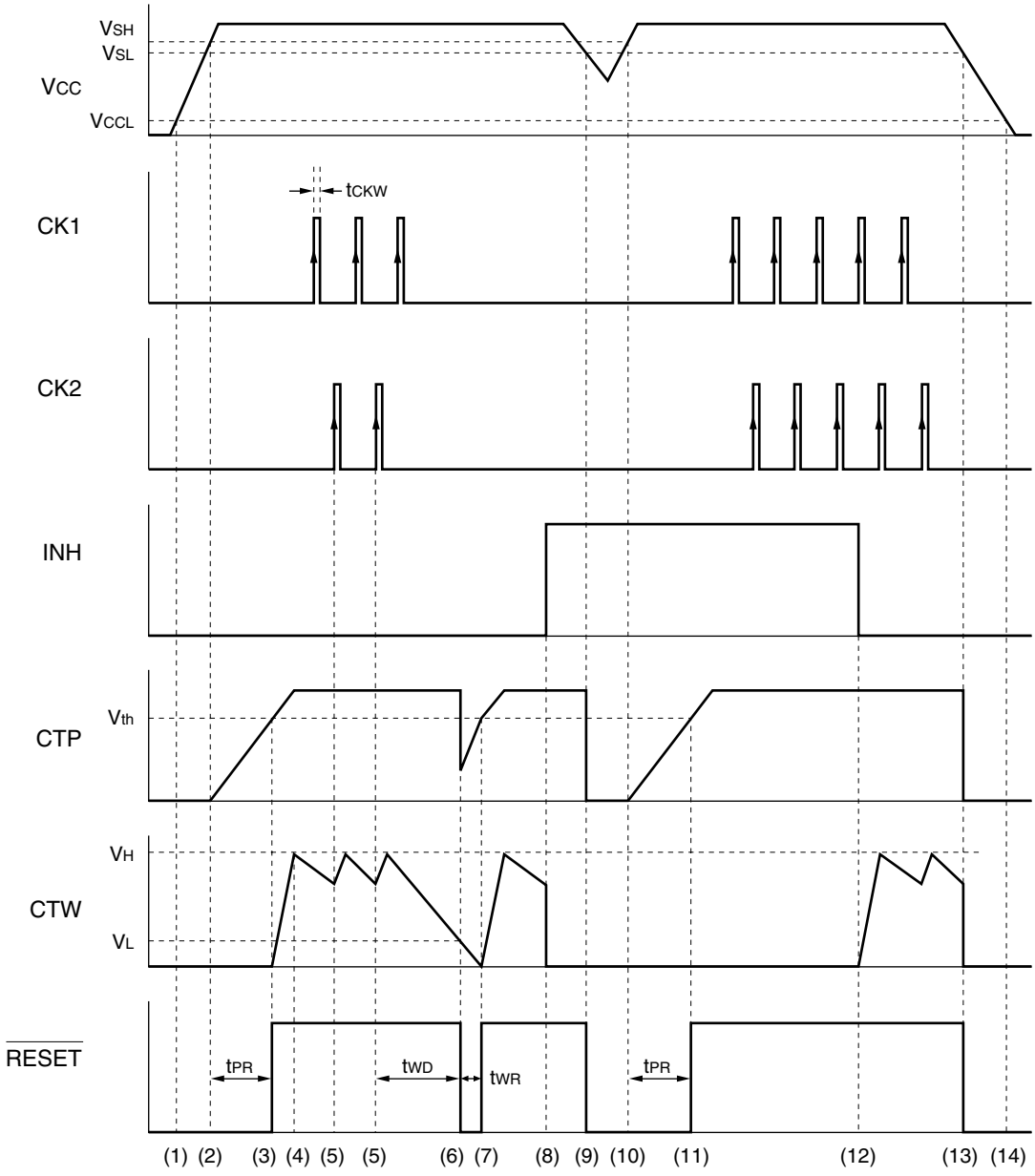


8.3 Single-clock Input Monitoring (Positive Clock Pulse)

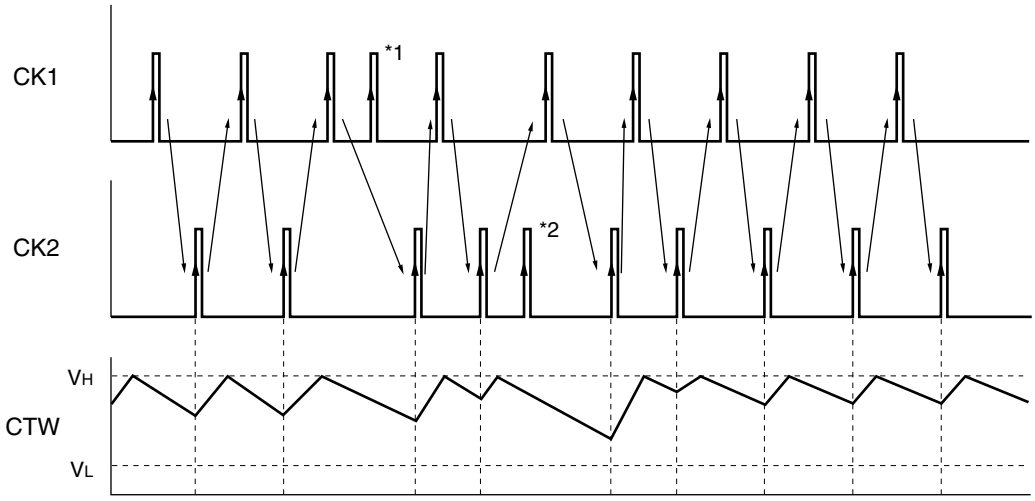


Note: The MB3793 can monitor only one clock.
The MB3793 checks the clock signal at every other input pulse. Therefore, set watchdog timer monitor time tWD to the time that allows the MB3793 to monitor the period twice as long as the input clock pulse.

8.4 Inhibition Operation (Positive Clock Pulse)

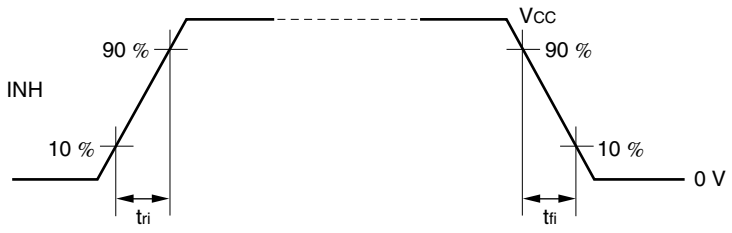


8.5 Clock Pulse Input (Positive Clock Pulse)



Note: The MB3793 watchdog timer monitors Clock 1 (CK1) and Clock 2 (CK2) pulses alternately. When a CK2 pulse is detected after detecting a CK1 pulse, the monitoring time setting capacity (C_{TW}) switches to charging from discharging.
When two consecutive pulses occur on one side of this alternation before switching, the second pulse is ignored. In the above figure, pulses *1 and *2 are ignored.

8.6 Inhibition Input Rising and Falling Time



9. Operation Sequence

The operation sequence is explained by using “8. Timing Diagram 8.1. Basic Operation (Positive Clock Pulse)”.
The following item numbers correspond to the numbers in “8.Timing Diagram 8.1. Basic Operation (Positive Clock Pulse)”.

1. When the power voltage (V_{CC}) reaches about 0.8 V (V_{CCL}), a reset signal is output.
2. When V_{CC} exceeds the rising-edge detection voltage (V_{SH}), charging of power-on reset hold time setting capacitance (C_{TP}) is started. V_{SH} is about 4.3 V.
3. When the voltage at the CTP terminal setting the power-on reset hold time exceeds the threshold voltage (V_{th}), resetting is canceled and the voltage at the $\overline{\text{RESET}}$ terminal changes to High level to start charging of the watchdog timer monitoring time setting capacitance (C_{TW}). Vth is about 3.6 V.

   The power-on reset hold time (t_{PR}) can be calculated by the following equation.

   t_{PR} (ms) ≈ A × C_{TP} (µF)

   Where, A is about 1300.
4. When the voltage at the CTW terminal setting the monitoring time reaches High level (V_H), C_{TW} switches to discharging from charging. V_H is about 1.24 V (reference value).
5. When clock pulses are input to the CK2 terminal during C_{TW} discharging after clock pulses are input to the CK1 terminal—positive-edge trigger, C_{TW} switches to charging.
6. If clock pulse input does not occur at either the CK1 or CK2 clock terminals during the watchdog timer monitoring time (t_{WD}), the CTW voltage falls below Low level (V_L), a reset signal is output, and the voltage at the $\overline{\text{RESET}}$ terminal changes to Low level. V_L is about 0.24 V.

   t_{WD} can be calculated from the following equation.

   t_{WD} (ms) ≈ B × C_{TW} (µF) + C × C_{TP} (µF)

   Where, B is about 1500. C is about 3; it is much smaller than B.
   Hence, when C_{TP} / C_{TW} ≤ 10, the calculation can be simplified as follows:

   t_{WD} (ms) ≈ B × C_{TW} (µF)
7. When the voltage of the CTP terminal exceeds V_{th} again as a result of recharging C_{TP}, resetting is canceled and the watchdog timer restarts monitoring.

   The watchdog timer reset time (t_{WR}) can be calculated by the following equation.

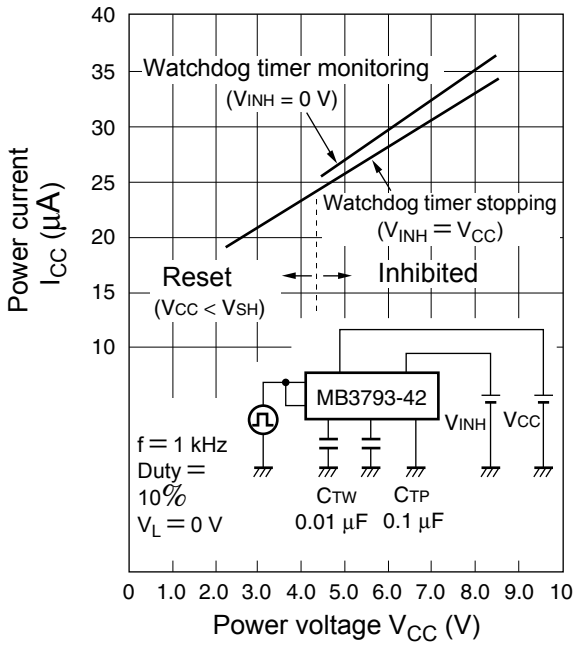
   t_{WR} (ms) ≈ D × C_{TP} (µF)

   Where, D is about 100.
8. When V_{CC} falls below the rising-edge detection voltage (V_{SL}), the voltage of the CTP terminal falls and a reset signal is output, and the voltage at the $\overline{\text{RESET}}$ terminal changes to Low level. V_{SL} is about 4.2 V.
9. When V_{CC} exceeds V_{SH}, C_{TP} begins charging.
10. When the voltage of the CTP terminal exceeds V_{th}, resetting is canceled and the watchdog timer restarts.
11. When an inhibition signal is input (INH terminal is High level), the watchdog timer is halted forcibly.
    In this case, V_{CC} monitoring is continued without the watchdog timer.
    The watchdog timer does not function unless this inhibition input is canceled.
12. When the inhibition input is canceled (INH terminal is Low level), the watchdog timer restarts.
13. When the V_{CC} voltage falls below V_{SL} after power-off, a reset signal is output.
14. When the power voltage (V_{CC}) falls below about 0.8 V (V_{CCL}) , a reset signal is released.

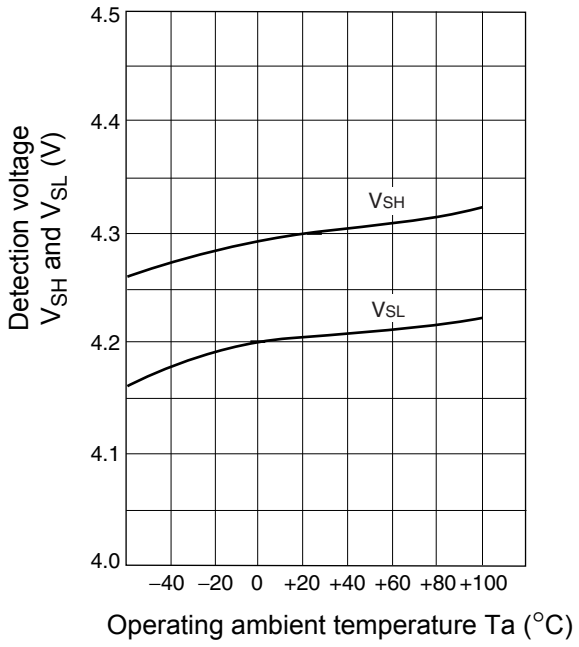
    Similar operation is also performed for negative clock-pulse input (“8. Timing Diagram 8.2. Basic operation (Negative clock pulse)”).
    Short-circuit the clock terminals CK1 and CK2 to monitor a single clock. The basic operation is the same but the clock pulses are monitored at every other pulse (8. Timing Diagram 8.3. Single-clock input monitoring).

10. Typical Characteristics

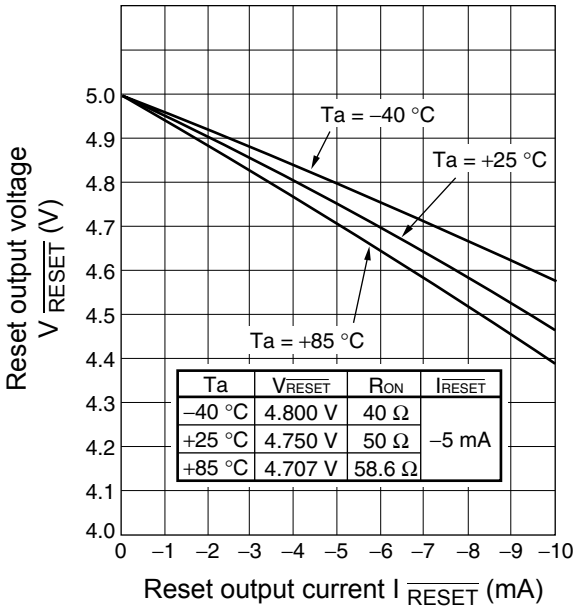
Power Current - Power Voltage



Detection Voltage - Operating ambient Temperature

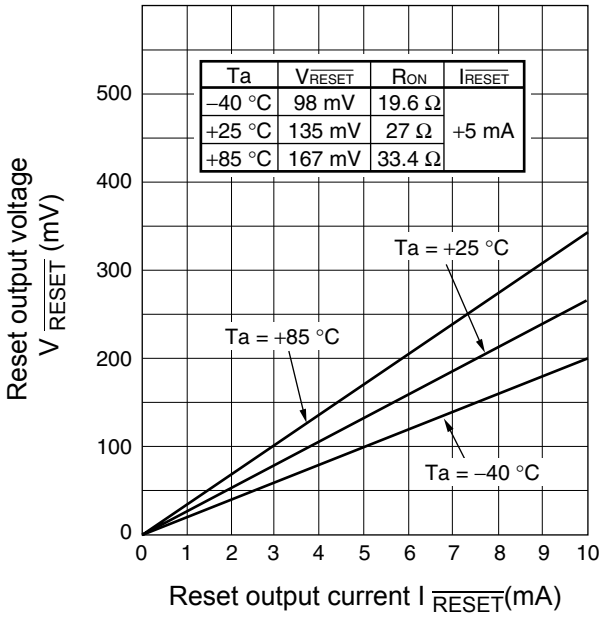


Reset Output Voltage - Reset Output Current (P-MOS side)



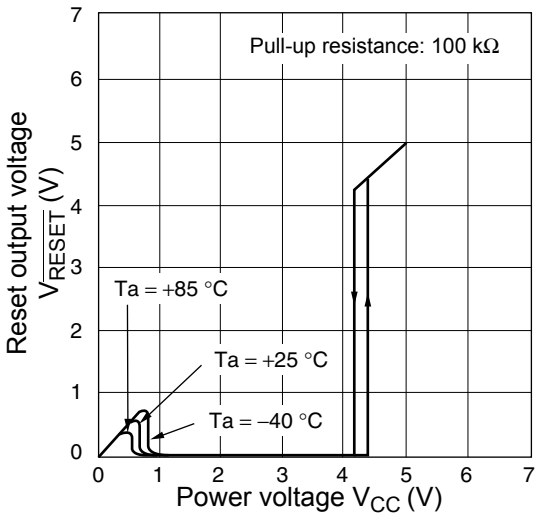
Ta	VRESET	RON	IRESET
−40 °C	4.800 V	40 Ω	−5 mA
+25 °C	4.750 V	50 Ω	
+85 °C	4.707 V	58.6 Ω	

Reset Output Voltage - Reset Output Current (N-MOS side)

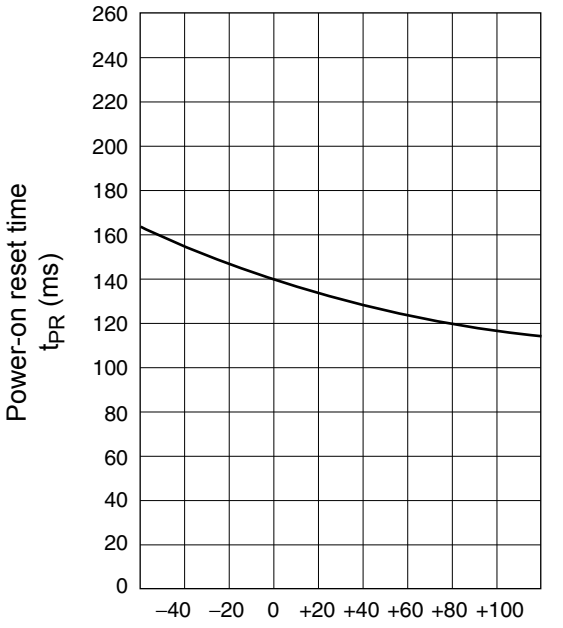


Ta	VRESET	RON	IRESET
−40 °C	98 mV	19.6 Ω	+5 mA
+25 °C	135 mV	27 Ω	
+85 °C	167 mV	33.4 Ω	

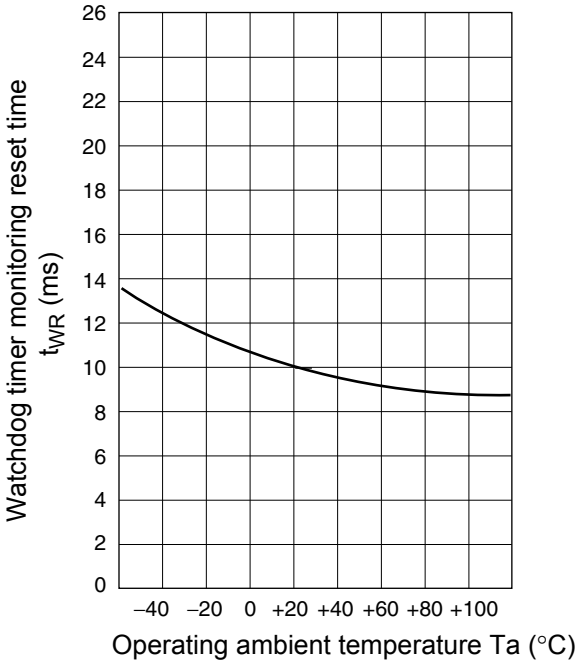
Reset Output Voltage - Power Voltage



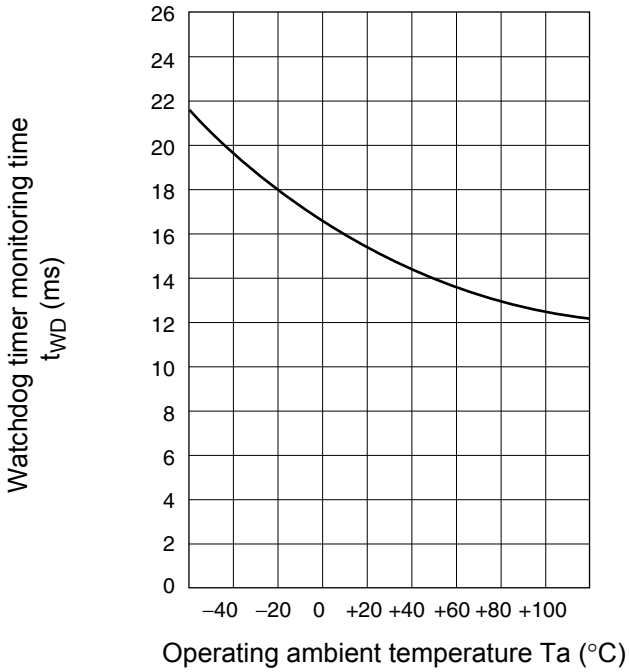
Reset-on Reset Time - Operating ambient temperature (when V_{CC} rising)



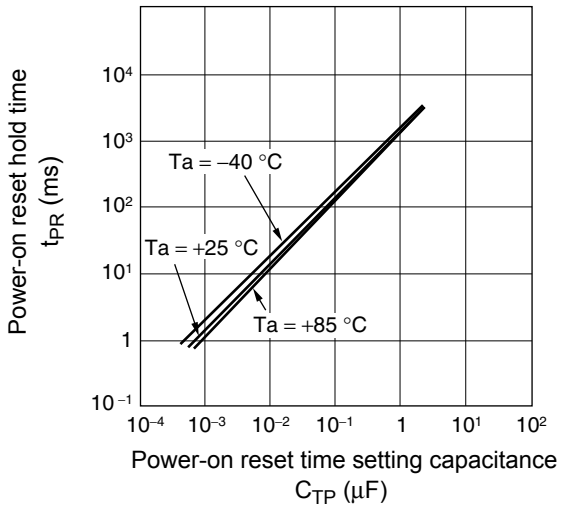
Watchdog Timer Monitoring Reset Time - Operating ambient temperature (when monitoring)



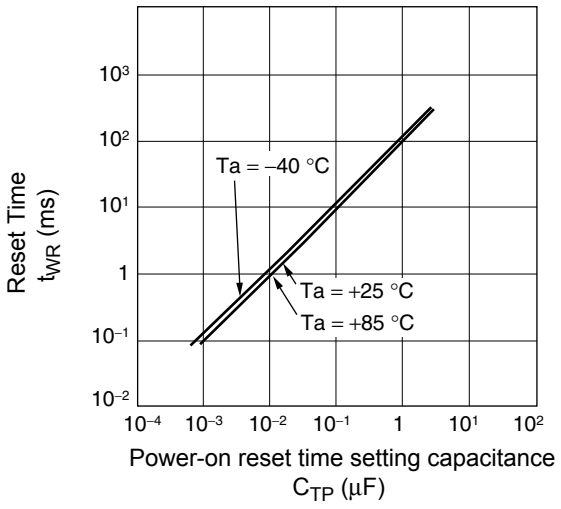
Watchdog Timer Monitoring Time - Operating ambient temperature



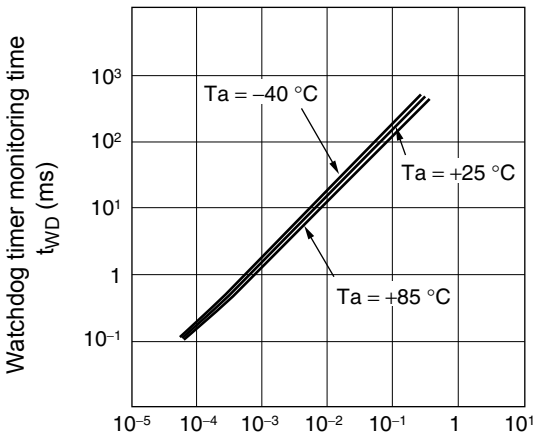
Power-on Reset Hold Time - C_{TP} Capacitance



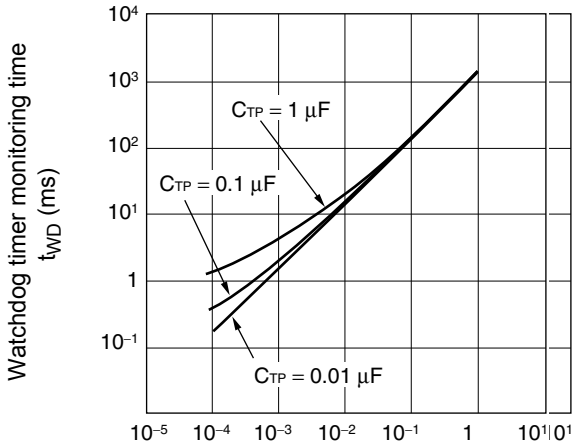
Reset Time - C_{TP} Capacitance



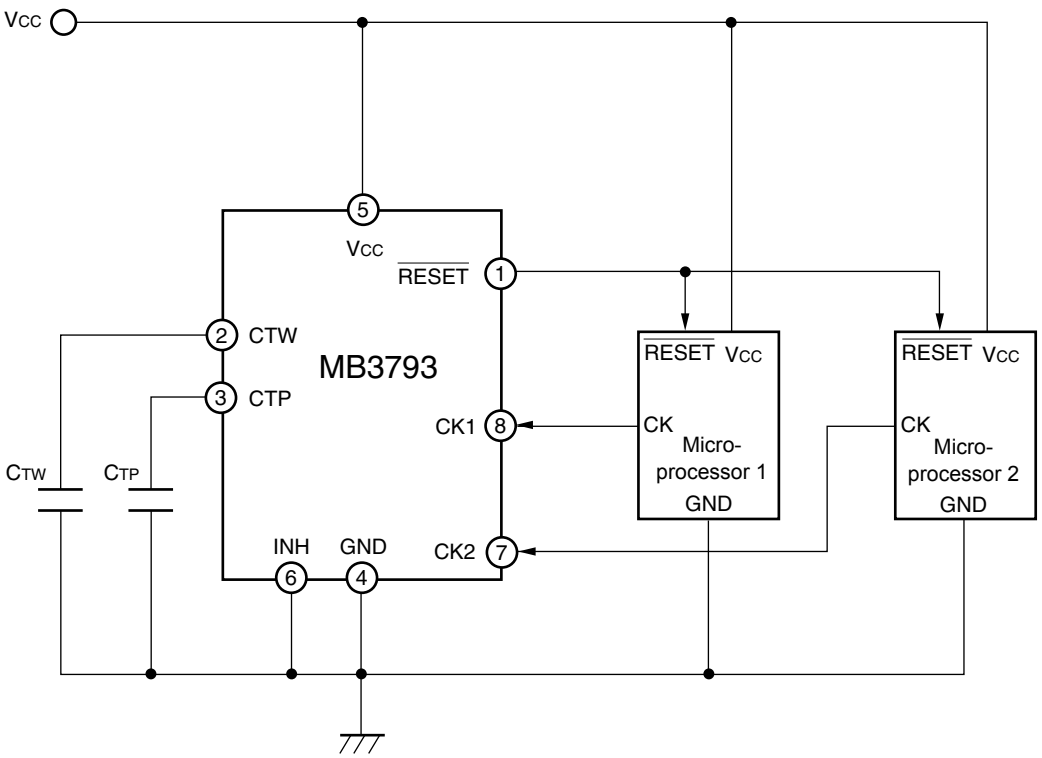
Watchdog Timer Monitoring Time - C_{TW} Capacitance (under Ta condition)



Watchdog Timer Monitoring Time - C_{TW} Capacitance



11. Standard Connection



Equation of time-setting capacitances (C_{TP} and C_{TW}) and set time

t_{PR} (ms) ≈ A × C_{TP} (µF)

t_{WD} (ms) ≈ B × C_{TW} (µF) + C × C_{TP} (µF)

However, when $C_{TP}/C_{TW} \leq 10$,

t_{WD} (ms) ≈ B × C_{TW} (µF)

t_{WR} (ms) ≈ D × C_{TP} (µF)

Value of A, B, C and D

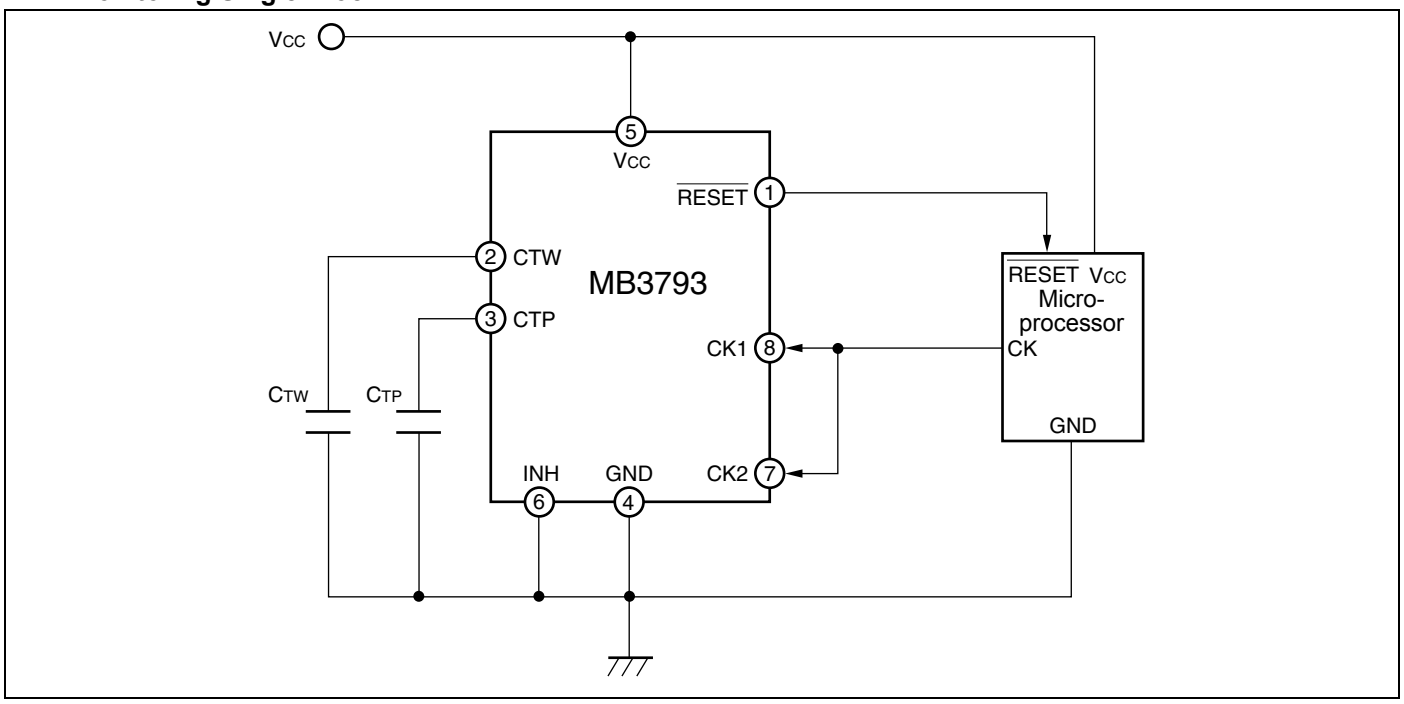
A	B	C	D	Remark
1300	1500	3	100	

(Example) When C_{TP} = 0.1 µF and C_{TW} = 0.01 µF,

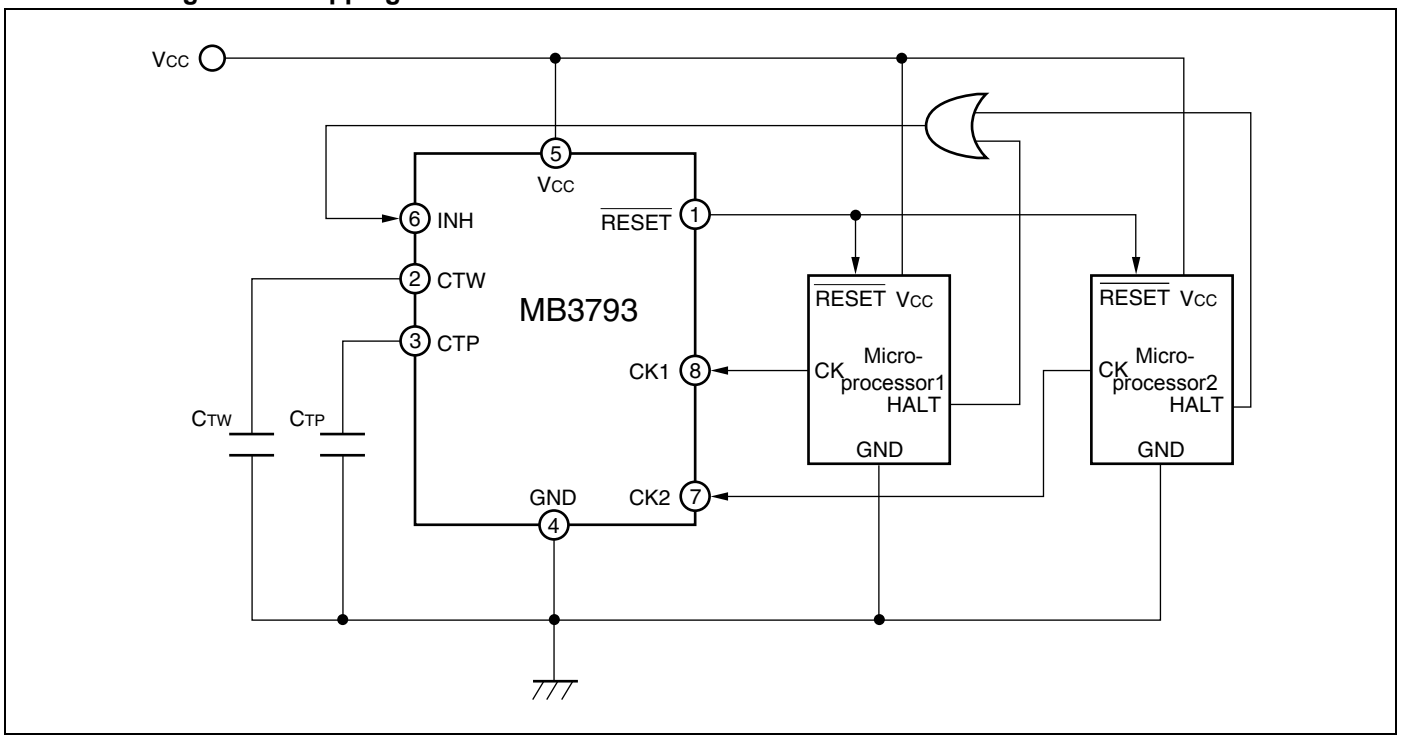
t_{PR} ≈ 130 [ms]
t_{WD} ≈ 15 [ms]
t_{WR} ≈ 10 [ms]

12. Application Example

12.1 Monitoring Single Clock



12.2 Watchdog Timer Stopping



13. Notes on Use

- Take account of common impedance when designing the earth line on a printed wiring board.
- Take measures against static electricity.
  - For semiconductors, use antistatic or conductive containers.
  - When storing or carrying a printed circuit board after chip mounting, put it in a conductive bag or container.
  - The work table, tools and measuring instruments must be grounded.
  - The worker must put on a grounding device containing 250 kΩ to 1 MΩ resistors in series.
- Do not apply a negative voltage
  - Applying a negative voltage of −0.3 V or less to an LSI may generate a parasitic transistor, resulting in malfunction.

14. Ordering Information

Part Number	Package	Remarks
MB3793-42PF-❑❑❑E1	8-pin plastic SOP (SOE008)	–
MB3793-42PNF-❑❑❑E1	8-pin plastic SOP (SOB008)	–

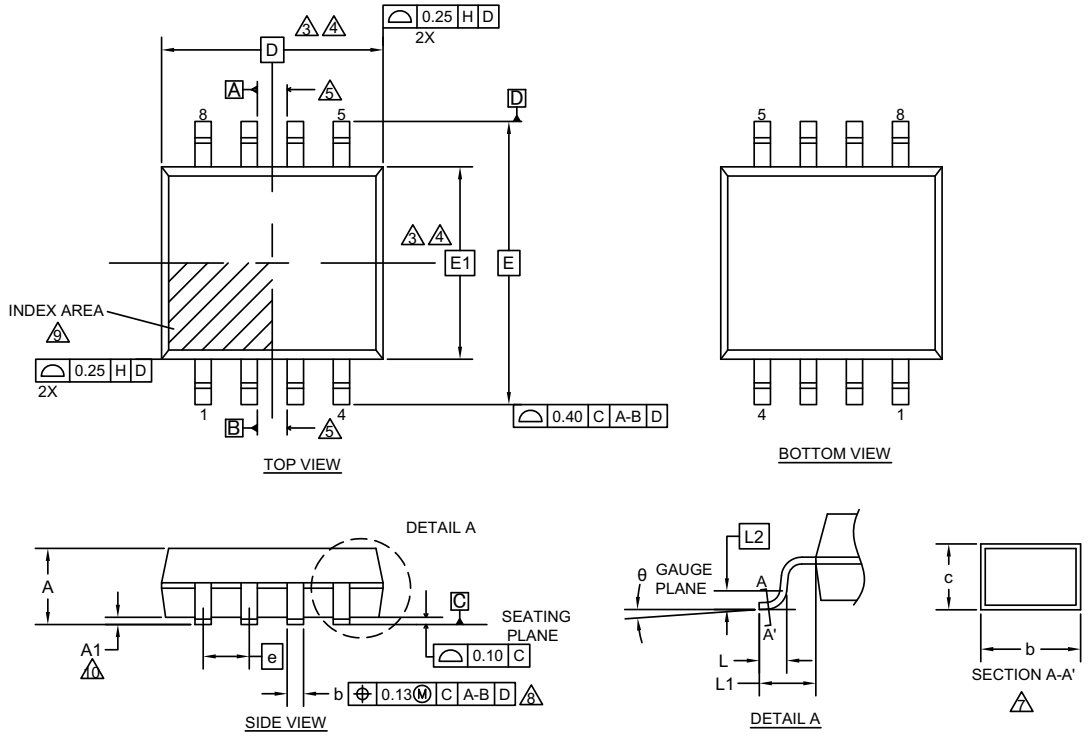
15. RoHS Compliance Information

The LSI products of Cypress with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

16. Package Dimensions

Package Code: SOE008



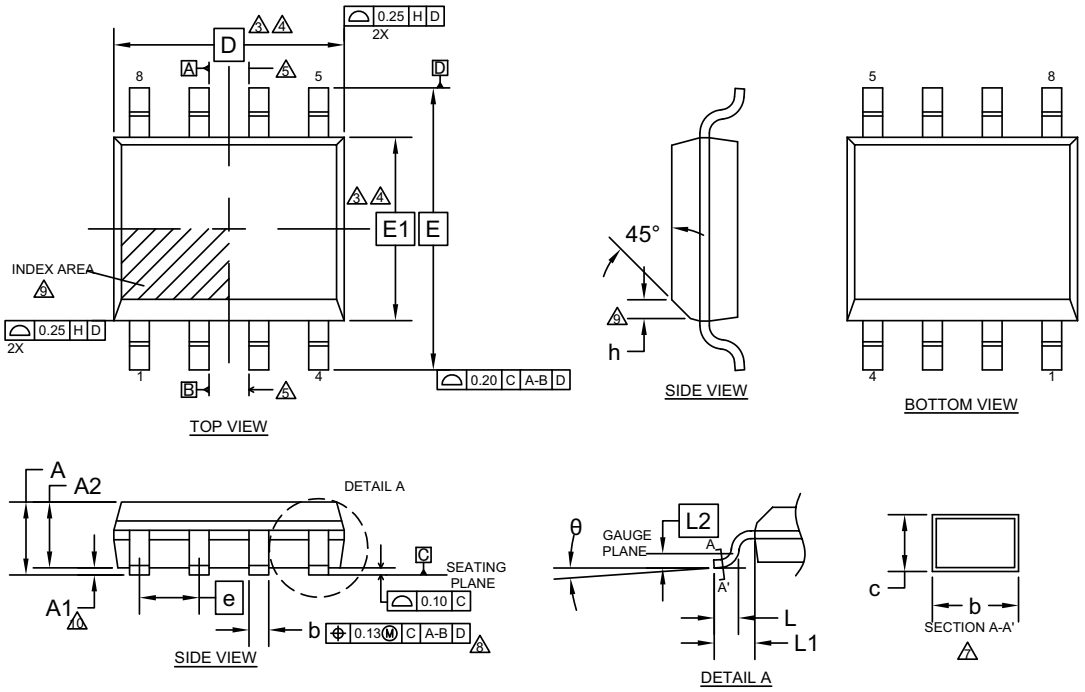
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	2.25
A1	0.05	——	0.20
D	6.35 BSC		
E	7.80 BSC		
E1	5.30 BSC		
θ	0°	——	8°
c	0.13	——	0.20
b	0.39	0.47	0.55
L	0.45	0.60	0.75
L 1	1.25 REF		
L 2	0.25 BSC		
e	1.27 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15857 Rev. **

Package Code: SOB008



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.75
A1	0.05	——	0.25
A2	1.30	1.40	1.50
D	5.05 BSC.		
E	6.00 BSC.		
E1	3.90 BSC		
θ	0°	——	8°
c	0.15	——	0.25
b	0.36	0.44	0.52
L	0.45	0.60	0.75
L 1	1.05 REF		
L 2	0.25 BSC		
e	1.27 BSC.		
h	0.40 BSC.		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15856 Rev. **

17. Major Changes

Spansion Publication Number: MB3793-42_DS04-27402

Page	Section	Change Results
Revision 6.0		
-	-	Company name and layout design change
1	Description	Deleted “There is also a mask option that can detect voltages of 4.9 V to 2.4 V in 0.1-V steps.”
Revision 6.1		
22	MB3793-42PF-❑❑❑1, MB3793-42PNF-❑❑❑E1 Recommended Conditions of Moisture Sensitivity Level	Changed the subtitle text of Figure

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB3793-42 Power-Voltage Monitoring IC with Watchdog Timer
Document Number: 002-08515

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	TAOA	02/27/2015	Migrated to Cypress and assigned document number 002-08515. No change to document contents or format.
*A	5199108	TAOA	04/04/2016	Updated to Cypress format.
*B	5610247	HIXT	01/31/2017	Updated Pin Assignment: Change the package name from FPT-8P-M01 to SOE008 Change the package name from FPT-8P-M02 to SOB008 Updated Ordering Information: Change the package name from FPT-8P-M01 to SOE008 Change the package name from FPT-8P-M02 to SOB008 Deleted the part numbers, MB3793-42PF- ❑❑❑ and MB3793-42PNF- ❑❑❑ Deleted the words in the Remarks, “Lead Free version” Updated Package Dimensions: Updated to Cypress format Deleted “Marking Format (Lead Free version)” Deleted “Labeling Sample (Lead free version)” Deleted “MB3793-42PF- ❑❑❑ E1, MB3793-42PNF- ❑❑❑ E1 Recommended Conditions of Moisture Sensitivity Level”
*C	5788795	MASG	06/28/2017	Adapted Cypress new logo.

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