

High-Voltage, Precision, Low-Power Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})	-0.3V to +40V
All Other Pins (Note 1)	($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)
OUT Short-Circuit Current Duration	
8-Pin μ MAX ($V_{CC} - V_{EE} \leq 20V$)	3s
8-Pin μ MAX ($V_{CC} - V_{EE} > 20V$)	Momentary
6-Pin TDFN ($V_{CC} - V_{EE} \leq 20V$)	60s
6-Pin TDFN ($V_{CC} - V_{EE} > 20V$)	2s
8-Pin SO ($V_{CC} - V_{EE} \leq 20V$)	60s
8-Pin SO ($V_{CC} - V_{EE} > 20V$)	2s
8-Pin TDFN ($V_{CC} - V_{EE} \leq 20V$)	60s
8-Pin TDFN ($V_{CC} - V_{EE} > 20V$)	2s

Continuous Input Current (Any Pins)	$\pm 20mA$
Thermal Limits (Note 2)	
Multiple Layer PCB	
Continuous Power Dissipation ($T_A = +70^\circ C$)	
8-Pin μ MAX (derate 4.8mW/ $^\circ C$ above $+70^\circ C$)	387.8mW
6-Pin TDFN-EP (derate 23.8mW/ $^\circ C$ above $+70^\circ C$)	1904.8mW
8-Pin SO (derate 7.6mW/ $^\circ C$ above $+70^\circ C$)	606.1W
8-Pin TDFN-EP (derate 24.4mW/ $^\circ C$ above $+70^\circ C$)	1951.2mW
Operating Temperature Range	$-40^\circ C$ to $+125^\circ C$
Junction Temperature	$+150^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$
Soldering Temperature (reflow)	$+260^\circ C$

Note 1: Operation is limited by thermal limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

8 μ MAX		8 SO	
Junction-to-Ambient Thermal Resistance (θ_{JA})	206.3 $^\circ C/W$	Junction-to-Ambient Thermal Resistance (θ_{JA})	132 $^\circ C/W$
Junction-to-Ambient Case Resistance (θ_{JC})	42 $^\circ C/W$	Junction-to-Ambient Case Resistance (θ_{JC})	38 $^\circ C/W$
6 TDFN-EP		8 TDFN-EP	
Junction-to-Ambient Thermal Resistance (θ_{JA})	42 $^\circ C/W$	Junction-to-Ambient Thermal Resistance (θ_{JA})	41 $^\circ C/W$
Junction-to-Ambient Case Resistance (θ_{JC})	9 $^\circ C/W$	Junction-to-Ambient Case Resistance (θ_{JC})	8 $^\circ C/W$

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{CC} = 15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ to GND, $V_{GND} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Operating Supply Voltage Range	V_{SUPPLY}	Guaranteed by PSRR test	± 3		± 19	V
Quiescent Supply Current per Amplifier	I_{CC}			550	950	μA
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 19V$	105	130		dB
Input Offset Voltage	V_{OS}	$T_A = +25^\circ C$		20	100	μV
		$T_A = -40^\circ C$ to $+125^\circ C$			240	
Input Offset Voltage Drift	TCV_{OS}			0.4		$\mu V/^\circ C$
Input Bias Current	I_{BIAS}	$V_{EE} + 0.3V \leq V_{CM} \leq V_{CC} - 1.8V$		4	20	nA
		$V_{EE} \leq V_{CM} \leq V_{CC} - 1.8V$			90	
Input Offset Current	I_{OS}	$V_{EE} \leq V_{CM} \leq V_{CC} - 1.8V$		1	10	nA
Input Voltage Range	V_{IN+} , V_{IN-}	Guaranteed by CMRR test, $T_A = -40^\circ C$ to $+125^\circ C$	V_{EE}		$V_{CC} - 1.8$	V
Common-Mode Rejection Ratio	CMRR	$V_{EE} + 0.3V \leq V_{CM} \leq V_{CC} - 1.8V$	105	125		dB
		$V_{EE} \leq V_{CM} \leq V_{CC} - 1.8V$	105			

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MAX9943/MAX9944

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ to GND, $V_{GND} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

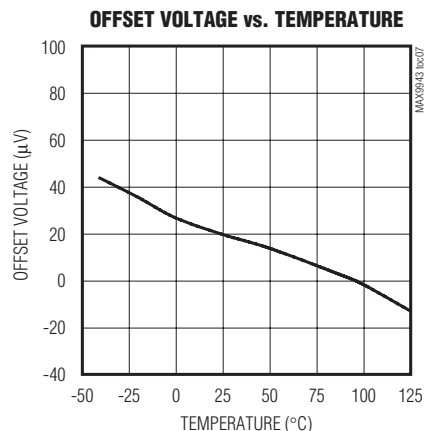
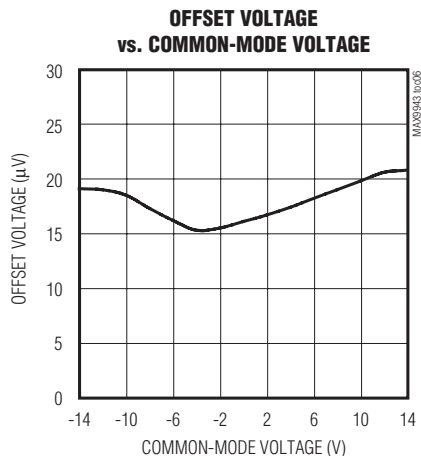
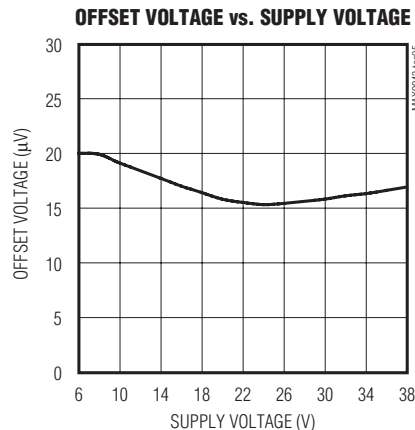
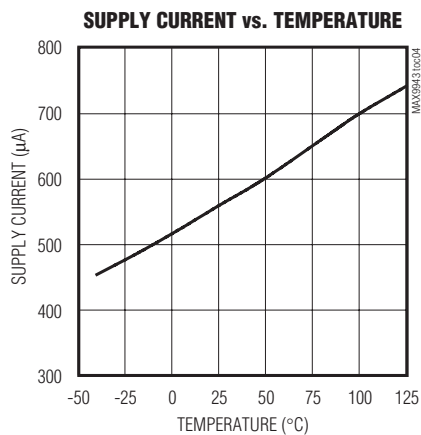
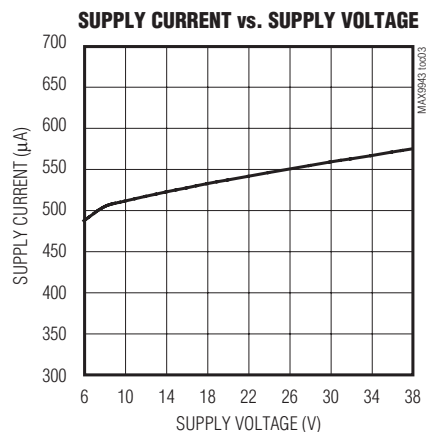
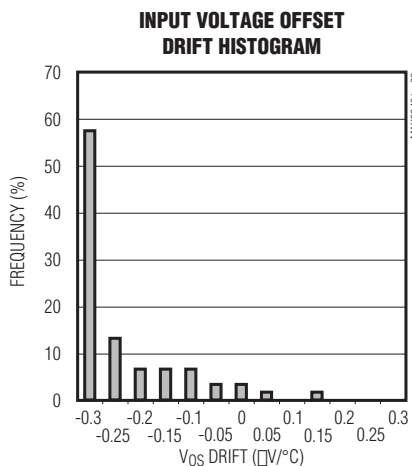
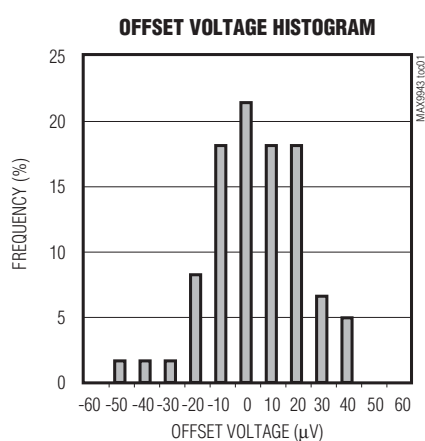
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Open-Loop Gain	A _{VOL}	-13.5V ≤ V _O ≤ +13.5V, R _L = 10kΩ, T _A = +25°C		115	130		dB
		-13.5V ≤ V _O ≤ +13.5V, R _L = 10kΩ, T _A = -40°C to +125°C		100			
		-12V ≤ V _O ≤ +12V, R _L = 600Ω, T _A = +25°C		100	110		
		-12V ≤ V _O ≤ +12V, R _L = 600Ω, T _A = -40°C to +85°C		90			
Output Voltage Swing	V _{OH}	R _L = 10kΩ		V _{CC} - 0.2			V
		R _L = 600Ω	T _A = +25°C	V _{CC} - 1.8			
			T _A = -40°C to +85°C	V _{CC} - 2			
	V _{OL}	R _L = 10kΩ		V _{EE} + 0.1			
		R _L = 600Ω	T _A = +25°C	V _{EE} + 1			
			T _A = -40°C to +85°C	V _{EE} + 1.1			
Short-Circuit Current	I _{SC}	T _A = +25°C		60			mA
		T _A = -40°C to +125°C		100			
AC CHARACTERISTICS							
Gain Bandwidth Product	GBWP			2.4			MHz
Slew Rate	SR	-5V ≤ V _{OUT} ≤ +5V		0.35			V/μs
Input Voltage Noise Density	e _n	f = 1kHz		17.6			nV/√Hz
Input Voltage Noise	TOTAL NOISE	0.1Hz ≤ f ≤ 10Hz		500			nV _{p-p}
Input Current Noise Density	i _n	f = 1kHz		0.18			pA/√Hz
Capacitive Loading	C _{LOAD}	No sustained oscillation		1000			pF

Note 3: All devices are 100% production tested at $T_A = +25^\circ C$. Temperature limits are guaranteed by design.

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Typical Operating Characteristics

($V_{CC} = 15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ to GND, $V_{GND} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

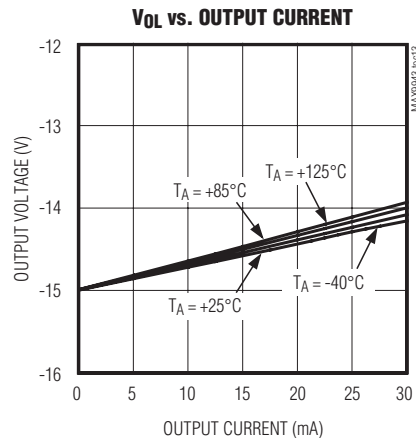
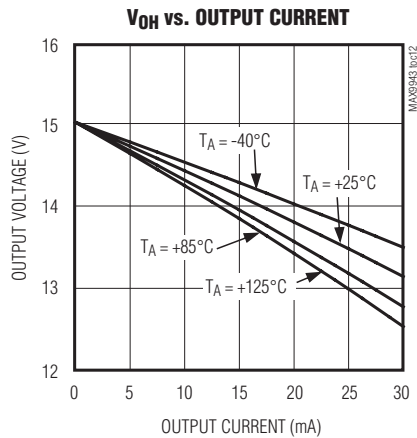
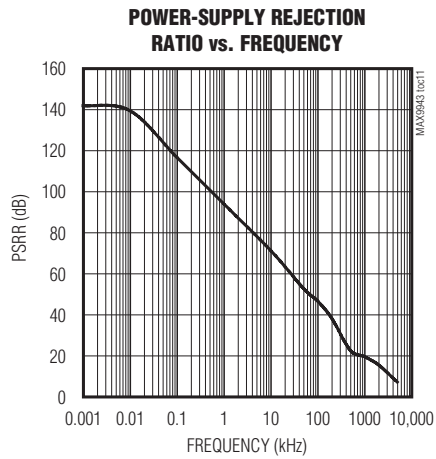
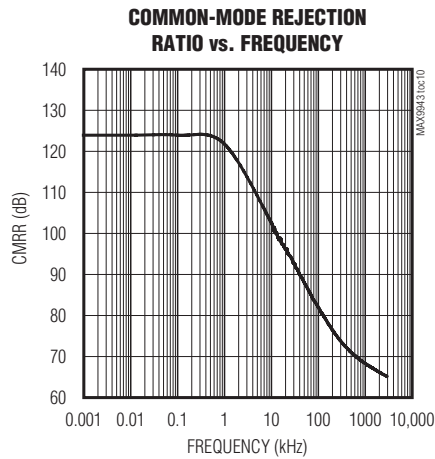
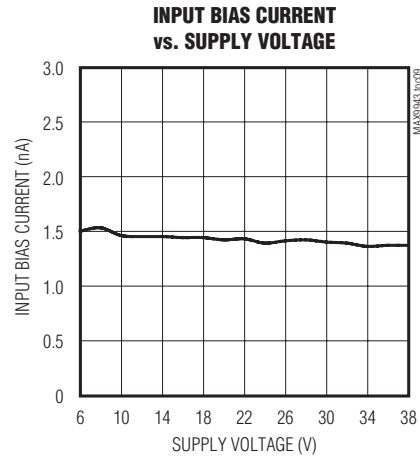
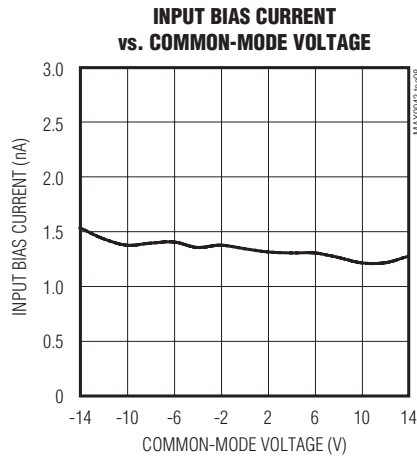


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Typical Operating Characteristics (continued)

($V_{CC} = 15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ to GND, $V_{GND} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

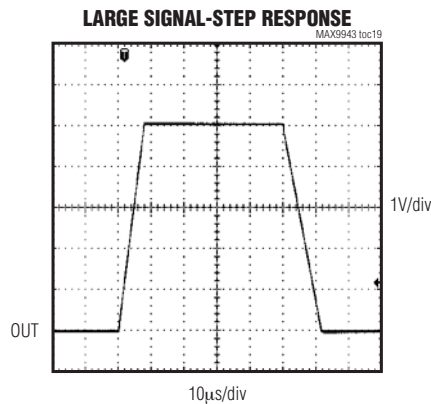
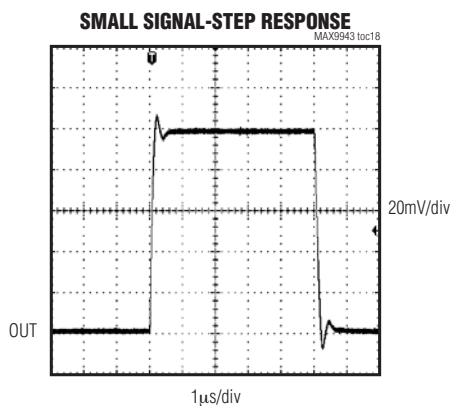
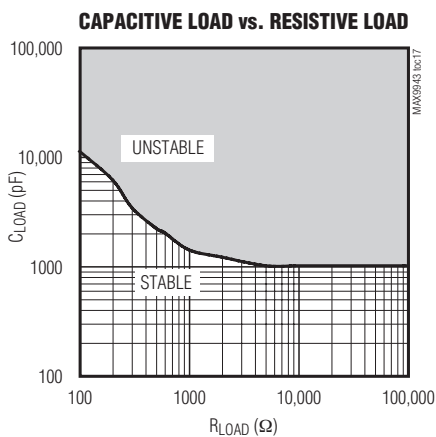
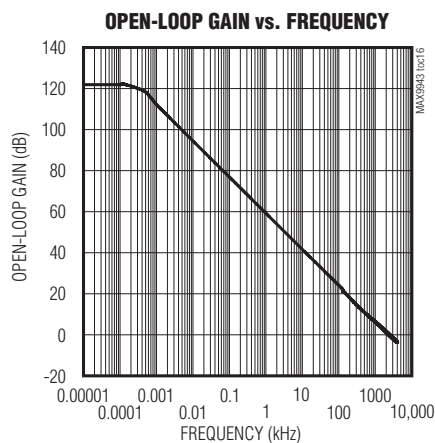
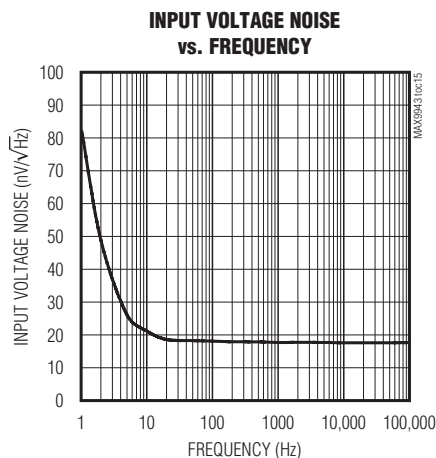
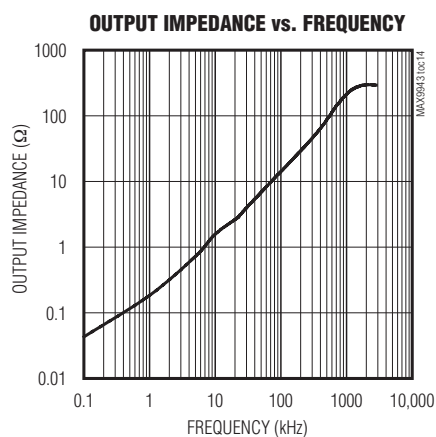
MAX9943/MAX9944



High-Voltage, Precision, Low-Power Op Amps

Typical Operating Characteristics (continued)

($V_{CC} = 15V$, $V_{EE} = -15V$, $V_{CM} = 0V$, $R_L = 10k\Omega$ to GND, $V_{GND} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



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MAX9943/MAX9944

Pin Description

MAX9943 6 TDFN-EP	MAX9943 8 μ MAX	MAX9944 8 SO/TDFN-EP	NAME	FUNCTION
1	6	—	OUT	Output
—	—	1	OUTA	Output A
—	—	7	OUTB	Output B
2	4	4	VEE	Negative Power Supply. Bypass with a 0.1 μ F capacitor to ground.
3	3	—	IN+	Positive Input
—	—	3	INA+	Positive Input A
—	—	5	INB+	Positive Input B
4	2	—	IN-	Negative Input
—	—	2	INA-	Negative Input A
—	—	6	INB-	Negative Input B
5	1, 5, 8	—	N.C.	No Connection
6	7	8	V _{CC}	Positive Power Supply. Bypass with a 0.1 μ F capacitor to ground.
—	—	—	EP	Exposed Pad (TDFN Only). Connect to a large V _{EE} plane to maximize thermal performance. Not intended as an electrical connection point.

Detailed Description

The MAX9943/MAX9944 are single/dual operational amplifiers designed for industrial applications. They operate from 6V to 38V supply range while maintaining excellent performance. These devices utilize a three-stage architecture optimized for low offset voltage and low input noise with only 550 μ A supply current. The devices are unity gain stable with a 1nF capacitive load. These well-matched devices guarantee the high open-loop gain, CMRR, PSRR, and low voltage offset.

The MAX9943/MAX9944 provide a wide input/output voltage range. The input terminals of the MAX9943/MAX9944 are protected from excessive differential voltage with back-to-back diodes. The input signal current is also limited by an internal series resistor. With a 40V differential voltage, the input current is limited to 20mA. The output can swing to the negative rail while delivering 20mA of current, which is ideal for loop-powered system applications. The specifications and operation of the MAX9943/MAX9944 family is guaranteed over the -40°C to +125°C temperature range.

Application Information

Bias Current vs. Input Common Mode

The MAX9943/MAX9944 use an internal bias current cancellation circuit to achieve very low bias current over a wide input common-mode range. For such a circuit to function properly, the input common mode must be at least 300mV away from the negative supply V_{EE}. The input common mode can reach the negative supply V_{EE}. However, in the region between V_{EE} and V_{EE} + 0.3V, there is an increase in bias current for both inputs.

Capacitive Load Stability

Driving large capacitive loads can cause instability in many op amps. The MAX9943/MAX9944 are stable with capacitive loads up to 1nF. The Capacitive Load vs. Resistive Load graph in the *Typical Operating Characteristics* gives the stable operation region for capacitive versus resistive loads. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output, as shown in Figure 1. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output.

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Power Supplies and Layout

The MAX9943/MAX9944 can operate with dual supplies from $\pm 3\text{V}$ to $\pm 19\text{V}$ or with a single supply from $+6\text{V}$ to $+38\text{V}$ with respect to ground. When used with dual supplies, bypass both V_{CC} and V_{EE} with their own $0.1\mu\text{F}$ capacitor to ground. When used with a single supply, bypass V_{CC} with a $0.1\mu\text{F}$ capacitor to ground. Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

Output Current Capability

The MAX9943/MAX9944 are capable of driving heavy loads such as the ones that can be found in loop-powered systems for remote sensors. The information is transmitted through $\pm 20\text{mA}$ or 4mA – 20mA current output across long lines that are terminated with low resistance loads (e.g., 600Ω). The *Typical Application Circuit* shows the MAX9944 used as a voltage-to-current converter with a current-sense amplifier in the feedback loop. Because of the high output current capability of the MAX9944, the device can be used to directly drive the current-loop.

The specifications and operation of the MAX9943/MAX9944 family is guaranteed over the -40°C to $+125^\circ\text{C}$ temperature range. However, when used in applications with $\pm 15\text{V}$ supply voltage (see Figure 3), the capability of driving more than $\pm 20\text{mA}$ of current is limited to the -40°C to $+85^\circ\text{C}$ temperature range. Use a lower supply voltage if this current must be delivered at a higher temperature range.

Input Common Mode and Output Swing

The MAX9943/MAX9944 input common-mode range can swing to the negative rail V_{EE} . The output voltage can swing to both the positive V_{CC} and the negative V_{EE} rails if the output stage is not heavily loaded. These two features are very important for applications where the MAX9943/MAX9944 are used with a single-supply (V_{EE} connected to ground). One of the applications that can benefit from these features is when the single-supply op amp is driving an ADC.

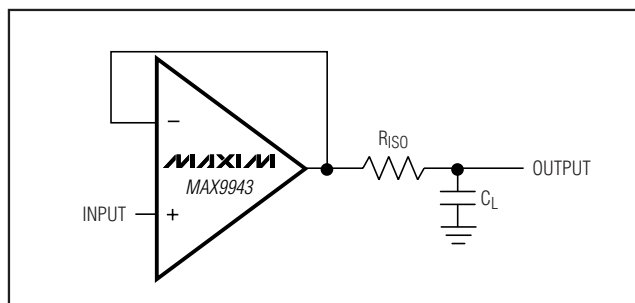


Figure 1. Capacitive Load Driving Circuit

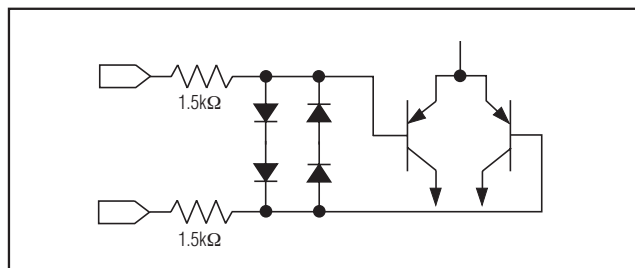


Figure 2. Input Protection Circuit

Input Differential Voltage Protection

During normal op-amp operation, the inverting and non-inverting inputs of the MAX9943/MAX9944 are at essentially the same voltage. However, either due to fast input voltage transients or due to other fault conditions, these pins can be forced to be at two different voltages.

Internal back-to-back diodes and series resistors protect the inputs from an excessive differential voltage (see Figure 2). Therefore, $IN+$ and $IN-$ can be any voltage within the range shown in the absolute maximum rating. Note the protection time is still dependent on the package thermal limits.

Chip Information

PROCESS: BiCMOS

High-Voltage, Precision, Low-Power Op Amps

MAX9943/MAX9944

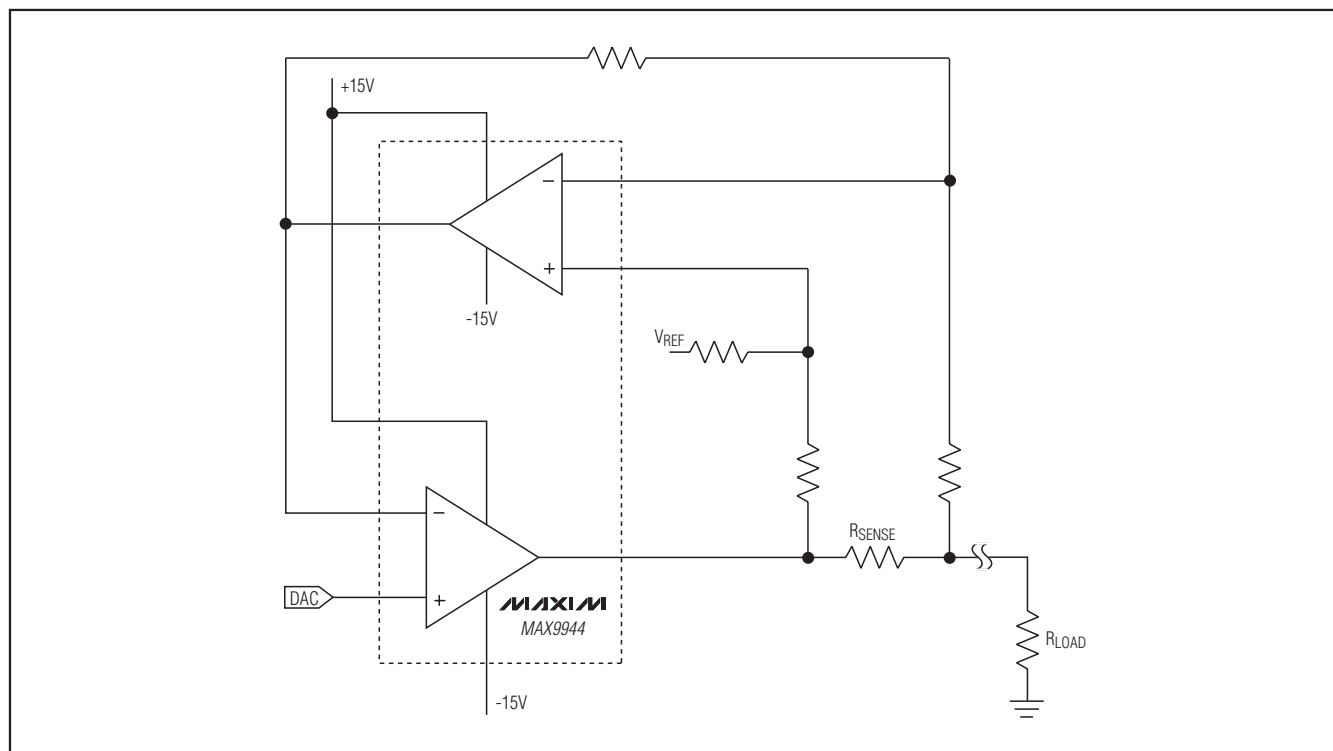
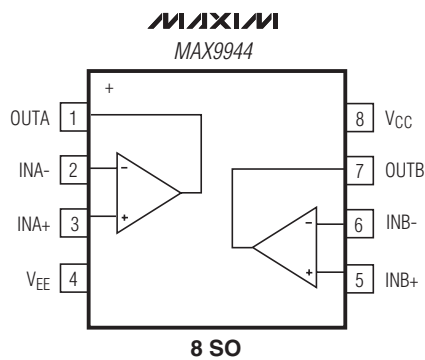
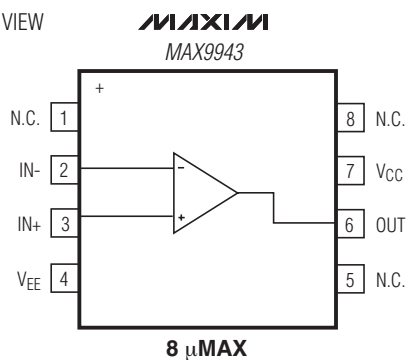


Figure 3. Typical $\pm 20\text{mA}$ Current-Source in Loop-Powered Systems

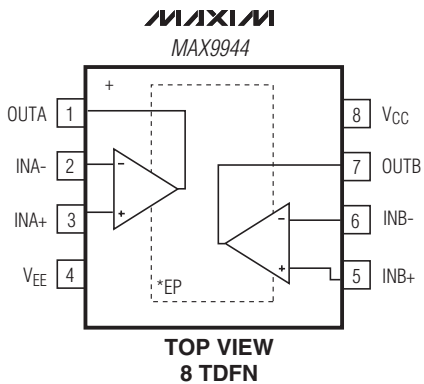
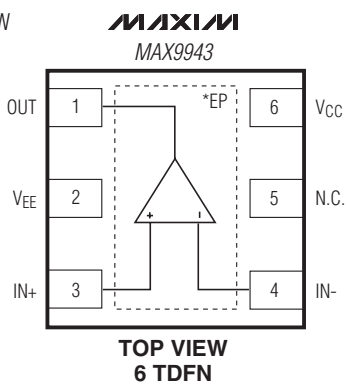
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Pin Configurations

TOP VIEW



TOP VIEW



NOT TO SCALE.
*EP = EXPOSED PAD.

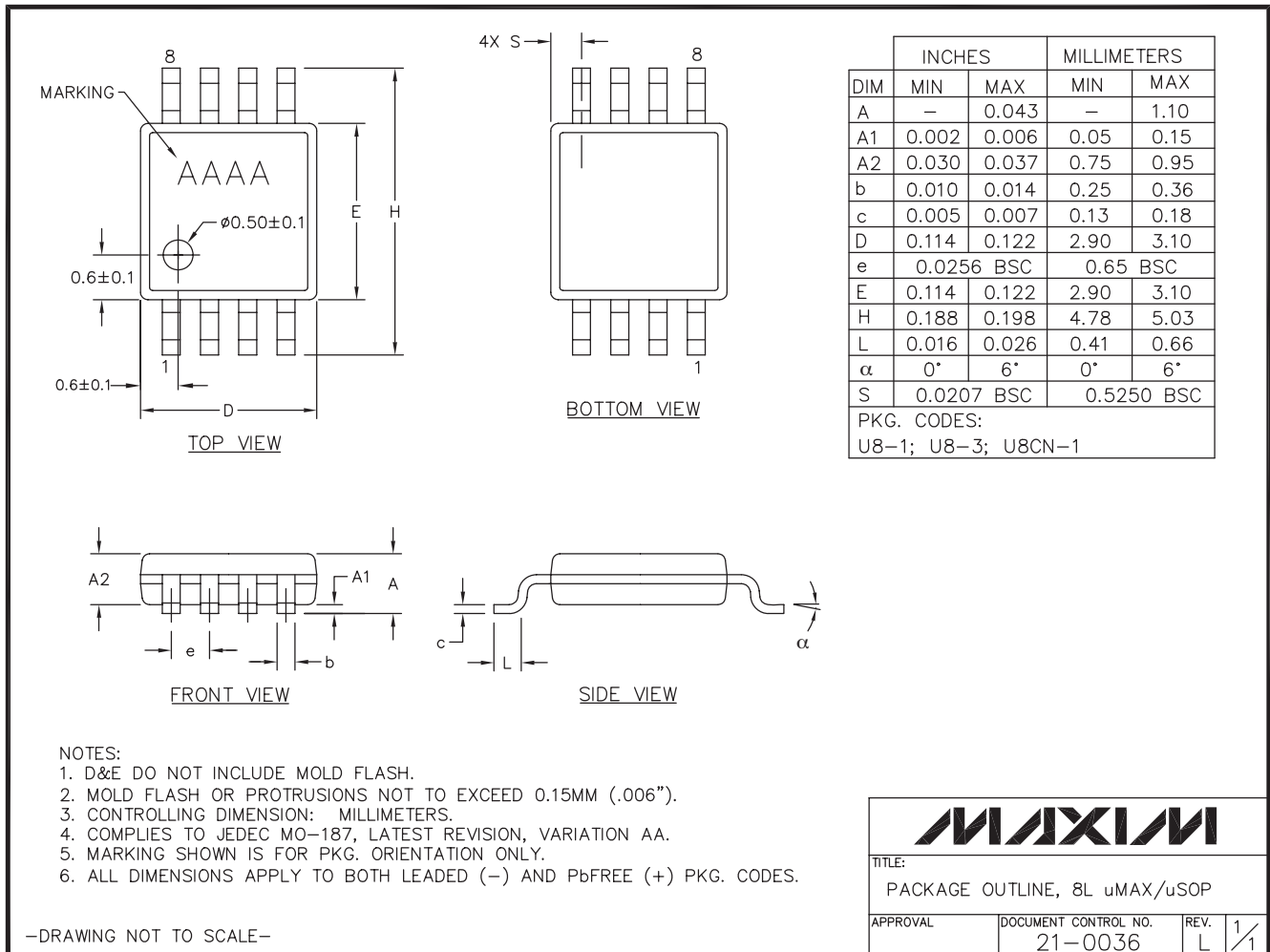
High-Voltage, Precision, Low-Power Op Amps

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 μ MAX	U8+1	21-0036	90-0092
6 TDFN-EP	T633+2	21-0137	90-0058
8 SO	S8+4	21-0041	90-0096
8 TDFN-EP	T833+2	21-0137	90-0059

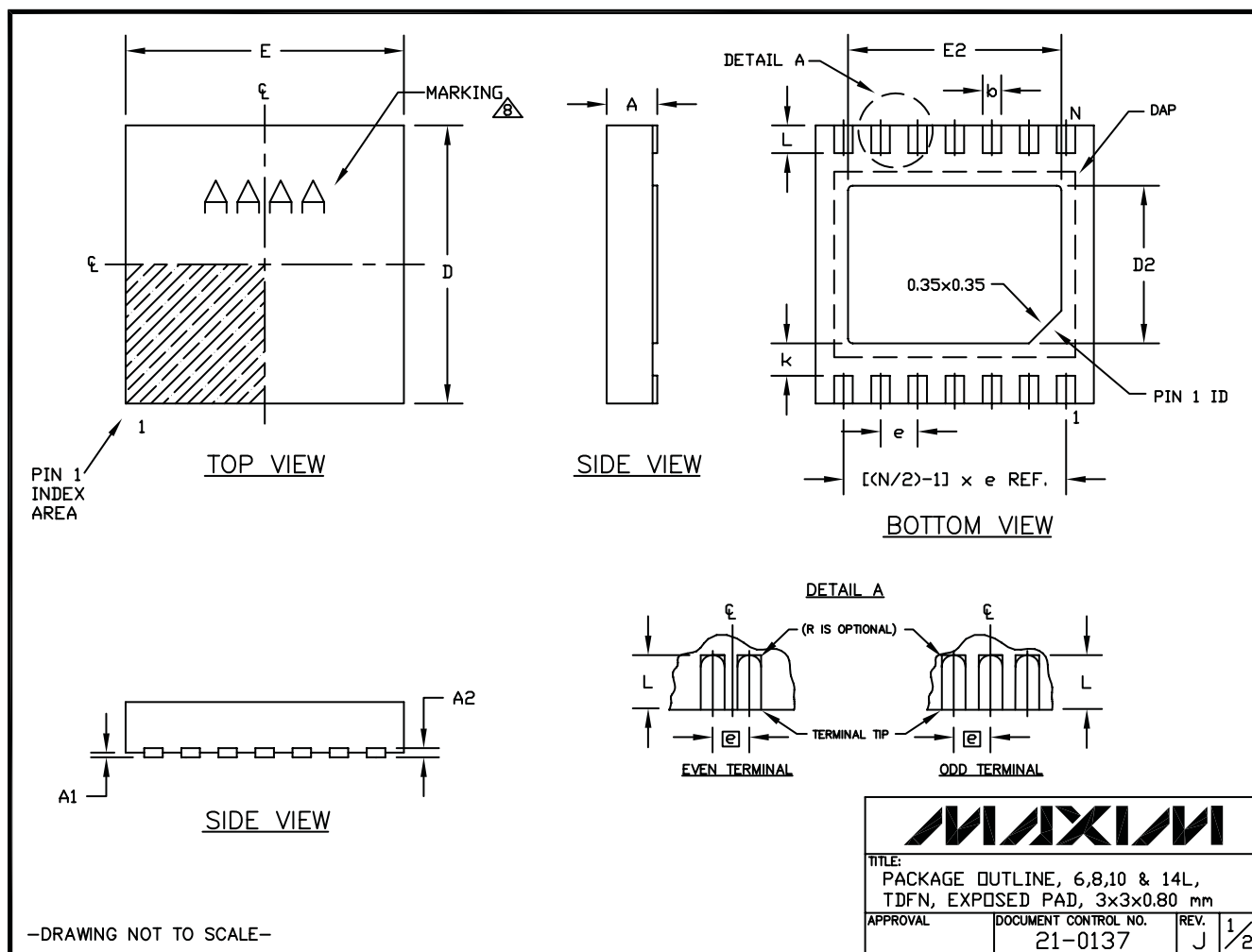
MAX9943/MAX9944



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MAX9943/MAX9944

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

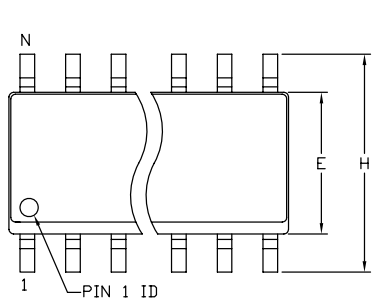
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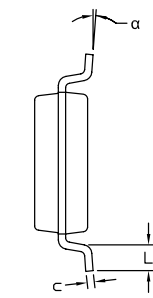
High-Voltage, Precision, Low-Power Op Amps

Package Information (continued)

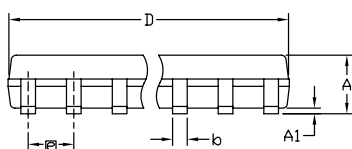
For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050	BSC	1.27	BSC
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
alpha	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			

VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6, S14M-4, S14M-5, S14M-6, S14M-7			

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F, S16M-3, S16M-6			

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
- MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
- LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
- MEETS JEDEC MS012
- ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

TITLE:
PACKAGE OUTLINE,
8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO. 21-0041	REV. C	1/1
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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/09	Initial release	—
1	4/09	Removed future product reference for the MAX9944, updated EC table	1, 2
2	6/09	Corrected TOC 13 and added rail-to-rail output feature	1, 3, 5, 8
3	4/11	Updated <i>Pin Description</i> section	7

MAX9943/MAX9944

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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