## ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- $V_{CC}$ to GND ..... 6V
- All Other Pins to GND ..... -0.3V to ($V_{CC}$ + 0.3V)

Current into Input Pins ..... ±20mA
Duration of Output Short-Circuit to GND or $V_{CC}$ ..... Continuous
Continuous Power Dissipation ($T_A$ = +70°C)
- 5-Pin SC70 (derate 3.1mW/°C above +70°C) ..... 247mW
- 5-Pin SOT23 (derate 3.1mW/°C above +70°C) ..... 247mW
- 8-Pin SOT23 (derate 5.2mW/°C above +70°C) ..... 412mW
- 8-Pin µMAX (derate 4.5mW/°C above +70°C) ..... 362mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) ..... 471mW

Operating Temperature Range ..... -40°C to +85°C
Military Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
- Lead (Pb)-free ..... +260°C
- Containing lead (Pb) ..... +240°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5V, $V_{CM}$ = 0V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Operating Supply Voltage Range | $V_{CC}$ | Inferred from PSRR | | 2.1 | | 5.5 | V |
| Supply Current per Comparator | $I_{CC}$ | $V_{CC}$ = 5V | $T_A$ = +25°C | | 3 | 5.2 | µA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 7.5 | |
| | | $V_{CC}$ = 3V | | | 2.4 | | |
| Power-Supply Rejection Ratio | PSRR | 2.1V ≤ $V_{CC}$ ≤ 5.5V | | 54 | 77 | | dB |
| Common-Mode Voltage Range | $V_{CMR}$ | (Note 2) | | 0 | | $V_{CC}$ - 1.2 | V |
| Input Offset Voltage | $V_{OS}$ | | | | ±1 | ±8 | mV |
| Input Offset Current | $I_{OS}$ | | | | 1 | | nA |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0.2V (Note 3) | | | -5 | -20 | nA |
| Input Capacitance | $C_{IN}$ | | | | 3 | | pF |
| Common-Mode Rejection Ratio | CMRR | 0V ≤ $V_{CM}$ ≤ ($V_{CC}$ - 1.2V) | | 60 | 82 | | dB |
| OUT_ Output-Voltage High | $V_{OH}$ | $I_{SOURCE}$ = 2mA | | $V_{CC}$ - 0.4 | | | V |
| OUT_ Output-Voltage Low | $V_{OL}$ | $I_{SINK}$ = 2mA | | | | 0.4 | V |
| Propagation Delay Low to High | $t_{PD+}$ | $C_{LOAD}$ = 10pF, overdrive = 100mV | | | 580 | | ns |
| Propagation Delay High to Low | $t_{PD-}$ | $C_{LOAD}$ = 10pF, overdrive = 100mV | | | 250 | | ns |
| Rise/Fall Time | | $C_{LOAD}$ = 10pF | | | 1.6 | | ns |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. All temperature limits are guaranteed by design.
**Note 2:** Inferred from CMRR. Either input can be driven to the absolute maximum limit without output inversion, as long as the other input is within the input voltage range.
**Note 3:** Guaranteed by design.



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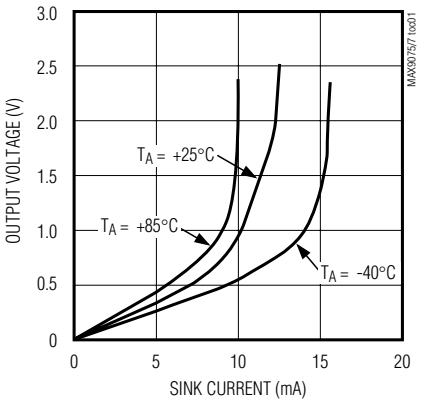
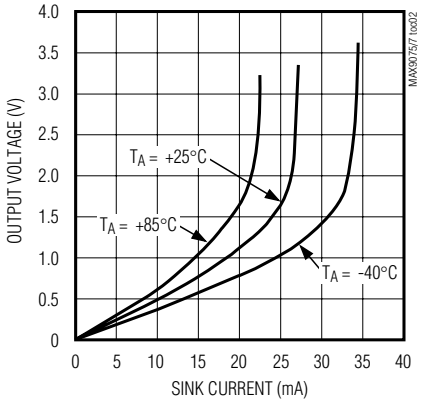
## Typical Operating Characteristics

($V_{CC}$ = 5V, $V_{CM}$ = 0V, 100mV overdrive, $T_A$ = +25°C, unless otherwise noted.)

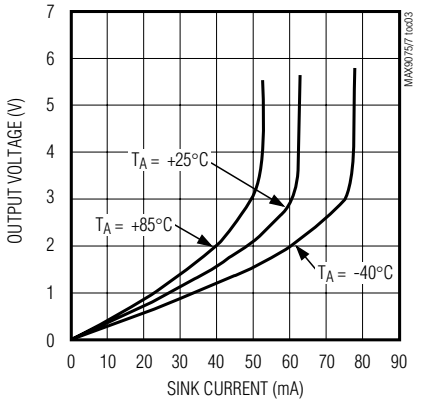
**OUTPUT-VOLTAGE LOW vs. SINK CURRENT ($V_{CC}$ = 2.1V)**



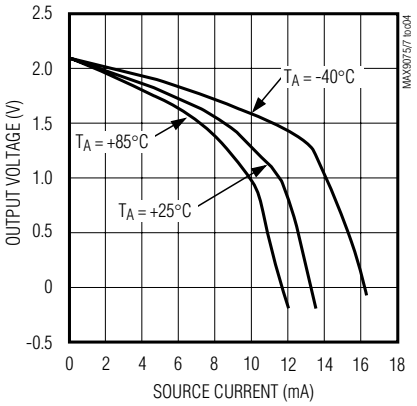

**OUTPUT-VOLTAGE LOW vs. SINK CURRENT ($V_{CC}$ = 3V)**



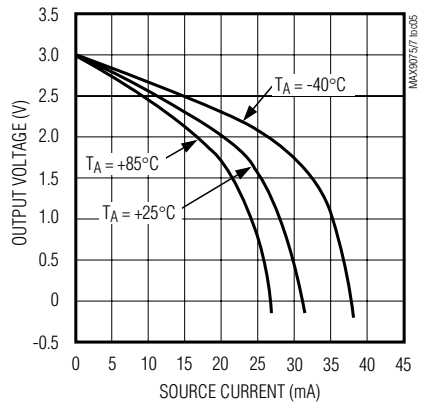

**OUTPUT-VOLTAGE LOW vs. SINK CURRENT ($V_{CC}$ = 5V)**



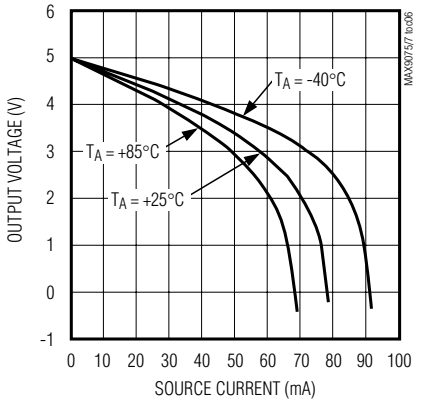

**OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT ($V_{CC}$ = 2.1V)**



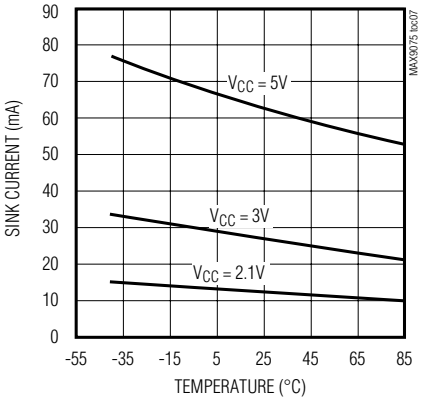

**OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT ($V_{CC}$ = 3V)**



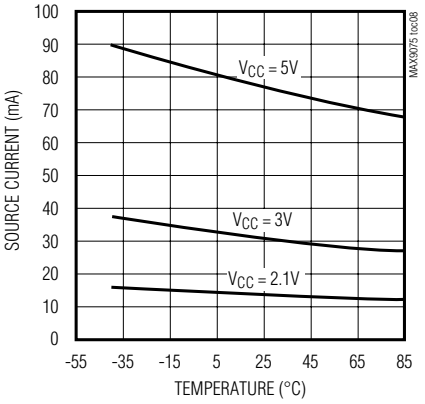

**OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT ($V_{CC}$ = 5V)**



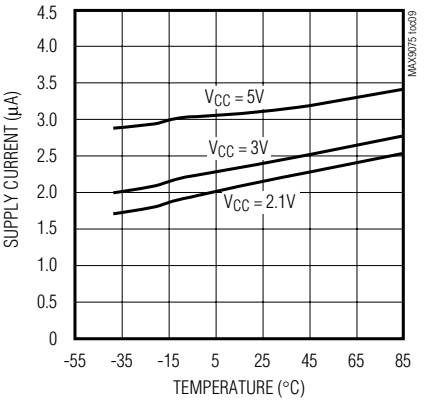

**SHORT-CIRCUIT SINK CURRENT vs. TEMPERATURE**




**SHORT-CIRCUIT SOURCE CURRENT vs. TEMPERATURE**




**SUPPLY CURRENT vs. TEMPERATURE (OUT = HIGH)**



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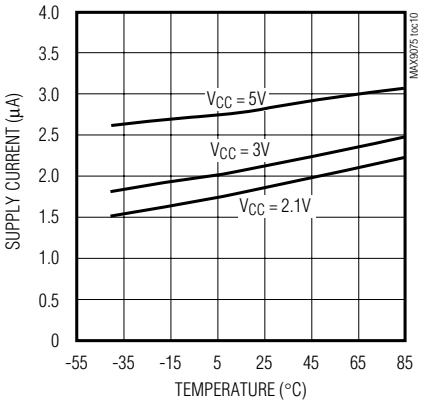
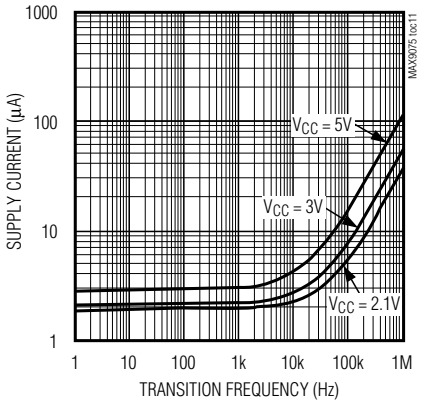
### Typical Operating Characteristics (continued)

($V_{CC}$ = 5V, $V_{CM}$ = 0V, 100mV overdrive, $T_A$ = +25°C, unless otherwise noted.)

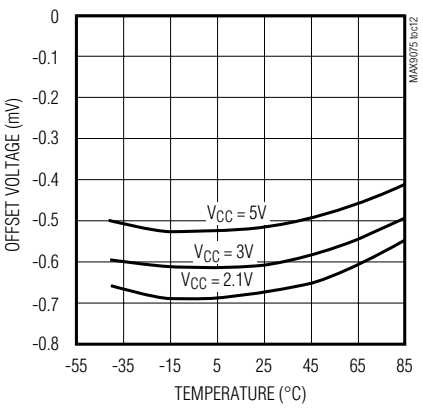
**SUPPLY CURRENT vs. TEMPERATURE (OUT = LOW)**



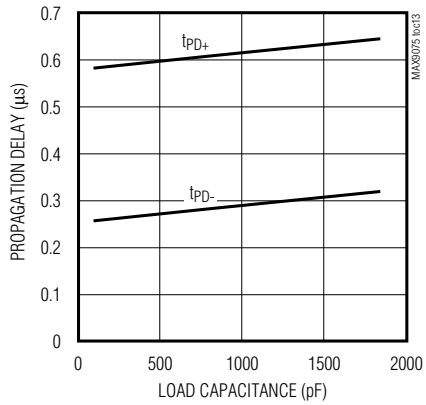

**SUPPLY CURRENT vs. OUTPUT TRANSITION FREQUENCY**



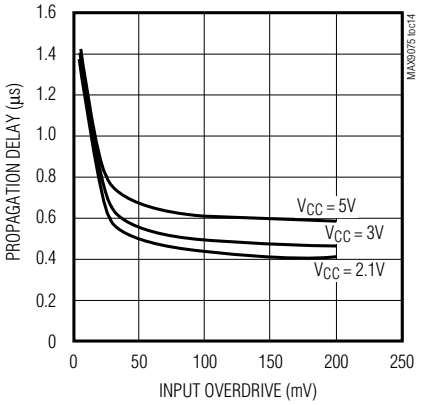

**INPUT OFFSET VOLTAGE vs. TEMPERATURE**



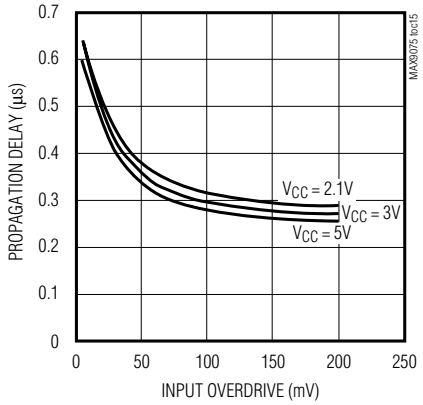

**PROPAGATION DELAY vs. LOAD CAPACITANCE**



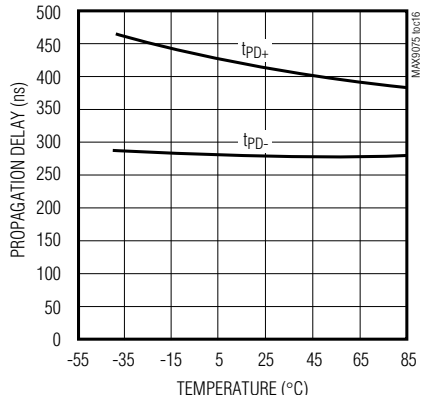

**PROPAGATION DELAY vs. INPUT OVERDRIVE ($t_{PD+}$)**



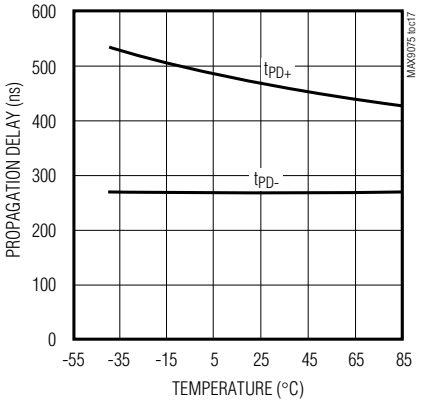

**PROPAGATION DELAY vs. INPUT OVERDRIVE ($t_{PD-}$)**



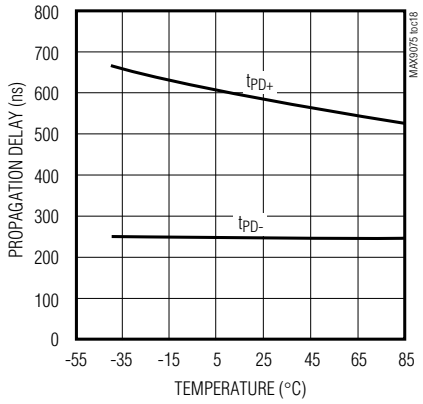

**PROPAGATION DELAY vs. TEMPERATURE ($V_{CC}$ = 2.1V)**




**PROPAGATION DELAY vs. TEMPERATURE ($V_{CC}$ = 3V)**




**PROPAGATION DELAY vs. TEMPERATURE ($V_{CC}$ = 5V)**







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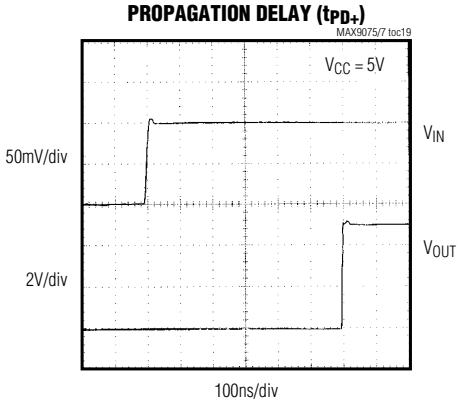
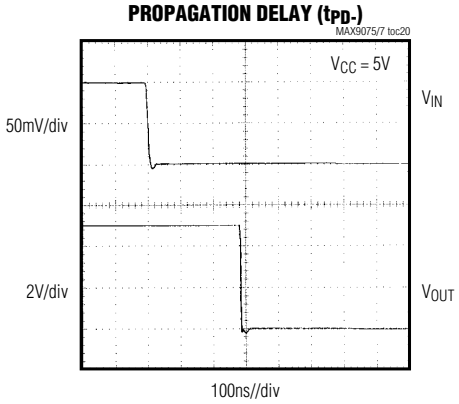
## Typical Operating Characteristics (continued)

($V_{CC}$ = 5V, $V_{CM}$ = 0V, 100mV overdrive, $T_A$ = +25°C, unless otherwise noted.)

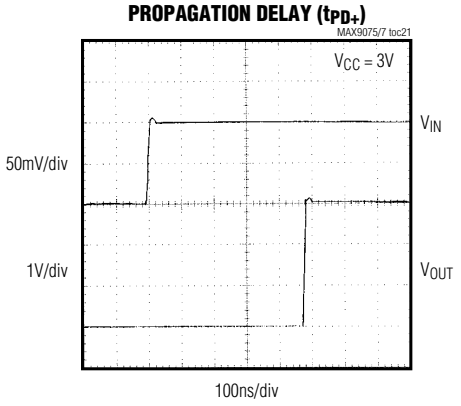
**PROPAGATION DELAY ($t_{PD+}$)**



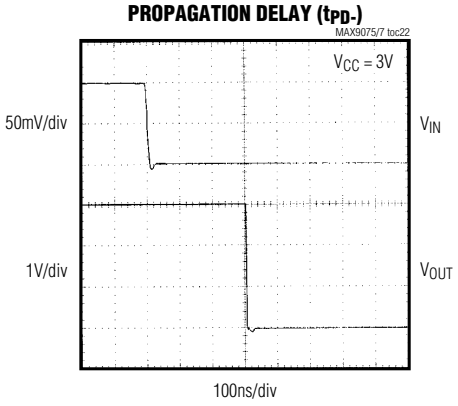

**PROPAGATION DELAY ($t_{PD-}$)**



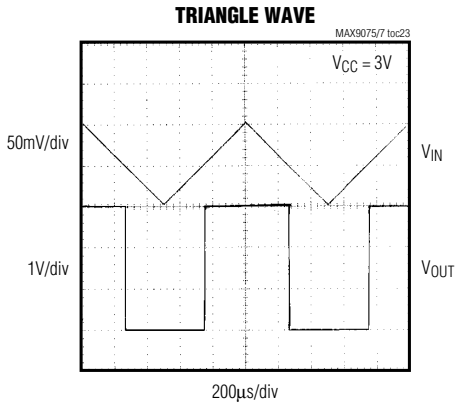

**PROPAGATION DELAY ($t_{PD+}$)**



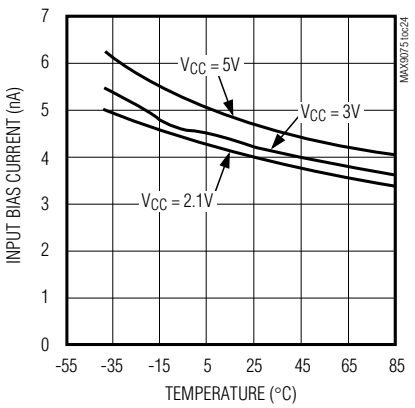

**PROPAGATION DELAY ($t_{PD-}$)**




**TRIANGLE WAVE**




**INPUT BIAS CURRENT vs. TEMPERATURE**



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## Pin Description

| PIN | | | | NAME | FUNCTION |
|---|---|---|---|---|---|
| MAX9075 | | MAX9077 | | | |
| SOT23 | SC70 | µMAX/SO | SOT23 | | |
| 1 | 1 | — | — | OUT | Comparator Output |
| — | — | 1 | 1 | OUTA | Output of Comparator A |
| 2 | 2 | 4 | 2 | GND | Ground |
| 3 | 3 | — | — | IN+ | Noninverting Comparator Input |
| — | — | 3 | 4 | INA+ | Noninverting Input of Comparator A |
| 4 | 4 | — | — | IN- | Inverting Comparator Input |
| — | — | 2 | 3 | INA- | Inverting Input of Comparator A |
| 5 | 5 | 8 | 8 | $V_{CC}$ | Positive Supply Voltage |
| — | — | 5 | 5 | INB+ | Noninverting Input of Comparator B |
| — | — | 6 | 6 | INB- | Inverting Input of Comparator B |
| — | — | 7 | 7 | OUTB | Output of Comparator B |

## Detailed Description

The MAX9075/MAX9077 feature a 580ns propagation delay from an ultra-low supply current of only 3µA per comparator. These devices are capable of single-supply operation in the 2.1V to 5.5V range. Large internal output drivers allow rail-to-rail output swing with up to 2mA loads. Both comparators offer a push-pull output that sinks and sources current.

### Comparator Output

The MAX9075/MAX9077 are designed to maintain a low-supply current during repeated transitions by limiting the shoot-through current.

### Noise Considerations, Comparator Input

The input common-mode voltage range for these devices extends from 0V to $V_{CC}$ - 1.2V. Unlike many other comparators, the MAX9075/MAX9077 can operate at any differential input voltage within these limits. Input bias current is typically -5nA if the input voltage is between the supply rails.

Although the comparators have a very high gain, useful gain is limited by noise. The comparator has a wideband peak-to-peak noise of approximately 70µV.

## Applications Information

### Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage divider from the output of the comparator sets the trip voltage. Therefore, the trip voltage is related to the output voltage. Set the hysteresis with three resistors using positive feedback, as shown in Figure 1.

The design procedure is as follows:

1) Choose R3. The leakage current of IN+ may cause a small error; however, the current through R3 can be approximately 500nA and still maintain accuracy. The added supply current due to the circuit at the trip point is $V_{CC}$/R3; 10MΩ is a good practical value for R3, as this keeps the current well below the supply current of the chip.
2) Choose the hysteresis voltage ($V_{HYS}$), which is the voltage between the upper and lower thresholds. In this example, choose $V_{HYS}$ = 50mV and assume $V_{REF}$ = 1.2V and $V_{CC}$ = 5V.
3) Calculate R1 as follows:

$$R1 = R3 \times V_{HYS}/V_{CC} = 10M\Omega \times 0.05/5 = 100k\Omega$$



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4) Choose the threshold voltage for $V_{IN}$ rising ($V_{THR}$). In this example, choose $V_{THR}$ = 3V.

5) Calculate R2 as follows:

$$R2 = 1/\{[V_{THR}/(V_{REF} \times R1)] - 1/R1 - 1/R3\} = 1/\{[3 / (1.2 \times 100k\Omega)] - 1/100k\Omega - 1/10M\Omega\} = 67.114k\Omega$$

A 1% preferred value is 64.9kΩ.

6) Verify the threshold voltages with these formulas:

$V_{IN}$ rising:

$$V_{THR} = V_{REF} \times R1\ (1/R1 + 1/R2 + 1/R3)$$

$V_{IN}$ falling:

$$V_{THF} = V_{THR} - (R1 \times V_{CC})/R3$$

7) Check the error due to input bias current (5nA). If the error is too large, reduce R3 and recalculate.

$$V_{TH} = I_B\ (R1 \times R2 \times R3)/(R1 + R2 + R3) = 0.2mV$$

### Board Layout and Bypassing

Use 10nF power-supply bypass capacitors. Use 100nF bypass capacitors when supply impedance is high, when supply leads are long, or when excessive noise is expected on the supply lines. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between IN- and OUT. For slow-moving input signals (rise time > 1ms) use a 1nF capacitor between IN+ and IN-.

## Chip Information

PROCESS: BiCMOS

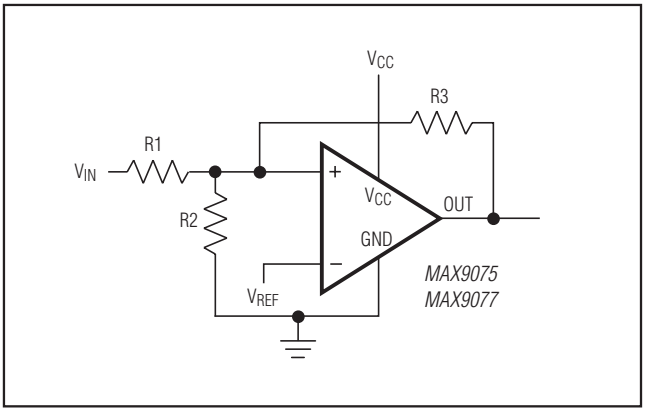
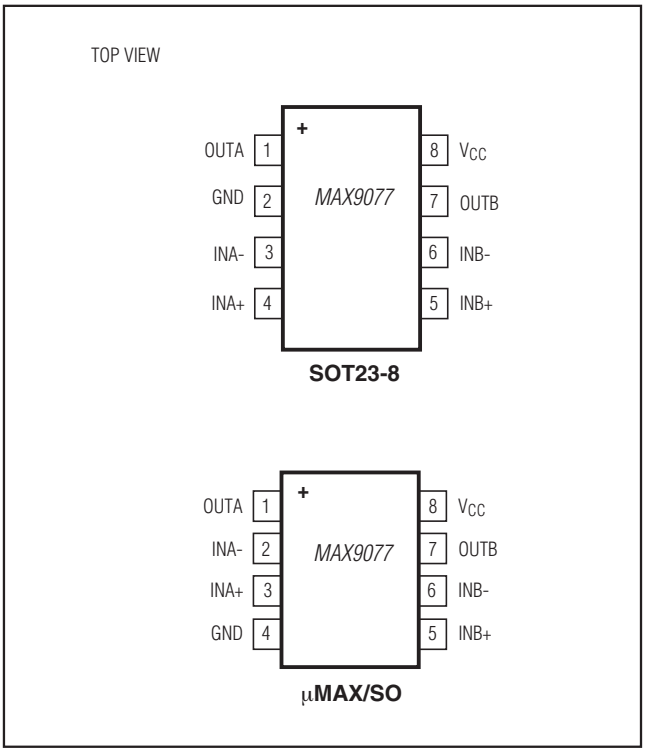



*Figure 1. Adding Hysteresis*

## Pin Configurations (continued)



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## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 5 SC70 | X5+1 | 21-0076 | 90-0188 |
| 5 SOT23 | U5+1 | 21-0057 | 90-0174 |
| 8 SOT23 | K8+2 | 21-0078 | 90-0176 |
| 8 µMAX | U8+1 | 21-0036 | 90-0092 |
| 8 S0 | S8+4 | 21-0041 | 90-0096 |



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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 0/99 | Initial release | — |
| 3 | 1/07 | Revised *Absolute Maximum Ratings* | 2 |
| 4 | 12/12 | Added MAX9077MSA/PR2 to *Ordering Information* and updated for lead-free notation. Revised *Absolute Maximum Ratings*, *Electrical Characteristics*, and the *Noise Considerations, Comparator Input* section. | 1, 2, 6 |

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