Dual, 5A, 2MHz Step-Down Regulators

ABSOLUTE MAXIMUM RATINGS

IN_, LX_, V_{DD}, VDL, PWRGD_ to GND	-0.3V to +4.5V
V_{DD}, VDL to IN_	-0.3V to +4.5V
EN_, SS_, COMP_, FB_, REFIN, FSYNC to GND	-0.3V to the lower of (V_{VDD} + 0.3V) and (V_{VDL} + 0.3V)
Continuous LX_ Current (Note 1)	5.5A_{RMS}
BST_ to LX_	-0.3V to +4.5V
PGND_ to GND	-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C) 32-Pin TQFN (5mm x 5mm) (derate 34.5mW/°C above +70°C)	2758.6mW
Operating Ambient Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Note 1: LX_ have internal clamp diodes to PGND_ and IN_. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.7°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

($V_{IN\_}$ = V_{VDD} = V_{VDL} = 3.3V, $V_{FB\_}$ = 0.5V, $V_{SS\_}$ = V_{REFIN} = 600mV, PGND_ = GND, R_{FSYNC} = 10kΩ, L = 0.47µH, $C_{BST\_}$ = 0.1µF, $C_{SS\_}$ = 0.022µF, PWRGD_ not connected; T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN1, IN2, VDL, VDD						
IN_, VDL, and V_{DD} Voltage Range	(Note 3)	MAX8855	2.35		3.60	V
		MAX8855A	2.25		3.60	
IN_ Supply Current	1MHz switching, no load	$V_{IN\_}$ = 2.5V		1.9	3.5	mA
		$V_{IN\_}$ = 3.3V		2.8	5	
V_{DD} + VDL Supply Current	1MHz switching, V_{DD} = VDL	V_{VDD} = 2.5V		7.2		mA
		V_{VDD} = 3.3V		10	15	
Shutdown Supply Current (I_{IN1} + I_{IN2} + I_{VDD} + I_{VDL})	$V_{IN\_}$ = V_{VDD} = V_{VDL} = $V_{BST\_}$ - $V_{LX\_}$ = 3.6V, $V_{EN\_}$ = 0V	T_A = +25°C			11	µA
		T_A = +85°C		0.3		
IN_, V_{DD} Undervoltage Lockout Threshold UVLO Monitors V_{DD}, IN1, and IN2	Rising			2.0	2.2	V
	Falling		1.8	1.9		
IN_, V_{DD} Undervoltage Lockout Deglitch				2		µs
BST1, BST2						
Shutdown BST_ Current	$V_{IN\_}$ = V_{VDD} = V_{VDL} = $V_{BST\_}$ = 3.6V, $V_{EN\_}$ = 0V, $V_{LX\_}$ = 0 or 3.6V	T_A = +25°C			2	µA
		T_A = +85°C		0.02		
COMP1, COMP2						
COMP_ Clamp Voltage, High	V_{VDD} = $V_{IN\_}$ = 2.25V to 3.6V, $V_{FB\_}$ = 0.7V		1.80	2.00	2.25	V
COMP_ Slew Rate				1.40		V/µs
COMP_ Shutdown Resistance	From COMP_ to GND, $V_{EN\_}$ = 0V			7	25	Ω

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN\_}$ = V_{VDD} = V_{VDL} = 3.3V, $V_{FB\_}$ = 0.5V, $V_{SS\_}$ = V_{REFIN} = 600mV, PGND_ = GND, R_{FSYNC} = 10kΩ, L = 0.47µH, $C_{BST\_}$ = 0.1µF, $C_{SS\_}$ = 0.022µF, PWRGD_ not connected; T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
ERROR AMPLIFIER							
FB_ Regulation Voltage	$V_{COMP\_}$ = 1V to 2V	V_{VDD} = $V_{IN\_}$ = 2.5V to 3.3V (MAX8855)		0.594	0.600	0.606	V
		V_{VDD} = $V_{IN\_}$ = 2.25V to 3.3V (MAX8855A)					
FB_ Regulation Voltage with External Reference	$V_{COMP\_}$ = 1V to 2V	V_{VDD} = $V_{IN\_}$ = 2.5V to 3.3V (MAX8855)		0.594	0.600	0.606	V
		V_{VDD} = $V_{IN\_}$ = 2.25V to 3.3V (MAX8855A)					
Error Amplifier Common-Mode-Input Range				0		V_{VDD} - 1.6	V
Error Amplifier Maximum Output Current				1			mA
FB_ Input Bias Current	$V_{FB\_}$ = 0.605V		T_A = +25°C		40	300	nA
			T_A = +85°C		37		
REFIN, SS2							
REFIN Input Bias Current	$V_{FB\_}$ = 0.610V		T_A = +25°C		90	500	nA
			T_A = +85°C		65		
REFIN Common-Mode Range	MAX8855	V_{VDD} = 2.35V to 2.6V		0		V_{VDD} - 1.65	V
	MAX8855A	V_{VDD} = 2.25V to 2.6V					
	V_{VDD} = 2.6V to 3.6V			0		V_{VDD} - 1.70	
LX1, LX2 (ALL PINS COMBINED)							
LX_ On-Resistance, High	$I_{LX\_}$ = -2A	$V_{IN\_}$ = $V_{BST\_}$ - $V_{LX\_}$ = 3.3V			31	52	mΩ
		$V_{IN\_}$ = $V_{BST\_}$ - $V_{LX\_}$ = 2.5V			34		
LX_ On-Resistance, Low	$I_{LX\_}$ = -2A	$V_{IN\_}$ = 3.3V			27	46	mΩ
		$V_{IN\_}$ = 2.5V			29		
LX_ Current-Limit Threshold	High-side sourcing and freewheeling			7.0	8.3	9.6	A
LX_ Leakage Current	$V_{IN\_}$ = 3.6V, $V_{EN\_}$ = 0V	$V_{LX\_}$ = 3.6V	T_A = +25°C			+0.1	µA
			T_A = +85°C		-0.1		
		$V_{LX\_}$ = 0V	T_A = +25°C	-10			
			T_A = +85°C		-0.1		
LX_ Switching Frequency	R_{FSYNC} = 10kΩ			0.9	1.0	1.1	MHz
	R_{FSYNC} = 4.75kΩ			1.80	2.0	2.2	
LX_ Minimum Off-Time					50		ns
LX_ Minimum On-Time					95		ns
LX_ Maximum Duty Cycle	R_{FSYNC} = 10kΩ			90	95		%
Maximum LX_ Output Current				3			A_{RMS}

ELECTRICAL CHARACTERISTICS (continued)

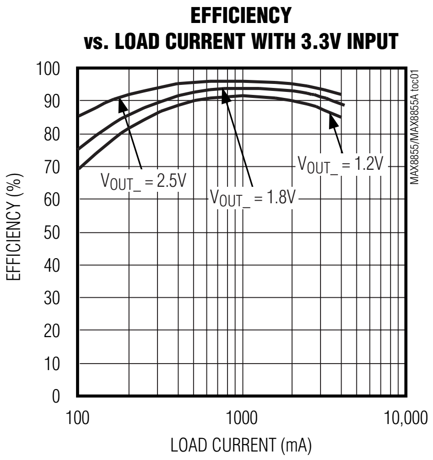
($V_{IN\_}$ = V_{VDD} = V_{VDL} = 3.3V, $V_{FB\_}$ = 0.5V, $V_{SS\_}$ = V_{REFIN} = 600mV, PGND_ = GND, R_{FSYNC} = 10kΩ, L = 0.47µH, $C_{BST\_}$ = 0.1µF, $C_{SS\_}$ = 0.022µF, PWRGD_ not connected; T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

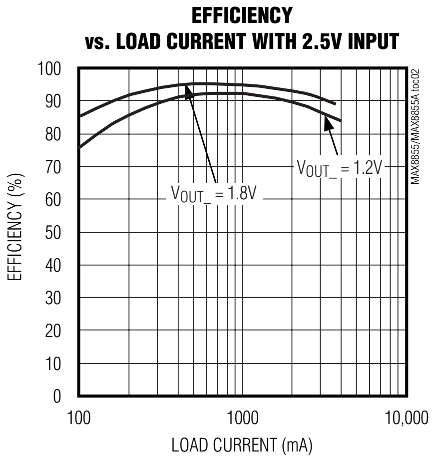
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EN1, EN2						
EN_ Logic-Low					0.7	V
EN_ Logic-High			1.7			V
EN_ Input Current	$V_{EN\_}$ = 0 or 3.6V, V_{VDD} = 3.6V	T_A = +25°C	-1		+1	µA
		T_A = +85°C		0.01		
SS1, SS2						
SS_ Charging Current	$V_{SS\_}$ = 300mV		5	8	11	µA
REFIN, SS2						
Discharge Resistance	In shutdown or a fault condition			335		Ω
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold (Independent Channels)				+165		°C
Thermal-Shutdown Hysteresis				20		°C

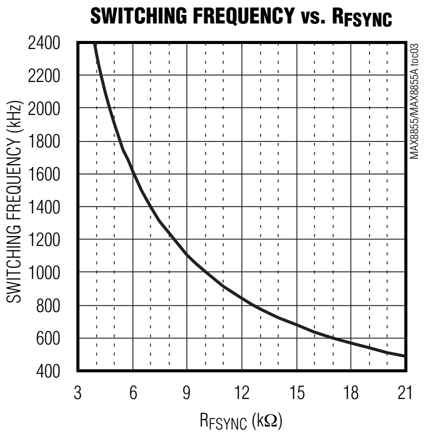
Note 2: All devices 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 3: V_{VDD} must equal V_{VDL} and be equal to or greater than $V_{IN\_}$.

Typical Operating Characteristics

(V_{IN1} = V_{IN2} = 3.3V, MAX8855/MAX8855A, circuit of Figure 6, T_A = +25°C, unless otherwise noted.)







Typical Operating Characteristics (continued)

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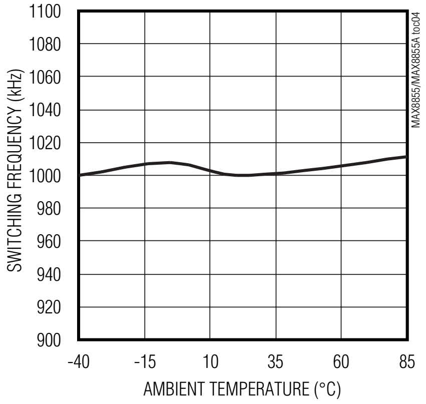
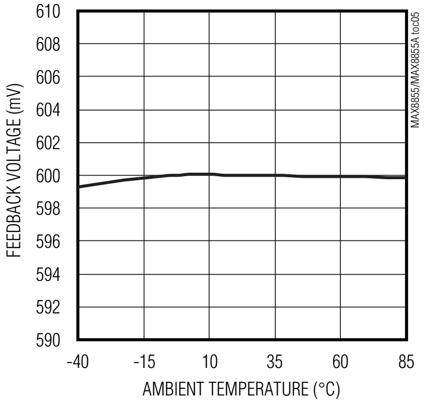
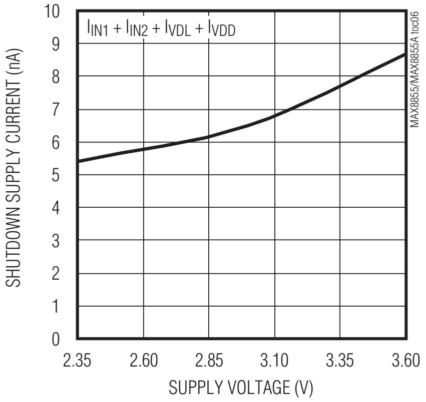


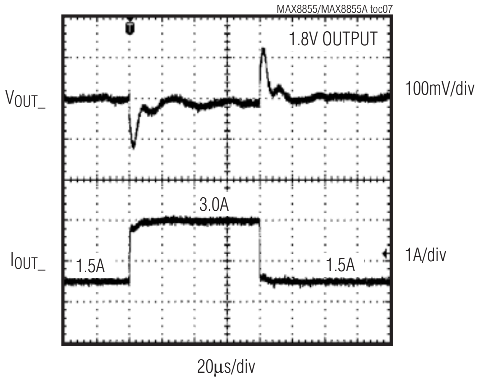
SWITCHING FREQUENCY vs. TEMPERATURE



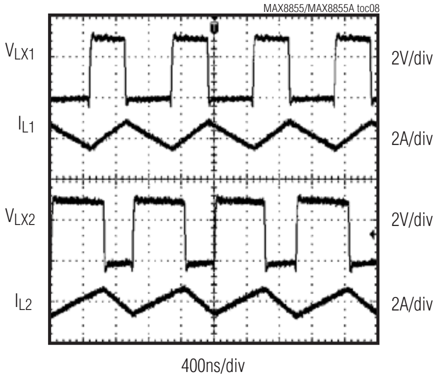
FEEDBACK VOLTAGE vs. TEMPERATURE



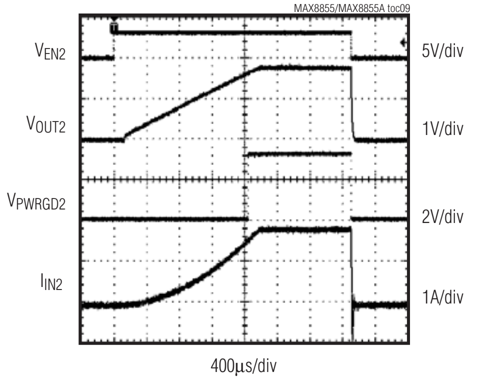
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



LOAD TRANSIENT



SWITCHING WAVEFORMS

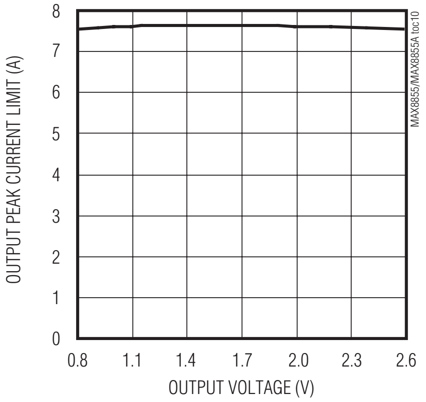


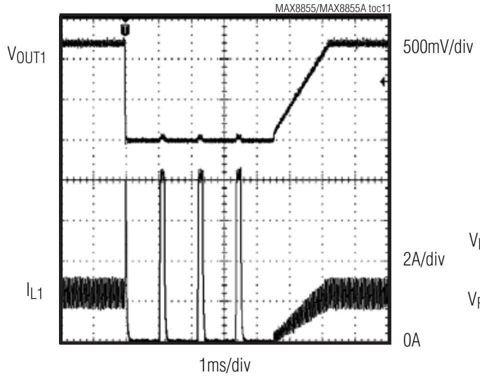
SOFT-START AND SHUTDOWN

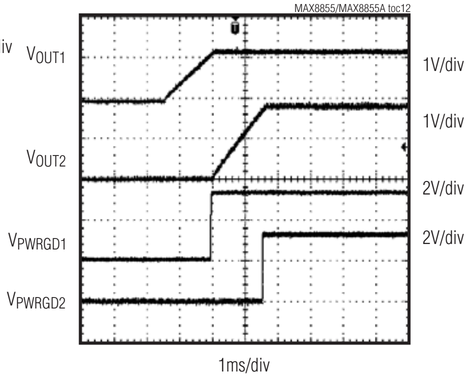
3A LOAD

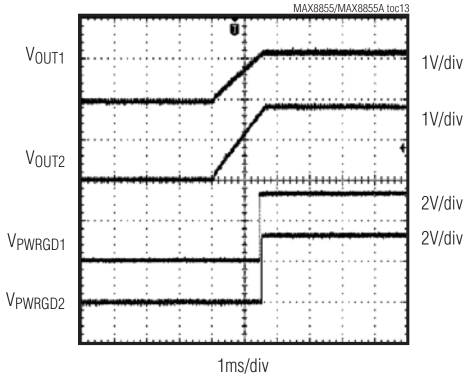
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = 3.3V, MAX8855/MAX8855A, circuit of Figure 6, T_A = +25°C, unless otherwise noted.)

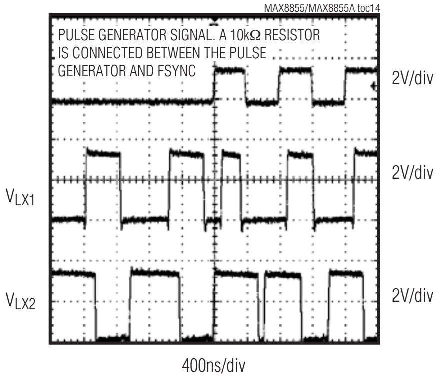

OUTPUT PEAK CURRENT LIMIT vs. OUTPUT VOLTAGE

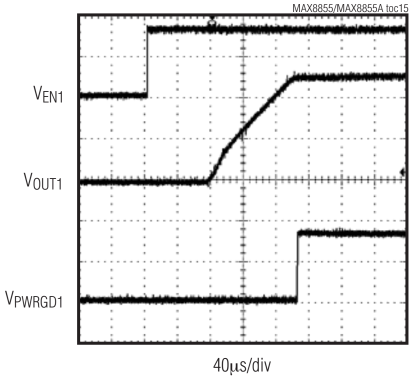

SHORT CIRCUIT AND RECOVERY


OUTPUT SEQUENCING (EN2 = PWRGD1)


OUTPUT TRACKING (EN1 = EN2)

DDR TRACKING 1.8V, 0.9V


EXTERNAL SYNCHRONIZATION


STARTING INTO PREBIASED OUTPUT

Pin Description

PIN	NAME	FUNCTION
1	PWRGD1	Power-Good Open-Drain Output for Regulator 1. PWRGD1 is high impedance when $V_{REFIN} \geq 0.54V$ and $V_{FB1} \geq 0.9 \times V_{REFIN}$. PWRGD1 is low when $V_{REFIN} < 0.54V$, EN1 is low, V_{DD} or IN1 is below UVLO, the thermal shutdown is activated, or when $V_{FB1} < 0.9 \times V_{REFIN}$.
2	REFIN	External Reference Input for Regulator 1. Connect an external reference to REFIN, or connect REFIN to SS1 to use the internal reference. REFIN is discharged to GND through 335Ω when EN1 is low or regulator 1 is shut down due to a fault condition.
3	V_{DD}	Supply Voltage. Connect a 10Ω resistor from V_{DD} to VDL and connect a 0.1µF capacitor from V_{DD} to GND.
4	GND	Analog Ground. Connect GND to the analog ground plane. Connect the analog and power ground planes together at a single point near the IC.
5	N.C.	No Connection
6	VDL	Supply Voltage Input for Low-Side Gate Drive. Connect VDL to IN_ or the highest available supply voltage less than 3.6V. Connect a 1µF capacitor from VDL to the power ground plane.
7	FSYNC	Frequency Set and Synchronization. Connect a 4.75kΩ to 20.5kΩ resistor from FSYNC to GND to set the switching frequency or drive with a 250kHz to 2.5MHz clock signal to synchronize switching. $R_{FSYNC} = (T - 0.05µs) \times (10kΩ/0.95µs)$, where T is the oscillator period.
8	PWRGD2	Power-Good Open-Drain Output for Regulator 2. PWRGD2 is high impedance when $V_{SS2} \geq 0.54V$ and $V_{FB2} \geq 0.9 \times V_{SS2}$. PWRGD2 is low when $V_{SS2} < 0.54V$, EN2 is low, V_{DD} or IN2 is below UVLO, the thermal shutdown is activated, or when $V_{FB2} < 0.9 \times V_{SS2}$.
9	SS2	Soft-Start for Regulator 2. Connect a capacitor from SS2 to GND to set the soft-start time. See the *Setting the Soft-Start Time* section. SS2 is internally pulled low with 335Ω when EN2 is low or regulator 2 is in a fault condition.
10	FB2	Feedback Input for Regulator 2. Connect FB2 to the center of an external resistor-divider from the output to GND to set the output voltage from 0.6V to 90% of V_{IN2}. FB2 is high impedance when the IC is shut down.
11	COMP2	Compensation for Regulator 2. COMP2 is the output of the internal voltage-error amplifier. Connect external compensation network from COMP2 to FB2. See the *Compensation Design* section. COMP2 is internally pulled to GND when the output is shut down.
12	EN2	Enable Input for Regulator 2. Drive EN2 high to enable regulator 2, or drive low for shutdown. For always-on operation, connect EN2 to V_{DD}.
13, 14	IN2	Power-Supply Input for Regulator 2. The voltage range is 2.35V (MAX8855A) to 3.6V. Connect two 10µF and one 0.1µF ceramic capacitors from IN2 to PGND2.
15, 16, 17	PGND2	Power Ground for Regulator 2. Connect all PGND_ pins to the power ground plane. Connect the power ground and analog ground planes together at a single point near the IC.
18, 19	LX2	Inductor Connection for Regulator 2. Connect an inductor between LX2 and the regulator output. LX2 is high impedance when the IC is shut down.
20	BST2	Bootstrap Connection for Regulator 2. Connect a 0.1µF capacitor from BST2 to LX2. BST2 is the supply for the high-side gate drive. BST2 is charged from VDL with an internal pMOS switch. In shutdown, there is an internal diode junction from LX2 to BST2 and from VDL to BST2.
21	BST1	Bootstrap Connection for Regulator 1. Connect a 0.1µF capacitor from BST1 to LX1. BST1 is the supply for the high-side gate drive. BST1 is charged from VDL with an internal pMOS switch. In shutdown, there is an internal diode junction from LX1 to BST1 and from VDL to BST1.
22, 23	LX1	Inductor Connection for Regulator 1. Connect an inductor between LX1 and the regulator output. LX1 is high impedance when the IC is shut down.
24, 25, 26	PGND1	Power Ground for Regulator 1. Connect all PGND_ pins to the power ground plane. Connect the power ground and analog ground planes together at a single point near the IC.

Pin Description (continued)

PIN	NAME	FUNCTION
27, 28	IN1	Power-Supply Input for Regulator 1. The voltage range is 2.35V to 3.6V for the MAX8855. The voltage range is 2.30V to 3.6V for the MAX8855A. Connect two 10µF and one 0.1µF ceramic capacitors from IN1 to PGND1.
29	EN1	Enable Input for Regulator 1. Drive EN1 high to enable regulator 1, or low for shutdown. For always-on operation, connect EN1 to V_{DD}.
30	COMP1	Compensation for Regulator 1. COMP1 is the output of the internal voltage-error amplifier. Connect external compensation network from COMP1 to FB1. See the *Compensation Design* section. COMP1 is internally pulled to GND when the output is shut down.
31	FB1	Feedback Input for Regulator 1. Connect FB1 to the center of an external resistor-divider from the output to GND to set the output voltage from 0.6V to 90% of V_{IN1}. FB1 is high impedance when the IC is shut down.
32	SS1	Soft-Start for Regulator 1. Connect a capacitor from SS1 to GND to set the startup time. See the *Setting the Soft-Start Time* section. When E1 is disabled (pulled low), or regulator 1 is in shutdown mode due to a fault condition, SS1 is internally pulled low with 335Ω resistor.
—	EP	Exposed Pad. Connect the exposed pad to the power ground plane.

Detailed Description

PWM Controller

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the control logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. It also contains the break-before-make logic and the timing for charging the bootstrap capacitors. The error signal from the voltage-error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator and, thus, the required PWM signal is produced. The high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the $V_{COMP\_}$ signal or the current-limit threshold is exceeded. The low-side switch is then turned on for the remainder of the oscillator cycle. The two switching regulators operate at the same switching frequency with 180° phase shift to reduce the input-capacitor ripple current requirement. Figure 1 shows the MAX8855/MAX8855A functional diagram.

Current Limit

The MAX8855/MAX8855A provide both peak and valley current limits to achieve robust short-circuit protection. During the high-side MOSFET's on-time, if the drain-source current reaches the peak current-limit threshold (specified in the *Electrical Characteristics* table), the high-side MOSFET turns off and the low-side MOSFET turns on, allowing the current to ramp down. At the next clock, the high-side MOSFET is turned on only if the inductor current is below the valley current limit. Otherwise, the PWM cycle is skipped to continue ramping down the inductor current. When the inductor current stays above the valley current limit for 12µs and the FB_ is below 0.7 x V_{REFIN}, the regulator enters hiccup mode. During hiccup mode, the SS_ capacitor is discharged to zero and the soft-start sequence begins after a predetermined time period.

Undervoltage Lockout (UVLO)

When the V_{DD} supply voltage drops below the falling undervoltage threshold (typically 1.9V), the MAX8855/MAX8855A enter the undervoltage lockout mode (UVLO). UVLO forces the devices to a dormant state until the input voltage is high enough to allow the device to function reliably. In UVLO, LX_ nodes of both regulators are in the high-impedance state. PWRGD1 and PWRGD2 are forced low in UVLO. When V_{VDD} rises above the rising undervoltage threshold (typically 2V), the IC powers up normally as described in the *Startup and Sequencing* section.

The UVLO circuitry also monitors the IN1 and IN2 supplies. When the IN_ voltage drops below the falling undervoltage threshold (typically 1.9V), the corresponding regulator shuts down, and corresponding PWRGD_ goes low. The regulator powers up when $V_{IN\_}$ rises above the rising undervoltage threshold (typically 2V).

Power-Good Output (PWRGD_)

PWRGD1 and PWRGD2 are open-drain outputs that indicate when the corresponding output is in regulation.

PWRGD1 is high impedance when $V_{REFIN} \geq 0.54V$ and $V_{FB1} \geq 0.9 \times V_{REFIN}$. PWRGD1 is low when $V_{REFIN} < 0.54V$, EN1 is low, V_{VDD} or V_{IN1} is below V_{UVLO}, the thermal-overload protection is activated, or when $V_{FB1} < 0.9 \times V_{REFIN}$.

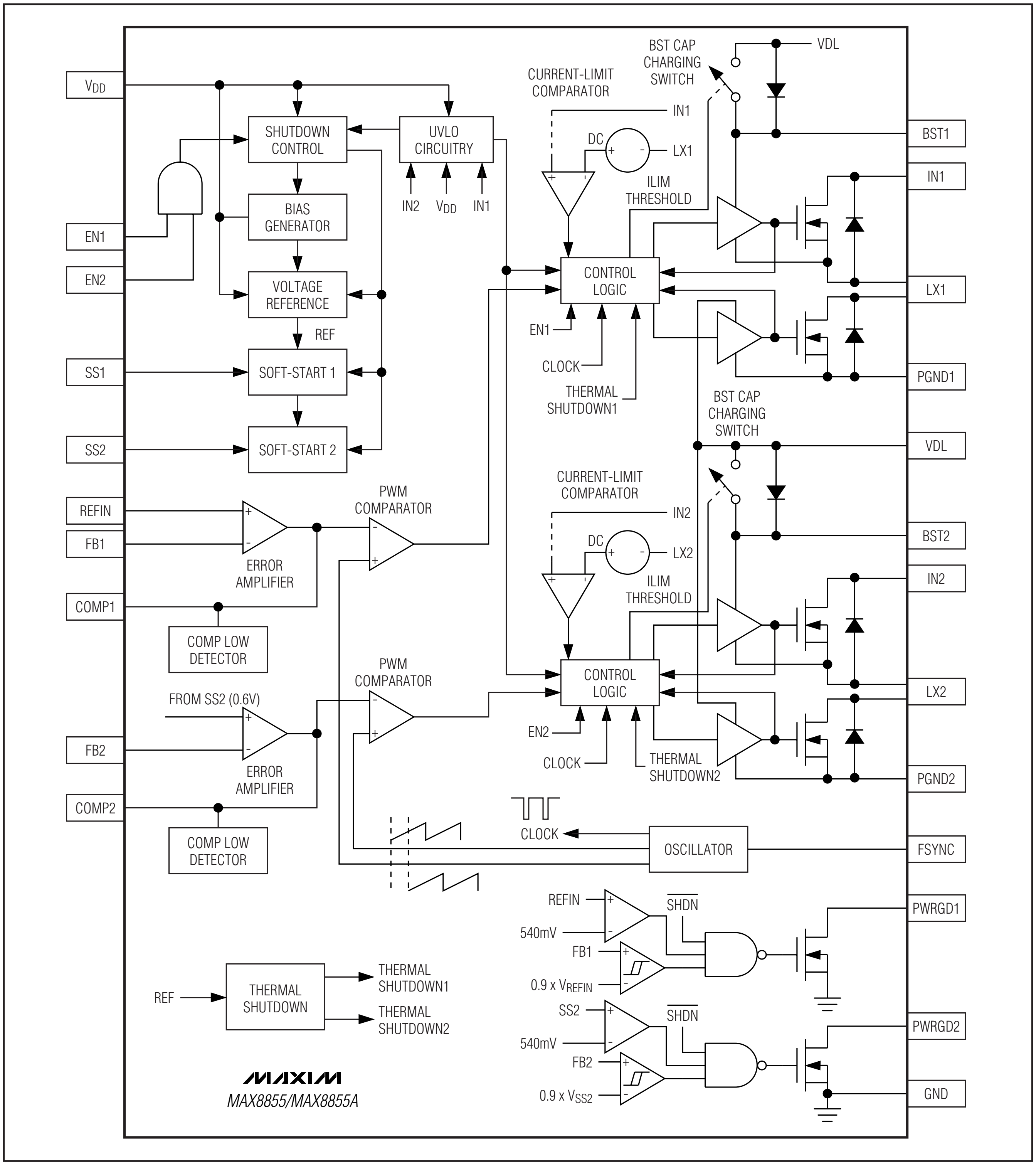


Figure 1. Functional Diagram

The power-good, open-drain output for regulator 2 (PWRGD2) is high impedance when $V_{SS2} \geq 0.54V$ and $V_{FB2} \geq 0.9 \times V_{SS2}$. PWRGD2 is low when $V_{SS2} < 0.54V$, EN2 is low, V_{VDD} or V_{IN2} is below V_{UVLO}, the thermal-overload protection is activated, or when $V_{FB2} < 0.9 \times V_{SS2}$.

External Reference Input (REFIN)

The MAX8855/MAX8855A have an external reference input. Connect an external reference between 0 and V_{VDD} - 1.6V to REFIN to set the FB1 regulation voltage. To use the internal 0.6V reference, connect REFIN to SS1. When the IC is shut down, REFIN is pulled to GND through 335Ω.

Startup and Sequencing

The MAX8855/MAX8855A feature separate enable inputs (EN1 and EN2) for the two regulators. Driving EN_ high enables the corresponding regulator; driving EN_ low turns the regulator off. Driving both EN1 and EN2 low puts the IC in low-power shutdown mode, reducing the supply current typically to 30nA. The MAX8855/MAX8855A regulators power up when the following conditions are met (see Figure 2):

- EN_ is logic-high.
- V_{VDD} is above the UVLO threshold.
- $V_{IN\_}$ is above the UVLO threshold.
- The internal reference is powered.
- The IC is not in thermal overload ($T_J < +165°C$).

Once these conditions are met, the MAX8855/MAX8855A begin soft-start. FB2 regulates to the voltage at SS2. During soft-start, the SS2 capacitor is charged with a constant 8µA current source so that its voltage ramps up for the soft-start time. See the *Setting the Soft-Start Time* section to select the SS2 capacitor for the desired soft-start time. FB1 regulates to the voltage at REFIN. Connect REFIN to SS1 to use the internal

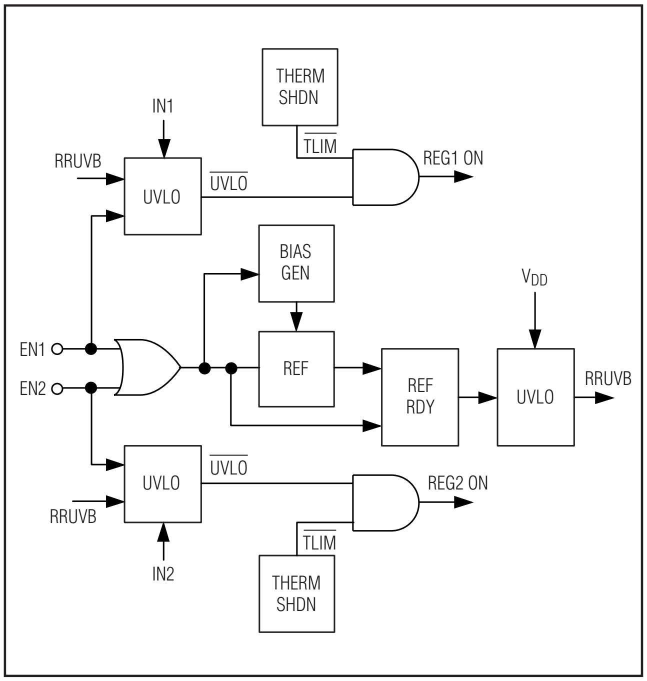


Figure 2. Startup Control Diagram

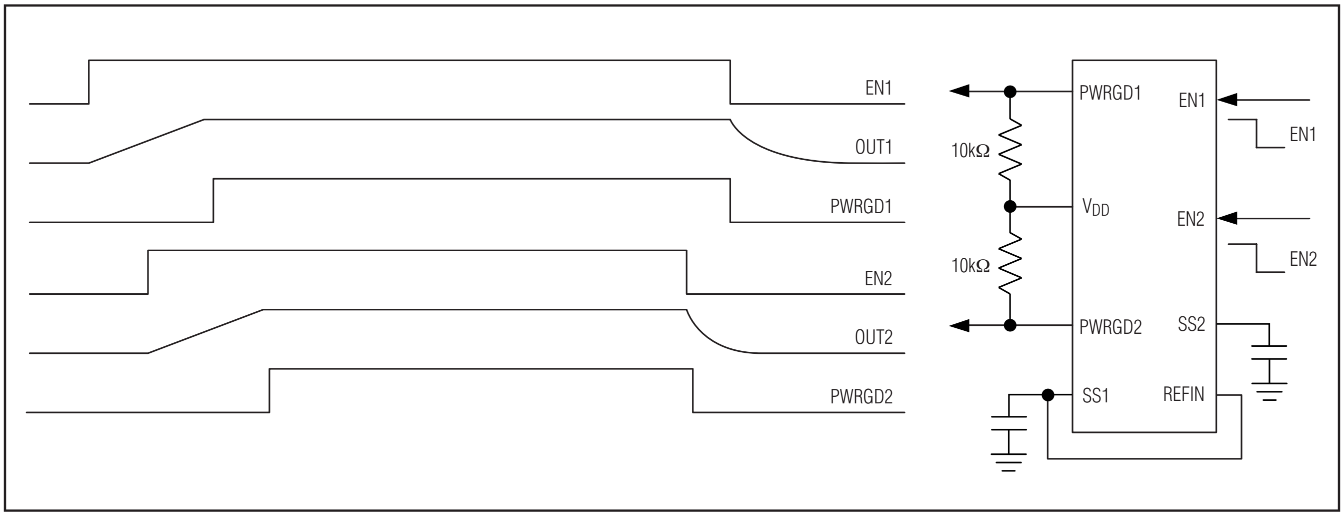


Figure 3a. Startup and Sequencing Options—Two Independent Output Startup and Shutdown Waveforms

reference with soft-start time set independently by the SS1 capacitor (see Figure 3a).

For ratiometric tracking applications, connect REFIN to the center of a voltage-divider from the output of regulator 2 to GND (see Figure 3b). In this application, the EN_ inputs are connected to each other and driven as a single enable input. Regulator 2 starts up with a normal soft-start (C_{SS2} sets the time), and regulator 1 output ratiometrically tracks the regulator 2 output voltage. The voltage-divider resistors set the V_{OUT1}/V_{OUT2} ratio (see the *Setting the Output Voltage* section). In Figure 3b, V_{OUT1} regulates to half of V_{OUT2}. Note that a capacitance of 1000pF should be connected to SS1 for stability.

Figure 3c shows the output sequencing application using an external reference.

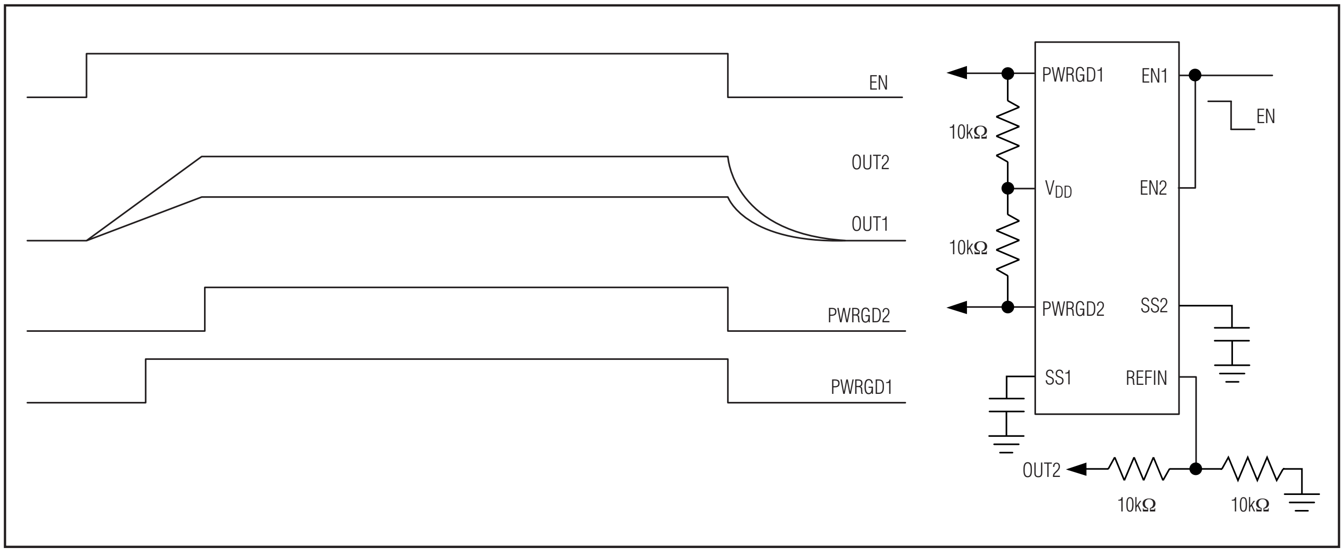


Figure 3b. Startup and Sequencing Options—Ratiometric Tracking Startup and Shutdown Waveforms V_{OUT1} Track V_{OUT2}

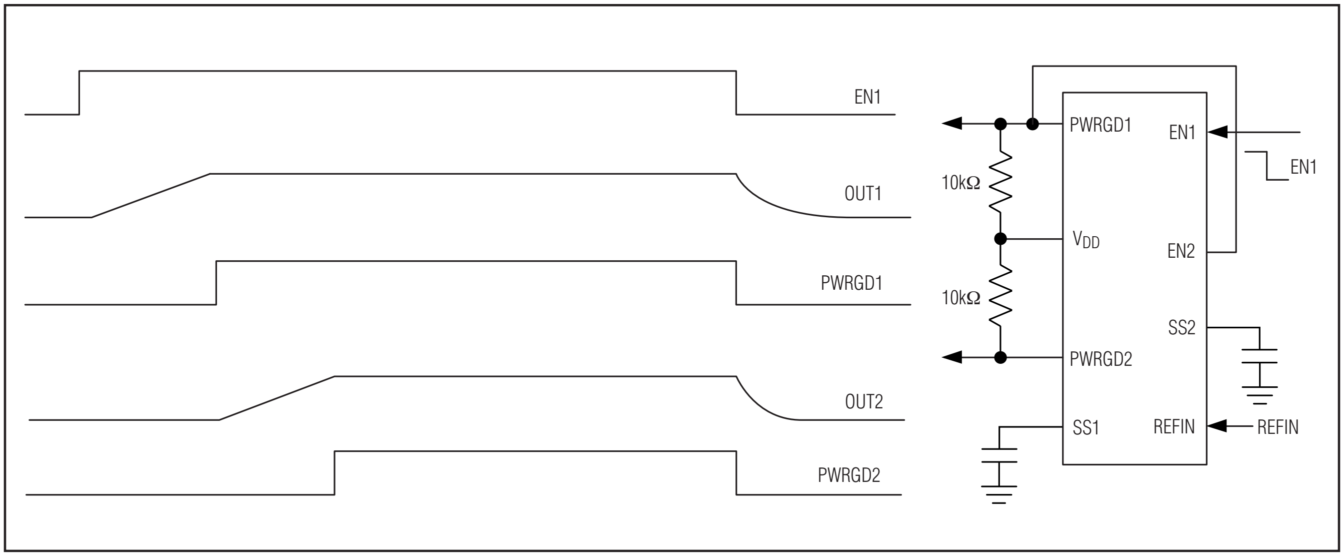


Figure 3c. Startup and Sequencing Options—Sequencing Startup and Shutdown Waveforms with External Reference

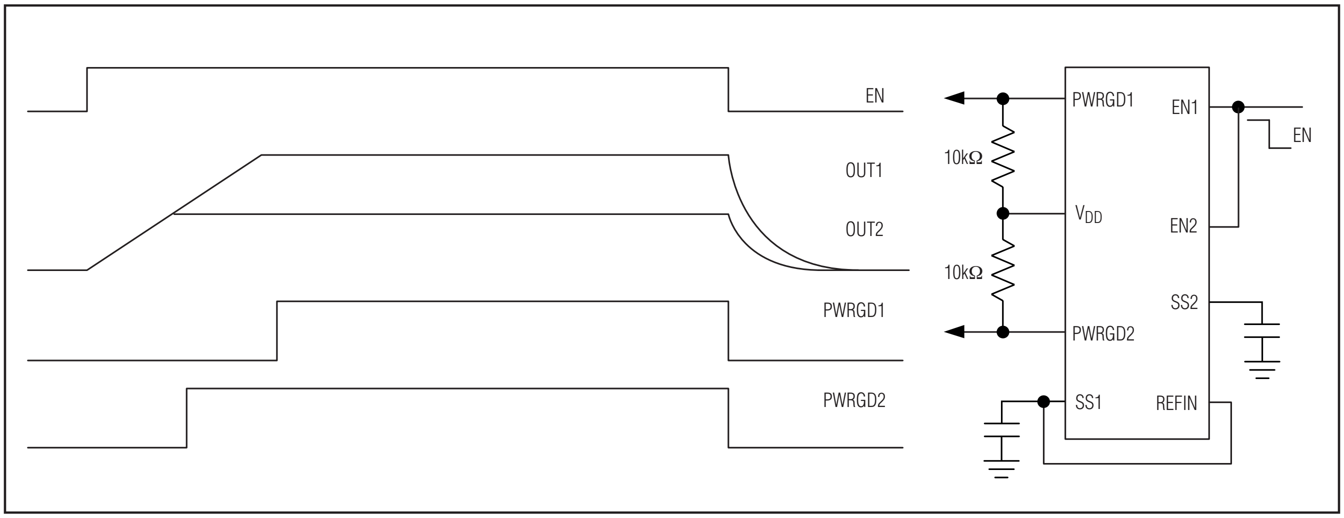


Figure 3d. Startup and Sequencing Options—Matching Startup Slopes of Output Voltages with Internal Reference

Sequencing is achieved by connecting EN2 to PWRGD1. In this mode, regulator 2 starts once regulator 1 reaches regulation.

In Figure 3d, EN1 and EN2 are connected together and driven as a single input. Although both outputs begin ramping up at the same time, slope matching is achieved by selecting the SS_ capacitors. See the *Setting the Soft-Start Time* section for information on selecting the SS_ capacitors. In Figure 3d, the slope of the output voltages during soft-start is equal. This is achieved by setting the ratio of the soft-start capacitors equal to the ratio of the output voltages:

$$\frac{C_{SS1}}{C_{SS2}} = \frac{V_{OUT1}}{V_{OUT2}}$$

Synchronization (FSYNC)

The MAX8855/MAX8855A operate from 500kHz to 2MHz using either its internal oscillator, or an externally supplied clock. See the *Setting the Switching Frequency* section.

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation of the MAX8855/MAX8855A. Internal thermal sensors monitor the junction temperature at each of the regulators. When the junction temperature exceeds +165°C, the corresponding regulator is shut down, allowing the IC to cool. The thermal sensor turns the regulator on after the junction temperature cools by +20°C. In a continuous thermal-overload condition, this results in a pulsed output.

Design Procedure

Setting the Output Voltage

The output voltages for regulator 1 (with REFIN connected to SS1) and regulator 2 are set with a resistor voltage-divider connected from the output to FB_ to GND as shown in Figure 4. Select a value for the resistor connected from output to FB_ (R4 in Figure 4) between 2kΩ and 10kΩ. Use the following equations to find the value for the resistor connected from FB_ to GND (R6 in Figure 4):

$$R6 = \frac{0.6}{\left(V_{OUT\_} - 0.6\right)} \times R4$$

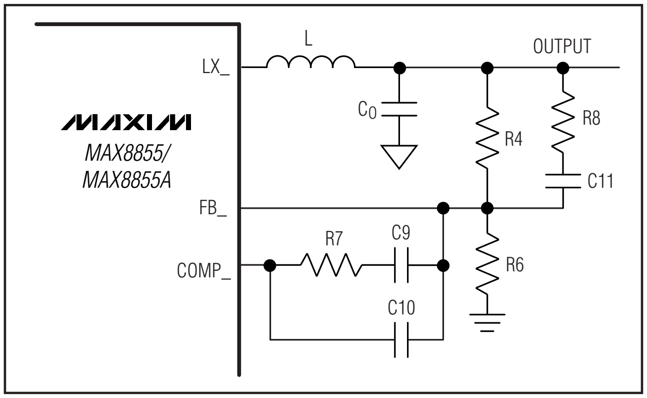


Figure 4. Type III Compensation Network

In DDR tracking applications such as Figure 7, the FB1 regulation voltage tracks the voltage at REFIN. In Figure 7, the output of regulator 1 tracks V_{OUT2}, and the ratio of the output voltages is set as follows:

$$\frac{V_{OUT1}}{V_{OUT2}} = \frac{R19}{R1 + R19}$$

Setting the Switching Frequency

The MAX8855/MAX8855A have an adjustable internal oscillator that can be set to any frequency from 500kHz to 2MHz. To set the switching frequency, connect a resistor from FSYNC to GND. Calculate the resistor value from the following equation:

$$R_{FSYNC} = \left(\frac{1}{f_S} - 50ns\right)\left(\frac{10k\Omega}{950ns}\right)$$

The MAX8855/MAX8855A can also be synchronized to an external clock from 500kHz to 2MHz by connecting the clock signal to FSYNC through a 10kΩ isolation resistor. The external sync frequency must be higher than the frequency that would be produced by R_{FSYNC}. The two regulators switch at the same frequency as the FSYNC clock, and are 180° out-of-phase with each other. The external clock duty cycle may range between 10% and 90% to ensure 180° out-of-phase operation.

Setting the Soft-Start Time

The two step-down regulators have independent adjustable soft-start. Capacitors from SS_ to GND are charged from a constant 8μA (typ) current source to the feedback-regulation voltage. The value of the soft-start capacitors is calculated from the desired soft-start time as follows:

$$C_{SS\_} = t_{SS} \times \left(\frac{8\mu A}{0.6V}\right)$$

Inductor Selection

There are several parameters that must be examined when determining which inductor to use: maximum input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of inductor current ripple to DC load current. A higher LIR value allows for a smaller inductor, but results in higher losses and higher output ripple. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. A good compromise between size and efficiency is a 30% LIR. For applications in which size and transient response are important, an LIR of around 40% to 50% is recommended. Once all the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where f_S is the switching frequency. Choose a standard value close to the calculated value. The exact inductor value is not critical and can be adjusted to make tradeoffs among size, cost, and efficiency. Find a low-loss inductor with the lowest possible DC resistance that fits the allotted dimensions. The peak inductor current is determined as:

$$I_{PEAK} = \left(1 + \frac{LIR}{2}\right) \times I_{OUT(MAX)}$$

I_{PEAK} must not exceed the chosen inductor's saturation current rating or the minimum current-limit specification for the MAX8855/MAX8855A.

Input-Capacitor Selection

The input capacitor for each regulator serves to reduce the current peaks drawn from the input power supply and reduces switching noise in the IC. The total input capacitance for each rail must be equal to or greater than the value given by the following equation to keep the input-voltage ripple within specifications and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN\_MIN\_} = \frac{D\_ \times I_{OUT\_}}{f_{SW} \times V_{IN\_RIPPLE\_}}$$

where D_ is the quiescent duty cycle ($V_{OUT\_}/V_{IN\_}$); f_{SW} is the switching frequency; and $V_{IN\_RIPPLE\_}$ is the peak-to-peak input-ripple voltage, which should be less than 2% of the minimum DC input voltage.

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source but are instead shunted through the input capacitor. High source impedance requires high-input capacitance. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current, $I_{RIPPLE\_}$, is given by:

$$I_{RIPPLE\_} = I_{OUT\_} \times \sqrt{D\_ \times (1 - D\_)}$$

Output-Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output-voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

or:

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

whichever is greater.

It should be noted that the above ripple voltage components add vectrorially rather than algebraically, thus making V_{RIPPLE} a conservative estimate.

The peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a function of the inductor value, the output-voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages due to ESL negligible.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the *Compensation Design* and *Safe-Starting into a Prebiased Output* sections for more details.

Compensation Design

The power-stage transfer function consists of one double pole and one zero. The double pole is introduced by the output filtering inductor, L, and the output filtering capacitor, C_O. The ESR of the output filtering capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DC resistance and the internal switch resistance, $R_{DS(ON)}$. A typical value for $R_{DS(ON)}$ is 35mΩ. R_O is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total ESR of the output-filtering capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single-output capacitor divided by the total number of output capacitors.

The high-switching-frequency range of the MAX8855/MAX8855A allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer-function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output filtering inductor and capacitor. The double pole produces a gain drop of 40dB and a phase shift of 180° per decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. Therefore, use type III compensation as shown in Figure 4. Type III compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at 0Hz (DC). Locations of other poles and zeros of type III compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R7 \times C9}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R4 \times C11}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R7 \times C10}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R8 \times C11}$$

These equations are based on the assumptions that C9 >> C10, and R4 >> R8, which are true in most applications. Placement of these poles and zeros is determined by the frequencies of the double pole and ESR zero of the power stage transfer function. It is also a function of the desired closed-loop bandwidth. Figure 5 shows the pole zero cancellations in the type III compensation design.

The following section outlines the step-by-step design procedure to calculate the required compensation components. Begin by setting the desired output voltage as described in the *Setting the Output Voltage* section.

The crossover frequency f_C (or closed-loop, unity-gain bandwidth of the regulator) should be between 10% and 20% of the switching frequency, f_S. A higher crossover frequency results in a faster transient response. Too high of a crossover frequency can result in instability. Once f_C is chosen, calculate C9 (in farads) from the following equation:

$$C9 = \frac{2.5 \times V_{IN}}{2\pi \times f_C \times R4 \times \left(1 + \frac{R_L}{R_O}\right)}$$

where V_{IN} is the input voltage in volts, f_C is the crossover frequency in Hertz, R4 is the upper feedback resistor (in ohms), R_L is the sum of the inductor resistance and the internal switch on-resistance, and R_O is the output load resistance (V_{OUT}/I_{OUT}).

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the type III compensation less than the LC double-pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R7 = \frac{1}{0.8 \times C9} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C11 = \frac{1}{0.8 \times R4} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

Set the third compensation pole, f_{P3_EA}, at f_{Z_ESR}, which yields:

$$R8 = \frac{C_O \times ESR}{C11}$$

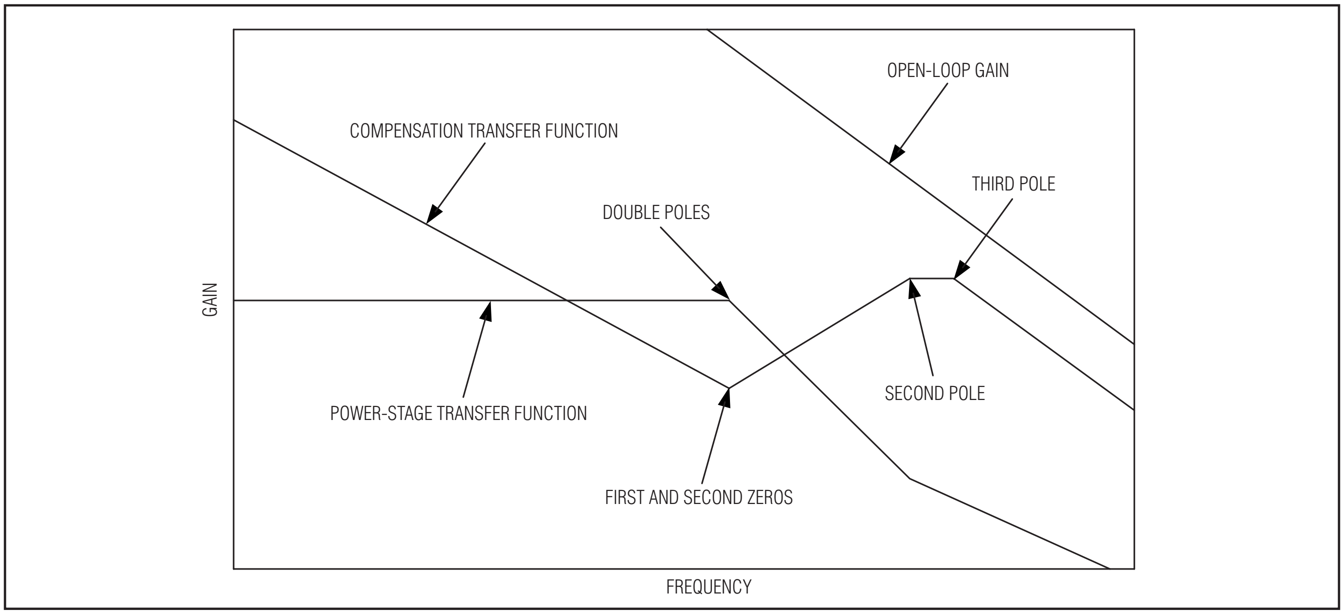


Figure 5. Pole Zero Cancellations in Compensation Design

Set the second compensation pole at 1/2 the switching frequency. Calculate C10 as follows:

$$C10 = \frac{1}{\pi \times R7 \times f_S}$$

The recommended range for R4 is 2kΩ to 10kΩ. Note that the loop compensation remains unchanged if only R6's resistance is altered to set different outputs.

Safe-Starting into a Prebiased Output

The MAX8855/MAX8855A are capable of safe-starting up into a prebiased output without discharging the output capacitor. This type of operation is also termed monotonic startup. However, in order to avoid output voltage glitches during safe-start it should be ensured that the inductor current is in continuous conduction mode during the end of the soft-start period, this is done by satisfying the following equation:

$$C_O \times \frac{V_O}{t_{SS}} \geq \frac{I_{P-P}}{2}$$

where C_O is the output capacitor, V_O is the output voltage, t_{SS} is the soft-start time set by the soft-start capacitor C_{SS}, and I_{P-P} is the peak inductor ripple current (as defined in the *Output-Capacitor Selection* section). Depending on the application, one of these parameters may drive the selection of the others. See Starting into Prebiased Output waveforms in the *Typical Operating Characteristics* section for an example selection of the above parameters.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. It is highly recommended to duplicate the MAX8855 EV kit layout for optimum performance. If deviation is necessary, follow these guidelines for a good PCB layout:

- A multilayer PCB is recommended. Use inner-layer ground (and power) planes to minimize noise coupling.
- Place the input ceramic decoupling capacitor directly across and as close as possible to IN_ and PGND_. This is to help contain the high switching currents within a small loop.
- Connect IN_ and PGND_ separately to large copper areas to help cool the IC and further improve efficiency and long-term reliability.
- Connect input, output, and VDL capacitors to the power ground plane (PGND_).
- Keep the path of switching currents short and minimize the loop area formed by LX_, the output capacitor(s), and the input capacitor(s).
- Place the IC decoupling capacitors as close as possible to the IC pins, connecting all other ground-terminated capacitors, resistors, and passive components to the reference or analog ground plane (GND).
- Separate the power and analog ground planes, using a single-point common connection point (typically, at the $C_{IN\_}$ cathode.
- Connect the exposed pad to the analog ground plane, allowing sufficient copper area to help cool the device. If the exposed pad is used as a common PGND_-to-GND connection point, avoid running high current through the exposed pad by using separate vias to connect the PGND_ pins to the power ground plane rather than connecting them to the exposed pad on the top layer.
- Use caution when routing feedback and compensation node traces; avoid routing near high dV/dt nodes (LX_) and high-current paths. Place the feedback and compensation components as close as possible to the IC pins.
- Reference the MAX8855 Evaluation Kit for an example layout.

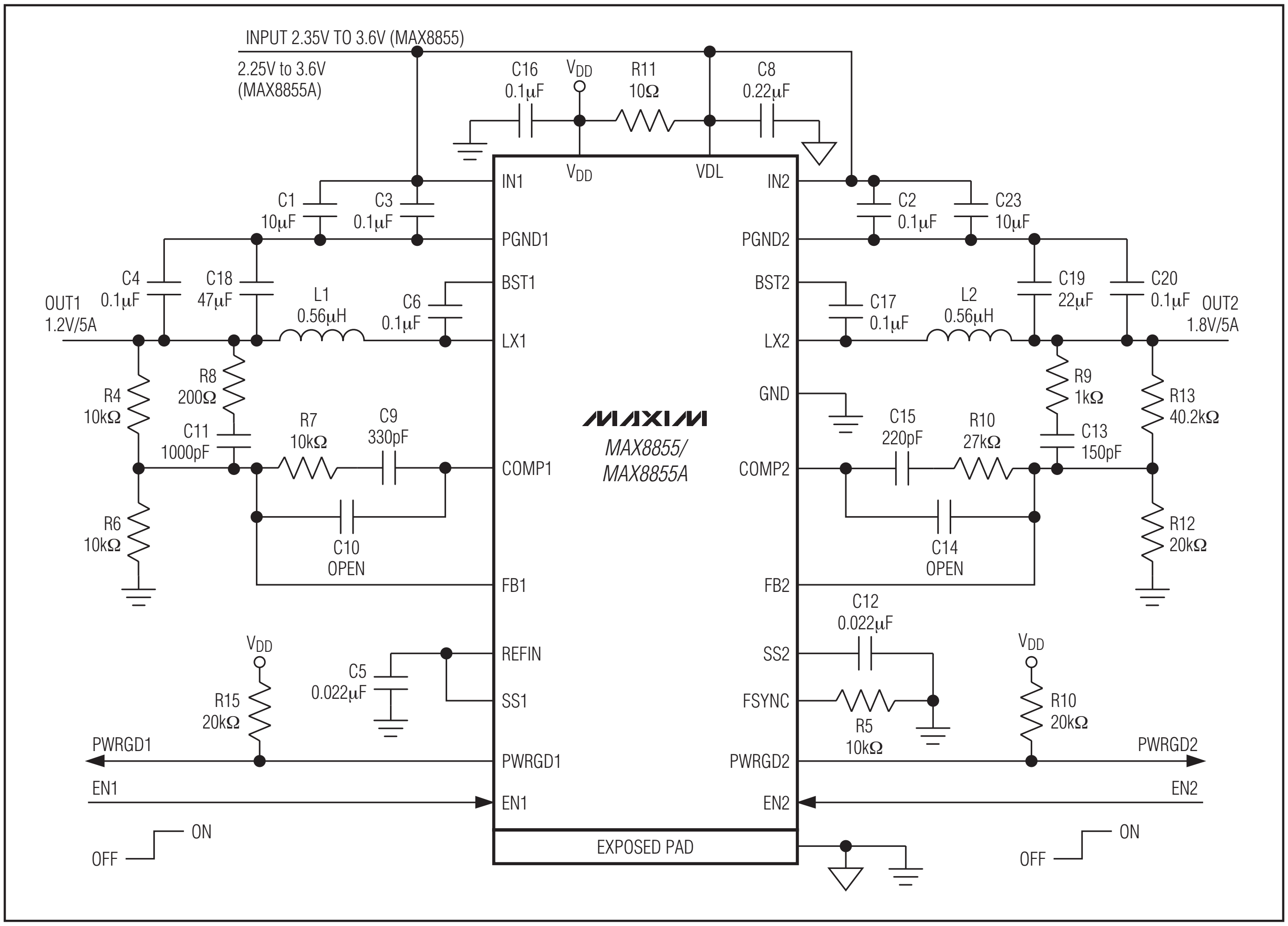


Figure 6. 1MHz Typical Application Circuit

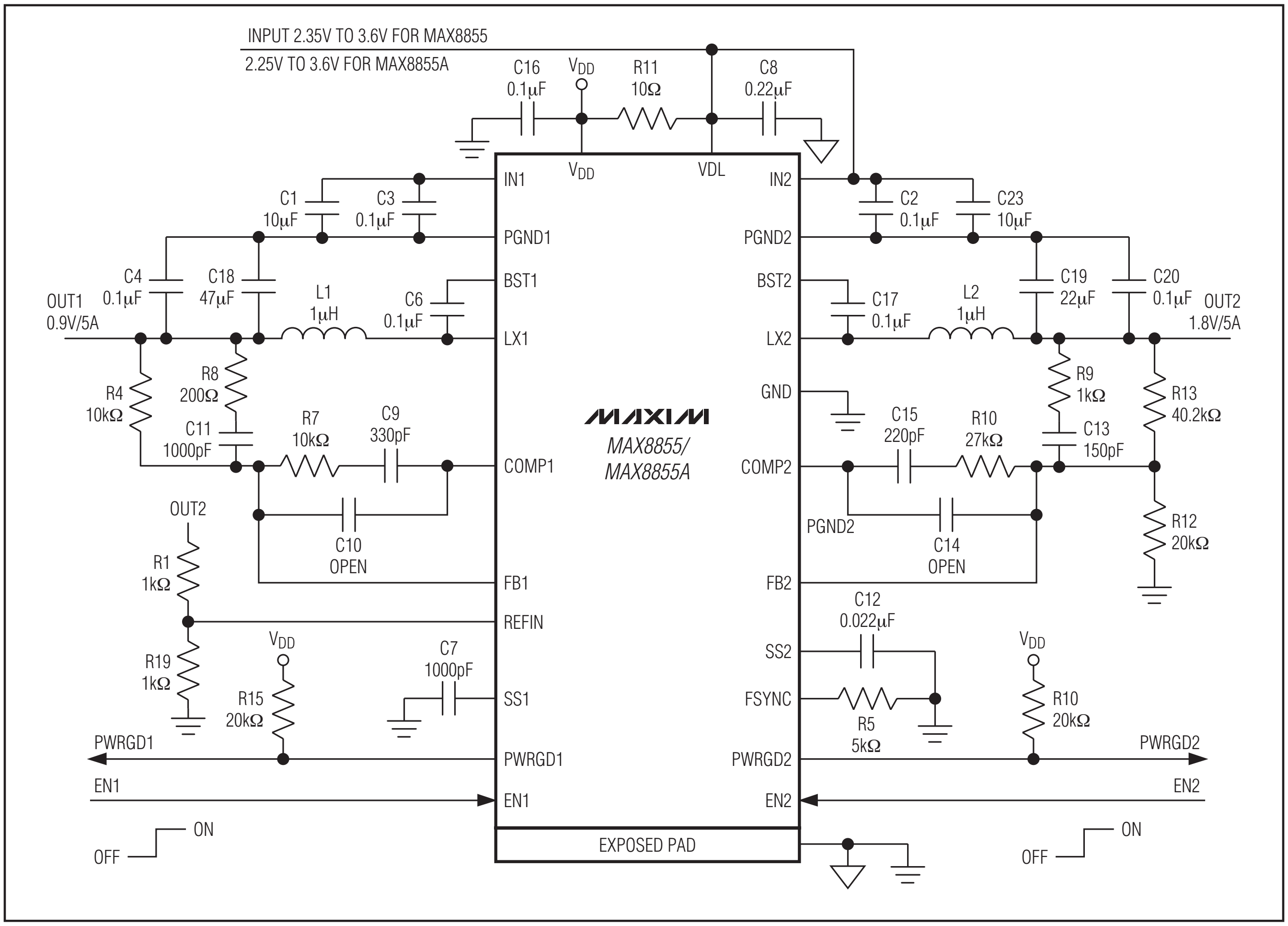
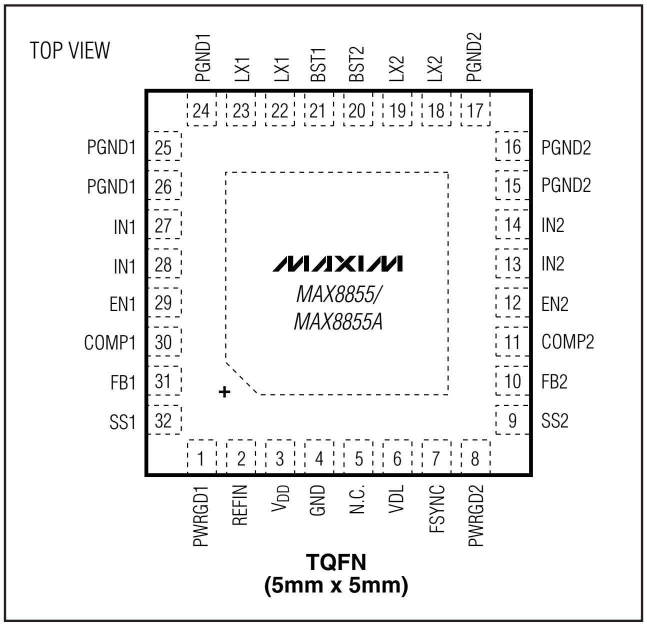


Figure 7. Tracking DDR Application Circuit

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255-4	**21-0140**	**90-0012**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/07	Initial release	—
1	6/08	Revised *Features* section and corrected Figure 6.	1, 17
2	4/09	Revised *Features*, *Typical Operating Characteristics*, and *Output-Capacitor Selection* sections. Added the *Safe-Starting into a Prebiased Output* section.	1, 6, 14, 16
3	7/11	Added the MAX8855A to the data sheet. Added soldering temperature and *Package Thermal Characteristics* to *Absolute Maximum Ratings*. Changed *Typical Operating Circuit*. Added new *Electrical Characteristics* Table. Changed input voltages in Figures 6 and 7.	1, 2, 3, 16
4	10/11	Updated the input voltage for the MAX8855A throughout the data sheet	1, 2, 3, 7, 16, 17, 18