Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND unless otherwise noted.)
V_{IN} to GND .....-0.3V to +30V
V_{CC} to GND .....-0.3V, lower of 6V or (VL + 0.3V)
FB to GND .....-0.3V to +6V
BST to GND .....-0.3V to +36V
VL, DL, COMP to GND .....-0.3V to (V_{CC} + 0.3V)
BST to LX .....-0.3V to +6V
DH to LX .....-0.3V to (V_{BST} + 0.3V)
VL Short to GND 5s
LX to GND .....-1V to +30V
Input Current (any pin) .....±50mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = VL = V_{CC} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Operating Range	V_{IN}	V_{CC} = VL, V_{IN} separate from V_{CC}	4.9		28.0	V
		V_{IN} = VL = V_{CC}	2.7		5.5	
V_{IN} Undervoltage Lockout (UVLO) Trip Level		Rising and falling edge, hysteresis = 2%	2.35	2.50	2.66	V
V_{IN} Operating Supply Current		V_{FB} = 0.88V (no switching)		0.7	1.2	mA
VL Output Voltage		5.5V < V_{IN} < 28V, V_{CC} = VL, 1mA < I_{LOAD} < 25mA	4.7	5	5.3	V
Thermal Shutdown		Rising temperature, typical hysteresis = 10°C (Note 1)		+160		°C
OSCILLATOR						
Frequency	f_{OSC}	MAX8545, MAX8546	250	300	360	kHz
		MAX8548	80	100	120	
Minimum Duty Cycle	DC_{MIN}	DH output, MAX8545, MAX8546			5	%
		MAX8548			10	
Maximum Duty Cycle	DC_{MAX}	DH output, MAX8545, MAX8546	83	86		%
		MAX8548	90	95		
SOFT-START						
Digital Ramp Period		MAX8545, MAX8546		6.6		ms
		MAX8548		10.2		
Soft-Start Levels		MAX8545, MAX8546		V_{OUT} / 64		V
		MAX8548		V_{OUT} / 32		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = VL = V_{CC} = 5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
FB Regulation Voltage		2.7V < V_{CC} < 5.5V, 0°C to +85°C	0.787	0.800	0.815	V
		2.7V < V_{CC} < 5.5V, -40°C to +85°C	0.782	0.800	0.815	
FB to COMP/EN Gain				4000		V/V
FB to COMP/EN Transconductance		-5µA < $I_{COMP/EN}$ < +5µA	70	108	160	µS
FB Input Bias Current		V_{FB} = 0.88V		1	2	µA
COMP/EN Source Current		$V_{COMP/EN}$ = 0V	15	46	100	µA
Current-Limit Threshold Voltage (Across Low-Side MOSFET)		LX to GND, MAX8545, MAX8548, V_{FB} = 0.8V	-355	-320	-280	mV
		LX to GND MAX8546, V_{FB} = 0.8V	-185	-165	-140	
Foldback Current-Limit Threshold Voltage (Across Low-Side MOSFET) When Output is Short		LX to GND, V_{FB} = 0V, MAX8545, MAX8548	-105	-75	-45	mV
		MAX8546, LX to GND, V_{FB} = 0	-53	-38	-22	
MOSFET DRIVERS						
Break-Before-Make Time		Rising edge, DH going low to DL going high		96		ns
		Falling edge, DL going low to DH going high		28		
DH On-Resistance in Low State				1.6	4	Ω
DH On-Resistance in High State				2.5	5.5	Ω
DL On-Resistance in Low State				1.1	2.5	Ω
DL On-Resistance in High State				2.5	5.5	Ω
BST Leakage Current		V_{BST} = 33V, V_{LX} = 28V, V_{FB} = 0.88V		0	50	µA
LX Leakage Current		V_{BST} = 33V, V_{LX} = 28V, V_{FB} = 0.88V		33	100	µA

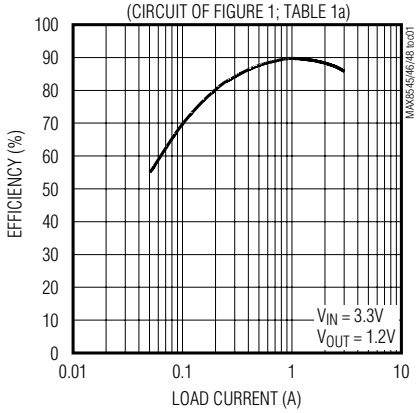
Note 1: Thermal shutdown disables the buck regulator when the die reaches this temperature. Soft-start is reset but the VL regulator remains on.

Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit

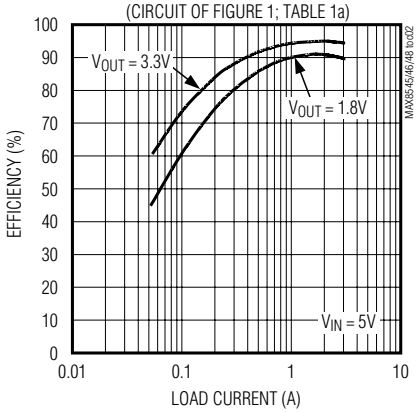
Typical Operating Characteristics

(V_{IN} = VL = V_{CC} = 5V, typical values are at T_A = +25°C, unless otherwise noted.)

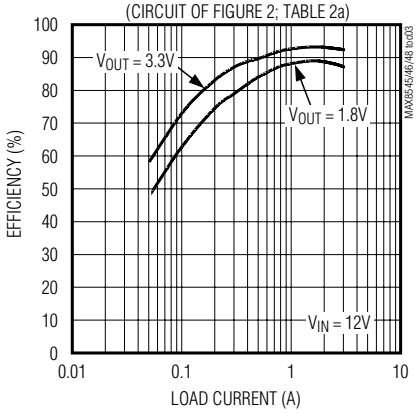
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 1; TABLE 1a)



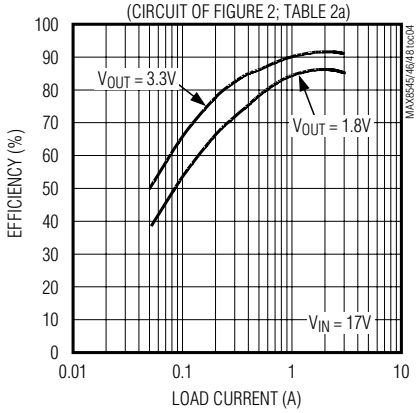
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 1; TABLE 1a)



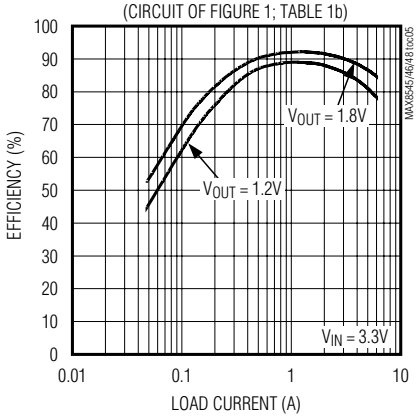
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 2; TABLE 2a)



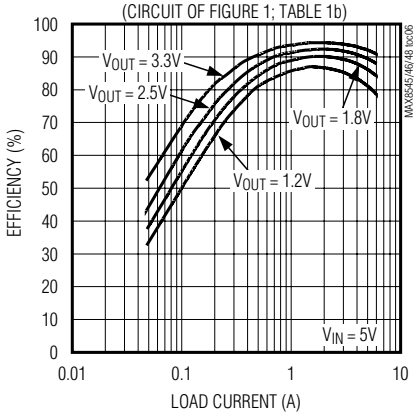
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 2; TABLE 2a)



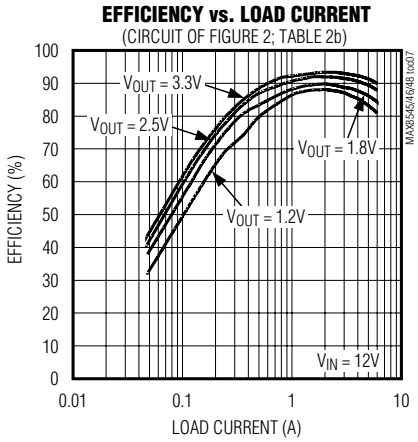
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 1; TABLE 1b)



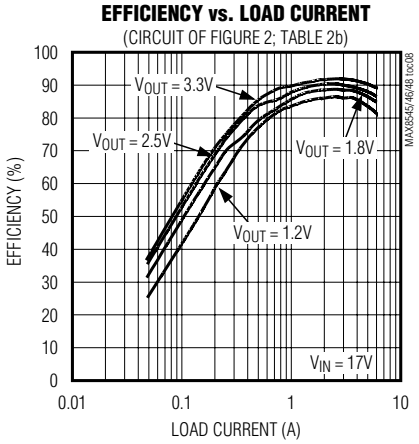
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 1; TABLE 1b)



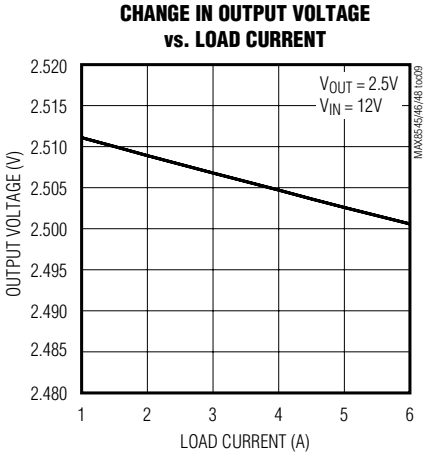
EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 2; TABLE 2b)



EFFICIENCY vs. LOAD CURRENT
(CIRCUIT OF FIGURE 2; TABLE 2b)



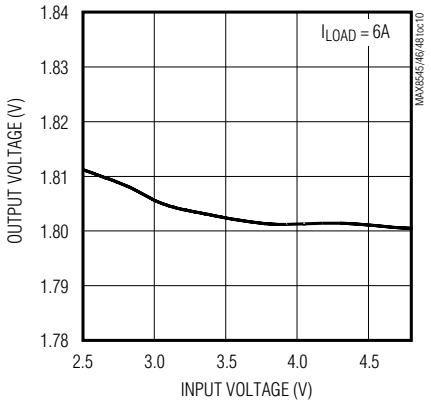
CHANGE IN OUTPUT VOLTAGE vs. LOAD CURRENT



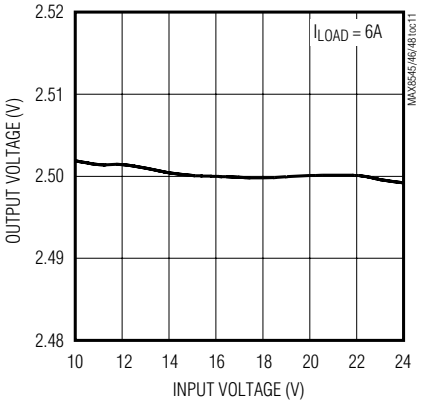
Typical Operating Characteristics (continued)

(V_{IN} = VL = V_{CC} = 5V, typical values are at T_A = +25°C, unless otherwise noted.)

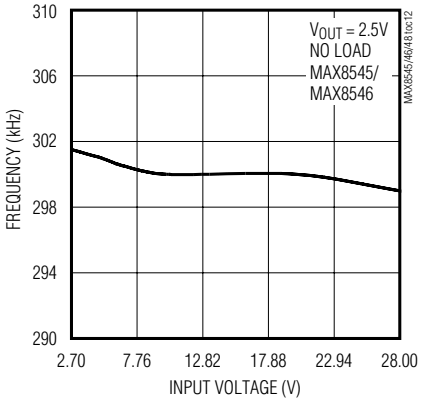
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE



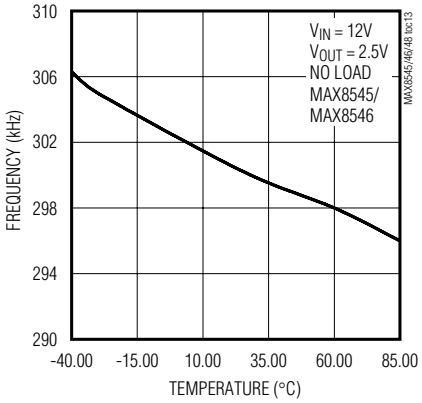
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE



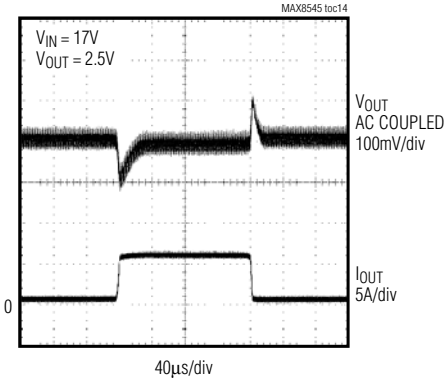
FREQUENCY vs. INPUT VOLTAGE



FREQUENCY vs. TEMPERATURE



LOAD TRANSIENT RESPONSE

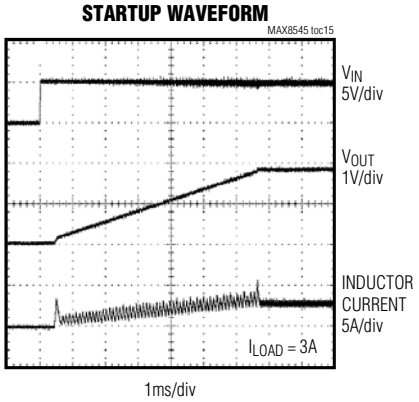


Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit

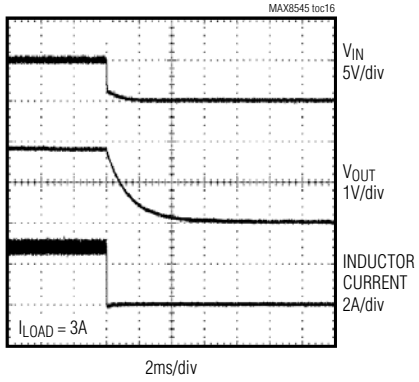
Typical Operating Characteristics (continued)

(V_{IN} = VL = V_{CC} = 5V, typical values are at T_A = +25°C, unless otherwise noted.)

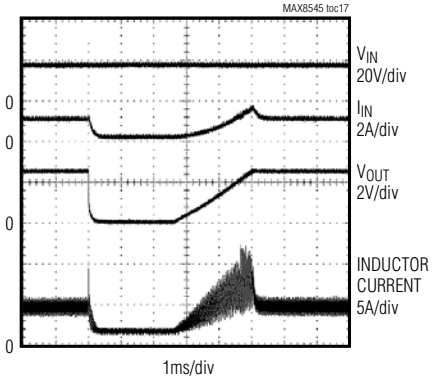
STARTUP WAVEFORM



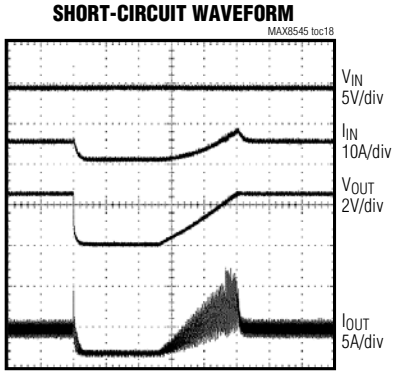
SHUTDOWN WAVEFORM



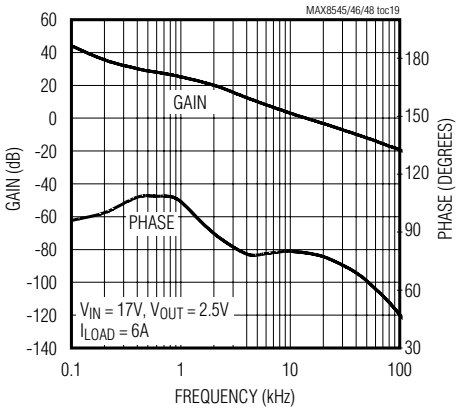
SHORT-CIRCUIT WAVEFORM



SHORT-CIRCUIT WAVEFORM



GAIN AND PHASE vs. FREQUENCY

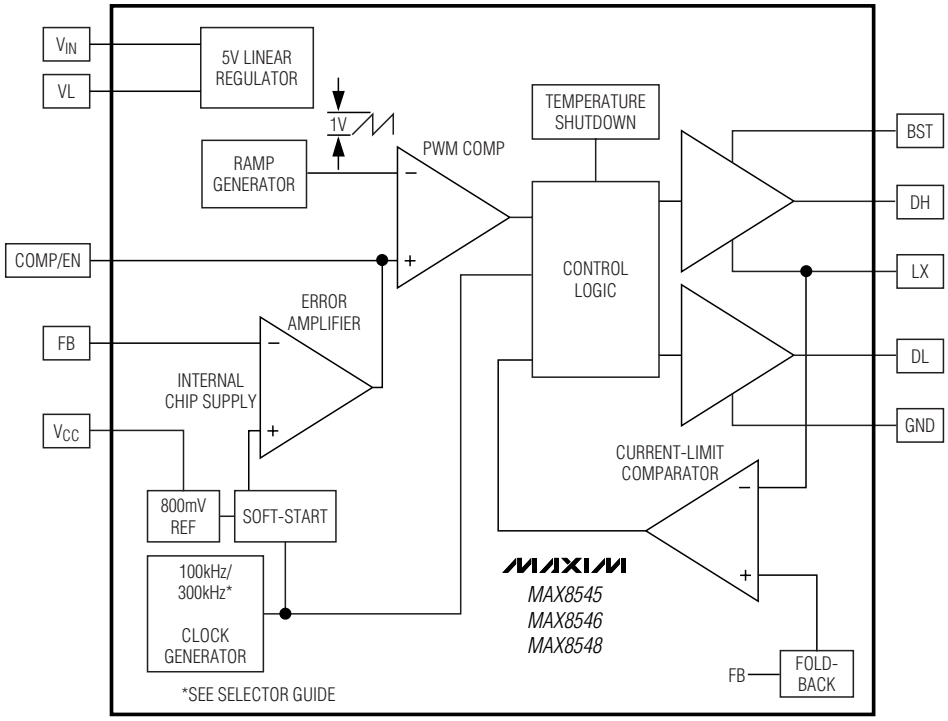


Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit

Pin Description

PIN	NAME	FUNCTION
1	COMP/EN	Compensation Input. Pull COMP/EN low with an open-collector or open-drain device to turn off the output.
2	FB	Feedback Input. Connect a resistive-divider network to set V_{OUT}. FB threshold is 0.8V.
3	V_{CC}	Internal Chip Supply. Connect V_{CC} to VL through a 10Ω resistor. Bypass V_{CC} to GND with at least a 0.1µF ceramic capacitor.
4	V_{IN}	Power Supply for LDO Regulator for V_{IN} > 5.5V, and Chip Supply for V_{IN} < 5.5V. Bypass V_{IN} with at least a 1µF ceramic capacitor to GND.
5	VL	Output of Internal 5V LDO. Connect VL to V_{IN} for V_{IN} < 5.5V. Bypass VL with at least a 1µF ceramic capacitor to GND.
6	DL	Low-Side External MOSFET Gate-Driver Output. DL swings from VL to GND.
7	GND	Ground and Negative Current-Sense Input
8	LX	Inductor Switching Node. LX is used for both current limit and the return supply of the DH driver.
9	DH	High-Side External MOSFET Gate-Driver Output. DH swings from BST to LX.
10	BST	Positive Supply of DH Driver. Connect a 0.1µF ceramic capacitor between BST and LX.

Functional Diagram



Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit

Detailed Description

The MAX8545/MAX8546/MAX8548 are BiCMOS switch-mode power-supply controllers designed to implement simple, buck-topology regulators in cost-sensitive applications. The main power-switching circuit consists of two n-channel MOSFETs, an inductor, and input/output filter capacitors. An all n-channel synchronous-rectified design provides high efficiency at reduced cost. These devices have an internal 5V linear regulator that steps down the input voltage to supply the IC and the gate drivers. The low-side-switch gate driver is directly powered from the 5V regulator (VL), while the high-side-switch gate driver is indirectly powered from VL plus an external diode-capacitor boost circuit.

Current-Limit and Short-Circuit Protection

The MAX8545/MAX8546/MAX8548 employ a valley current-sensing algorithm that uses the $R_{DS(ON)}$ of the low-side n-channel MOSFET to sense the current. This eliminates the need for an external sense resistor usually placed in series with the output. The voltage measured across the low-side MOSFET's $R_{DS(ON)}$ is compared to a fixed -320mV reference for the MAX8545/MAX8548 and a fixed -165mV reference for the MAX8546. The current limit is given by the equations below:

$$I_{LIMIT} = \frac{320mV}{R_{DS(ON)}} (MAX8545/MAX8548)$$

$$I_{LIMIT} = \frac{165mV}{R_{DS(ON)}} (MAX8546)$$

Aside from current limiting, these devices feature foldback short-circuit protection. This feature is designed to reduce the current limit by 80% as the output voltage drops to 0V.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving n-channel MOSFETs with low gate charge. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until the low-side MOSFET is fully off. There must be a low-resistance, low-inductance connection from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX8545/MAX8546/MAX8548 may detect the MOSFET gate as off while there is actually charge left on the gate. Use very short, wide traces measuring no less than 50mils to 100 mils wide if the MOSFET is 1in away from the MAX8545/MAX8546/MAX8548. The same type of adaptive dead-time circuit monitors the DH off edge. The same recommendations apply for the gate connection of the high-side MOSFET.

The internal pulldown transistor that drives DL low is robust, with a 1.1Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET during the fast rise time of the LX node.

Soft-Start

The MAX8545/MAX8546/MAX8548 feature an internally set soft-start function that limits inrush current. It accomplishes this by ramping the internal reference input to the controller's transconductance error amplifier from 0 to the 0.8V reference voltage. The ramp time is 1024 oscillator cycles for the MAX8548 and 2048 oscillator cycles for the MAX8545/MAX8546. At the nominal 100kHz and 300kHz switching rate, the soft-start ramp is approximately 10.2ms and 6.8ms, respectively.

High-Side Gate-Drive Supply (BST)

A flying-capacitor boost circuit generates gate-drive voltage for the high-side n-channel MOSFET. The flying capacitor is connected between the BST and LX nodes.

On startup, the synchronous rectifier (low-side MOSFET) forces LX to ground and charges the boost capacitor to VL. On the second half-cycle, the MAX8545/MAX8546/MAX8548 turn on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to drive the high-side MOSFET gate above its source at the input voltage.

Internal 5V Linear Regulator

All MAX8545/MAX8546/MAX8548 functions are internally powered from an on-chip, low-dropout 5V regulator (VL). These devices have a maximum input voltage (V_{IN}) of 28V. Connect V_{CC} to VL through a 10Ω resistor and bypass V_{CC} to GND with a 0.1µF ceramic capacitor. The V_{IN}-to-VL dropout voltage is typically 140mV, so when V_{IN} is less than 5.5V, VL is typically V_{IN} - 140mV.

The internal linear regulator can source a minimum of 25mA and a maximum of approximately 40mA to supply power to the IC low-side and high-side MOSFET drivers.

Duty-Cycle Limitations for Low V_{OUT}/V_{IN} Ratios

The MAX8545/MAX8546/MAX8548s' output voltage is adjustable down to 0.8V. However, the minimum duty cycle can limit the ability to supply low-voltage outputs

from high-voltage inputs. With high input voltages, the required duty factor is approximately:

$$\frac{V_{OUT} + (R_{DS(ON)} \times I_{LOAD})}{V_{IN}}$$

where $R_{DS(ON)} \times I_{LOAD}$ is the voltage drop across the synchronous rectifier. Therefore, the maximum input voltage ($V_{IN(DFMAX)}$) that can supply a given output voltage is:

$$V_{IN(DFMAX)} \le \frac{1}{DC_{MIN}}\left(V_{OUT} + \left(R_{DS(ON)} \times I_{LOAD}\right)\right)$$

If the circuit cannot attain the required duty cycle dictated by the input and output voltages, the output voltage still remains in regulation. However, there may be intermittent or continuous half-frequency operation as the controller attempts to lower the average duty cycle by deleting pulses. This can increase output voltage ripple and inductor current ripple, which increases noise and reduces efficiency. Furthermore, circuit stability is not guaranteed.

Applications Information

Design Procedures

1) **Input Voltage Range**. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high input voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and switches are considered. In general, lower input voltages provide the best efficiency.
2) **Maximum Load Current**. There are two current values to consider. Peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and is key in determining output capacitor requirements. $I_{LOAD(MAX)}$ also determines the required inductor saturation rating. Continuous load current (I_{LOAD}) determines the thermal stresses, input capacitor, and MOSFETs, as well as the RMS ratings of other heat-contributing components such as the inductor.
3) **Inductor Value**. This choice provides tradeoffs between size, transient response, and efficiency. Higher inductance value results in lower inductor ripple current, lower peak current, lower switching losses, and, therefore, higher efficiency at the cost of slower transient response and larger size. Lower inductance values result in large ripple currents, smaller size, and poor efficiency, while also providing faster transient response.

Setting the Output Voltage

An output voltage between 0.8V and (0.83 x V_{IN}) can be configured by connecting FB to a resistive divider between the output and GND (see Figures 1 and 2). Select resistor R4 in the 1kΩ to 10kΩ range. R3 is then given by:

$$R_3 = R_4\left[\frac{V_{OUT}}{V_{FB}} - 1\right]$$

where V_{FB} = +0.8V.

Inductor Selection

Determine an appropriate inductor value with the following equation:

$$L = V_{OUT} \times \frac{(V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of inductor ripple current to average continuous maximum load current. Choosing LIR between 20% to 40% results in a good compromise between efficiency and economy. Choose a low-core-loss inductor with the lowest possible DC resistance. Ferrite-core-type inductors are often the best choice for performance; however, the MAX8548's low switching frequency also allows the use of powdered iron core inductors in ultra-low-cost applications where efficiency is not critical. With any core material, the core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

Setting the Current Limit

The MAX8545/MAX8546/MAX8548 provide valley current limit by sensing the voltage across the external low-side MOSFET. The minimum current-limit threshold voltage is -280mV for the MAX8545/MAX8548 and -140mV for the MAX8546. The MOSFET on-resistance required to allow a given peak inductor current is:

$$R_{DS(ON)MAX} \le \frac{0.28V}{I_{VALLEY}} \text{ (for the MAX8545/MAX8548)}$$

$$R_{DS(ON)MAX} \le \frac{0.14V}{I_{VALLEY}} \text{ (for the MAX8546)}$$

where $I_{VALLEY} = I_{LOAD(MAX)} \times (1 - LIR / 2)$, and $R_{DS(ON)MAX}$ is the maximum on-resistance of the low-side MOSFET at the maximum operating junction temperature.

Low-Cost, Wide Input Range, Step-Down Controllers with Foldback Current Limit

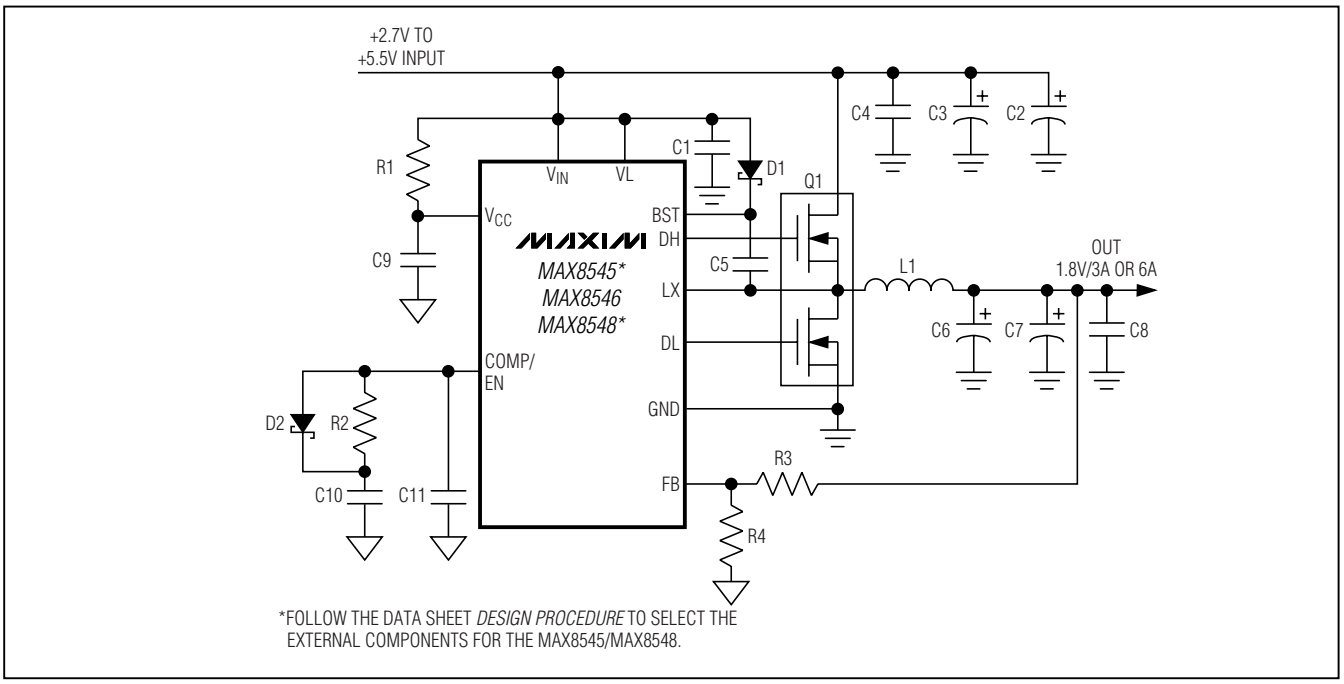


Figure 1. Typical Application Circuit (2.7V to 5V) Input (see Tables 1a, 1b)

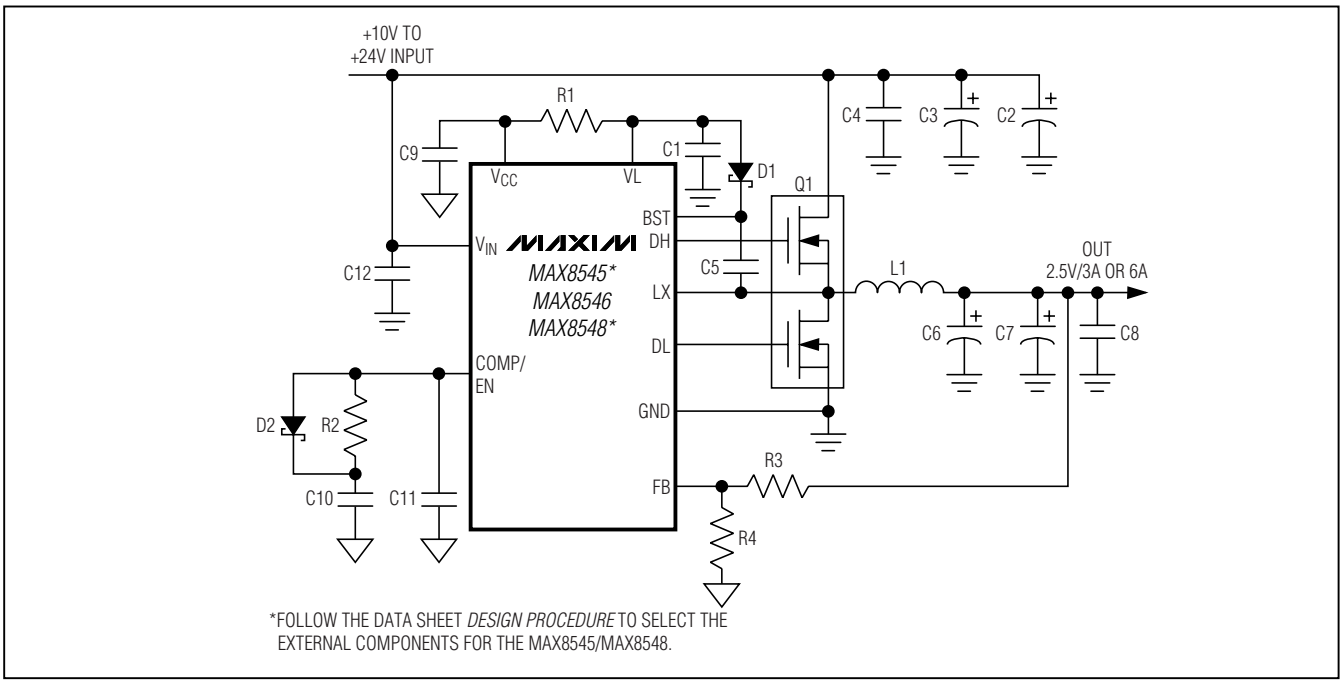


Figure 2. Typical Application Circuit (10V to 24V) Input (see Tables 2a, 2b)

A limitation of sensing current across a MOSFET's on-resistance is that the current-limit threshold is not accurate since MOSFET $R_{DS(ON)}$ specifications are not precise. This type of current limit provides a coarse level of fault protection. It is especially suited when the input source is already current-limited or otherwise protected.

Power MOSFET Selection

The MAX8545/MAX8546/MAX8548 drive two external, logic-level, n-channel MOSFETs as the circuit switching elements. The key selection parameters are:

1) On-resistance ($R_{DS(ON)}$): the lower, the better.
2) Maximum drain-to-source voltage (V_{DSS}) should be at least 10% higher than the input supply rail at the high-side MOSFET's drain.
3) Gate charges (Q_G, Q_{GD}, Q_{GS}): the lower, the better.

Choose the MOSFETs with rated $R_{DS(ON)}$ at V_{GS} = 4.5V for an input voltage greater than 5V, and at V_{GS} = 2.5V for an input voltage less than 5.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET (N1) that has conduction losses equal to the switching losses at nominal input voltage and maximum output current. For N2, make sure it does not spuriously turn on due to a dV/dt caused by N1 turning on as this would result in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{GD}/Q_{GS} ratio have higher immunity to dV/dt.

MOSFET Power Dissipation

For proper thermal-management design, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage (for the low-side MOSFET (N2) the worst case is at $V_{IN(MAX)}$, for the high-side MOSFET (N1) the worst case can be either at $V_{IN(MIN)}$ or $V_{IN(MAX)}$). N1 and N2 have different loss components due to the circuit operation. N2 operates as a zero-voltage switch; therefore, the major losses are: the channel conduction loss (P_{N2CC}), the body-diode conduction loss (P_{N2DC}), and the gate-drive loss (P_{N2DR}):

$$P_{N2CC} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times I^2_{LOAD} \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{N2DC} = 2 \times I_{LOAD} \times V_F \times t_{dt} \times f_S$$

where V_F is the body-diode forward voltage drop, t_{dt} is the dead time between N1 and N2 switching transitions (which is 30ns), and f_S is the switching frequency.

Because of zero-voltage switch operation, the N2 gate-drive losses are due to charging and discharging the input capacitor, C_{ISS}. These losses are distributed between the average DL gate driver's pullup and pull-down resistors and the internal gate resistance. The R_{DL} is typically 1.8Ω, and the internal gate resistance (R_{GATE}) of the MOSFET is typically 2Ω. The drive power dissipated in N2 is given by:

$$P_{N2DR} = C_{ISS} \times (V_{GS})^2 \times f_S \times \frac{R_{GATE}}{R_{GATE} + R_{DL}}$$

N1 operates as a duty-cycle control switch and has the following major losses: the channel conduction loss (P_{N1CC}), the voltage and current overlapping switching loss (P_{N1SW}), and the drive loss (P_{N1DR}). N1 does not have a body-diode conduction loss because the diode never conducts current:

$$P_{N1CC} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times (I_{LOAD})^2 \times R_{DS(ON)}$$

Use $R_{DS(ON)}$ at $T_{J(MAX)}$:

$$P_{N1SW} = V_{IN} \times I_{LOAD} \times f_S \times \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$$

where I_{GATE} is the average DH high driver output-current capability determined by:

$$I_{GATE(ON)} = \frac{1}{2} \times \frac{VL}{R_{DH} + R_{GATE}}$$

where R_{DH} is the high-side MOSFET driver's average on-resistance (2.05Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (2Ω typ):

$$P_{N1DR} = Q_{GS} \times V_{GS} \times f_S \times \frac{R_{GATE}}{R_{DH} + R_{GATE}}$$

where $V_{GS} \sim VL$.

In addition to the losses above, allow about 20% more for additional losses due to MOSFET output capacitance and N2 body-diode reverse recovery charge dissipated in N1. Refer to the MOSFET data sheet for thermal resistance specifications to calculate the PC board area needed. This information is essential to maintain the desired maximum operating junction temperature with the above calculated power dissipation.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side MOSFET drain to the low-side MOSFET source or add resistors in series

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with DH and DL to slow down the switching transitions. However, adding series resistors increases the power dissipation of the MOSFET, so ensure temperature ratings of the MOSFET are not exceeded.

Input-Capacitor Selection

The input capacitors (C2 and C3 in Figure 1) reduce noise injection and current peaks drawn from the input supply. The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RMS} = I_{LOAD} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}}}$$

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the RMS current. I_{RMS} is maximum when the input voltage equals 2 x V_{OUT}, where I_{RMS} = 1/2 I_{LOAD}.

Output Capacitor Selection

The key parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. All these parameters affect the overall stability, output ripple voltage, and transient response.

The output ripple has three components: variations in the charge stored in the output capacitor, the voltage drop across the ESR, and the voltage drop across the ESL.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)} + V_{RIPPLE(ESL)}$$

The output voltage ripple as a consequence of the ESR and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L + ESL}$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current (see the *Inductor Selection* section).

While these equations are suitable for initial capacitor selection to meet the ripple requirement, final values may also depend on the relationship between the LC double-pole frequency and the capacitor ESR-zero frequency. Generally, the ESR zero is higher than the LC double pole; however, it is preferable to keep the ESR zero close to the LC double pole when possible to negate the sharp phase shift of the typically high-Q double LC pole (see the *Compensation Design* section). Aluminum electrolytic or POS capacitors are recommended. Higher output current requires multiple capacitors to meet the output ripple voltage.

The MAX8545/MAX8546/MAX8548s' response to a load transient depends on the selected output capacitor. After a load transient, the output instantly changes by (ESR x ΔI_{LOAD}) + (ESL x dI/dt). Before the controller can respond, the output deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. Higher bandwidth results in faster response time, preventing the output voltage from further deviation. **Do not exceed the capacitor's voltage or ripple-current ratings**.

Boost Diode and Capacitor Selection

A low-current Schottky diode, such as the CMPSH-3 from Central Semiconductor, works well for most applications. Do not use large power diodes since higher junction capacitance can charge up BST to LX voltage that could exceed the device rating of 6V. The boost capacitor should be in the range of 0.1µF to 0.47µF, depending on the specific input and output voltages and the external components and PCB layout. The boost capacitance needs to be as large as possible to prevent it from charging to excessive voltage, but small enough to adequately charge during the minimum low-side MOSFET conduction time, which happens at the maximum operating duty cycle (this occurs at the minimum input voltage). In addition, ensure the boost capacitor does not discharge to below the minimum gate-to-source voltage required to keep the high-side MOSFET fully enhanced for lowest on-resistance. This minimum gate-to-source voltage $V_{GS(MIN)}$ is determined by:

$$V_{GS(MIN)} = V_L - \frac{Q_G}{C_{BOOST}}$$

where Q_G is the total gate charge of the high-side MOSFET and C_{BOOST} is the boost capacitor value.

Compensation Design

The MAX8545/MAX8546/MAX8548 use a voltage-mode control scheme that regulates the output voltage. This is done by comparing the error amplifier's output (COMP) to a fixed internal ramp. The inductor and output capacitor create a double pole at the resonant frequency, which

has a gain drop of 40dB per decade, and a phase shift of 180°. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth, closed-loop system.

The basic regulator loop consists of a power modulator (Figure 3), an output feedback divider, and an error amplifier. The power modulator has DC gain set by V_{IN}/V_{RAMP}, with a double pole set by the inductor and output capacitor, and a single zero set by the output capacitor (C_{OUT}) and its equivalent series resistance (ESR). Below are equations that define the power modulator:

The DC gain of the power modulator is:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

where V_{RAMP} = 1V.

The pole frequency due to the inductor and output capacitor is:

$$f_{PMOD} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

The zero frequency due to the output capacitor's ESR is:

$$f_{ZESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The output capacitor is usually comprised of several same capacitors connected in parallel. With n capacitors in parallel, the output capacitance is:

$$C_{OUT} = n \times C_{EACH}$$

The total ESR is:

$$ESR = \frac{ESR_{EACH}}{n}$$

The ESR zero (f_{ZESR}) for a parallel combination of capacitors is the same as for an individual capacitor.

The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 0.8V.

The transconductance error amplifier has DC gain $G_{EA(dc)}$ of 72dB. A dominant pole (f_{DPEA}) is set by the compensation capacitor (C_C), the amplifier output resistance (R_O) equals 37MΩ, and the compensation resistor (R_C):

$$f_{DPEA} = \frac{1}{2\pi \times C_C \times (R_O + R_C)}$$

The compensation resistor and the compensation capacitor set a zero:

$$f_{ZEA} = \frac{1}{2\pi \times C_C \times R_C}$$

The total closed-loop gain must equal unity at the crossover frequency. The crossover frequency should be higher than f_{ZESR}, so that the -1 slope is used to cross over at unity gain. Also, the crossover frequency should be less than or equal to 1/5 the switching frequency (f_{SW}) of the controller:

$$f_{ZESR} < f_C \le \frac{f_{SW}}{5}$$

The loop-gain equation at the crossover frequency is:

$$V_{FB}/V_{OUT} \times G_{EA(f_C)} \times G_{MOD(f_C)} = 1$$

where $G_{EA(f_C)} = g_{mEA} \times R_C$, and $G_{MOD(f_C)} = G_{MOD(DC)} \times (f_{PMOD})^2 / (f_{ZESR} \times f_C)$.

The compensation resistor, R_C, is calculated from:

$$R_C = V_{OUT}/ g_{mEA} \times V_{FB} \times G_{MOD(f_C)}$$

where g_{mEA} = 108µS.

Due to the underdamped (Q > 1) nature of the output LC double pole, the error-amplifier compensation zero should be approximately 0.2 f_{PMOD} to provide good phase boost. C_C is calculated from:

$$C_C = \frac{5}{2\pi \times R_C \times f_{PMOD}}$$

A small capacitor, C_F, can also be added from COMP to GND to provide high-frequency decoupling. C_F adds another high-frequency pole, f_{PHF}, to the error-amplifier response. This pole should be greater than 100 times the error-amplifier zero frequency to have negligible impact on the phase margin. This pole should also be less than 1/2 the switching frequency for effective decoupling:

$$100\ f_{ZEA} < f_{PHF} < 0.5\ f_{sw}$$

Select a value for f_{PHF} in the range given above, then solve for C_F using the following equation:

$$C_F = \frac{1}{2\pi \times R_C \times f_{PHF}}$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. If possible, mount all the power components on the top side of the board with their

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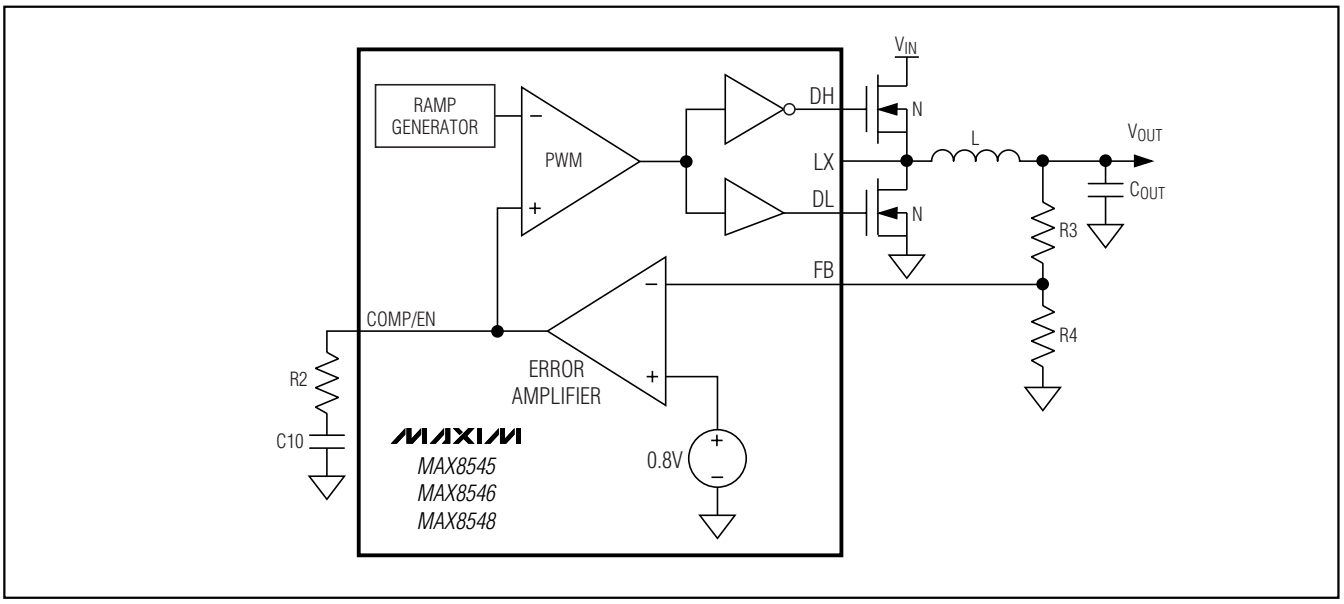

Figure 3. Compensation Scheme

ground terminals flush against one another. Follow these guidelines for good PCB layout:

1) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
2) Connect the power and analog grounds close to the IC pin 7.
3) Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a few milohms of excess trace resistance cause a measurable efficiency penalty.
4) LX and GND connections to the low-side MOSFET for current sensing must be made using Kelvin sense connections to guarantee the current-limit accuracy. With 8-pin MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting LX and GND inside (underneath) the 8-pin package.
5) When tradeoffs in trace lengths must be made, it is preferable to allow the inductor charging current path to be longer than the discharge path. For example, it is better to allow some extra distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
6) Ensure that the connection between the inductor and C3 is short and direct.
7) Route switching nodes (BST, LX, DH, and DL) away from sensitive analog areas (COMP and FB).

Ensure the C1 ceramic bypass capacitor is immediately adjacent to the pins and as close to the device as possible. Furthermore, the V_{IN} and GND pins of MAX8545/MAX8546/MAX8548 must terminate at the two ends of C1 before connecting to the power switches and C2.

Table 1a. Component Selection for Standard Applications for V_{IN} = 2.7V to 5.5V, V_{OUT} = 1.8V / 3A (Figure 1) (MAX8546 Only)

COMPONENT	QTY	DESCRIPTION
C1, C4	2	1µF, 10V X7R ceramic capacitors Taiyo Yuden LMK212BJ105MG
C2	0	Not installed
C3	1	1200µF, 10V, 44mΩ, 1.25A aluminum electrolytic capacitor SANYO 10MV1200AX (10 x 16 case size)
C5, C8, C9	3	0.1µF, 10V X7R ceramic capacitors Kemet C0603C104M8RAC
C6, C7	2	1000µF, 6.3V, 69mΩ, 0.8A aluminum electrolytic capacitors SANYO 6.3MV1000AX (8 x 20 case size)
C10	1	1.5nF, 10V X7R ceramic capacitor Kemet C0603C152M8RAC
C11	0	Not installed
D1, D2	2	30V, 100mA Schottky diodes Central Semiconductor CMPSH-3
L1	1	4.7µH, 5.7A, 18mΩ inductor Sumida CDRH124-4R7
Q1	1	20V/30V, 35mΩ dual n-channel, 8-pin SO Vishay Si4966DY **(for 2.7V to 3.6V_{IN})** Fairchild FDS6912A **(for 4.5V to 5.5V_{IN})**
R1	1	10Ω ±5% resistor
R2	1	150kΩ ±5% resistor
R3	1	5.11kΩ ±1% resistor
R4	1	4.02kΩ ±1% resistor

Table 1b. Component Selection for Standard Applications for V_{IN} = 2.7V to 5.5V, V_{OUT} = 1.8V / 6A (Figure 1) (MAX8546 Only)

COMPONENT	QTY	DESCRIPTION
C1, C4	2	1µF, 10V X7R ceramic capacitors Taiyo Yuden LMK212BJ105MG
C2, C3	2	1200µF, 10V, 44mΩ, 1.25A aluminum electrolytic capacitors SANYO 10MV1200AX (10 x 16 case size)
C5, C8, C9	3	0.1µF, 10V X7R ceramic capacitors Kemet C0603C104M8RAC
C6, C7	2	1500µF, 6.3V, 44mΩ, 1.25A aluminum electrolytic capacitors SANYO 6.3MV1500AX (10 x 20 case size)
C10	1	1.5nF, 10V X7R ceramic capacitor Kemet C0603C152M8RAC
C11	0	Not installed
D1, D2	2	30V, 100mA Schottky diodes Central Semiconductor CMPSH-3
L1	1	2.1µH, 8A, 11.6mΩ inductor Sumida CEP122-2R1
Q1	1	20V, 18mΩ dual n-channel, 8-pin SO Fairchild FDS6898A **(for 2.7V to 3.6V_{IN})** Fairchild FDS6890A **(for 4.5V to 5.5V_{IN})**
R1	1	10Ω ±5% resistor
R2	1	110kΩ ±5% resistor
R3	1	5.11kΩ ±1% resistor
R4	1	4.02kΩ ±1% resistor

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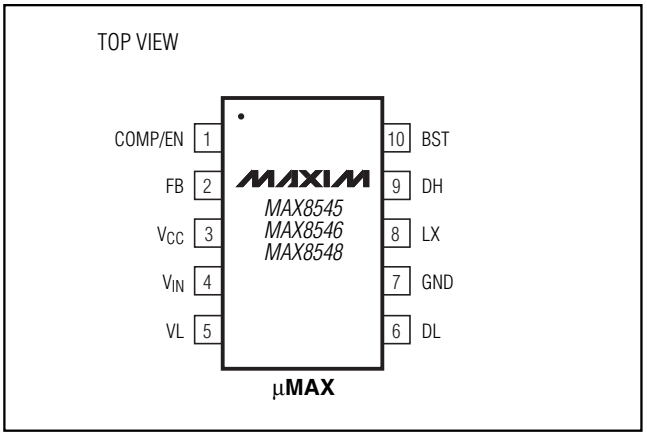
Table 2a. Component Selection for Standard Applications for V_{IN} = 10V to 24V, V_{OUT} = 2.5V / 3A (Figure 2) (MAX8546 Only)

COMPONENT	QTY	DESCRIPTION
C1	1	1µF, 10V X7R ceramic capacitor Taiyo Yuden LMK212BJ105MG
C2	0	Not installed
C3	1	470µF, 35V, 39mΩ, 1.45A aluminum electrolytic capacitor SANYO 35MV470AX (10 x 22 case size)
C4, C12	2	1µF, 35V X7R ceramic capacitors Taiyo Yuden GMK316BJ105ML
C5, C8, C9	3	0.1µF, 10V X7R ceramic capacitors Kemet C0603C104M8RAC
C6, C7	2	1000µF, 6.3V, 69mΩ, 0.8A aluminum electrolytic capacitors SANYO 6.3MV1000AX (8 x 20 case size)
C10	1	6.8nF, 10V X7R ceramic capacitor Kemet C0603C6822M8RAC
C11	0	Not installed
D1, D2	2	30V, 100mA Schottky diodes Central Semiconductor CMPSH-3
L1	1	8.2µH, 5.8A, 9.5mΩ inductor Sumida CEP125-8R2
Q1	1	30V, 35mΩ, dual n-channel, 8-pin SO Fairchild FDS6912A
R1	1	10Ω ±5% resistor
R2	1	82kΩ ±5% resistor
R3	1	8.66kΩ ±1% resistor
R4	1	4.02kΩ ±1% resistor

Table 2b. Component Selection for Standard Applications for V_{IN} = 10V to 24V, V_{OUT} = 2.5V / 6A (Figure 2) (MAX8546 Only)

COMPONENT	QTY	DESCRIPTION
C1	1	1µF, 10V X7R ceramic capacitor Taiyo Yuden LMK212BJ105MG
C2, C3	2	470µF, 35V, 39mΩ, 1.45A aluminum electrolytic capacitors SANYO 35MV470AX (10 x 22 case size)
C4, C12	2	1µF, 35V X7R ceramic capacitors Taiyo Yuden GMK316BJ105ML
C5, C8, C9	3	0.1µF, 10V X7R ceramic capacitors Kemet C0603C104M8RAC
C6, C7	2	1500µF, 6.3V, 44mΩ, 1.25A aluminum electrolytic capacitors SANYO 6.3MV1500AX (10 x 20 case size)
C10	1	6.8nF, 10V X7R ceramic capacitor Kemet C0603C682M8RAC
C11	0	Not installed
D1, D2	2	30V, 100mA Schottky diodes Central Semiconductor CMPSH-3
L1	1	4µH, 8.3A, 6.6mΩ inductor Sumida CEP125-4R0
Q1	1	30V, 18mΩ (LSFET)/35mΩ (HSFET), dual n-channel, 8-pin SO Fairchild FDS6982
R1	1	10Ω ±5% resistor
R2	1	68kΩ ±5% resistor
R3	1	8.66kΩ ±1% resistor
R4	1	4.02kΩ ±1% resistor

Pin Configuration



Chip Information

TRANSISTOR COUNT: 3351

PROCESS: BiCMOS

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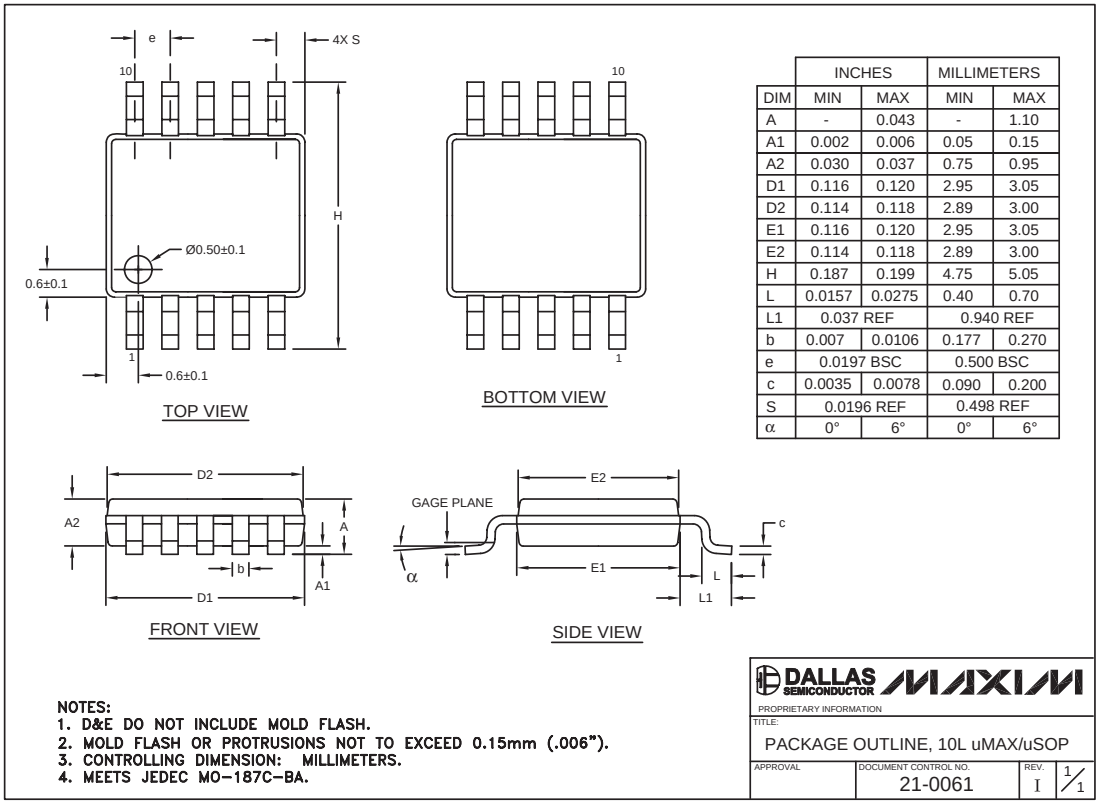
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

Revision History

Pages changed at Rev 2: 1, 2, 8, 11, 15, 16, 18