

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)

V_{CC}	-0.3V to 6.0V
All Other Inputs.....	-0.3V to ($V_{CC} + 0.3V$)
Input Current, V_{CC} , $\overline{MR}$	20mA
Output Current, RESET or RESET $\overline{}$	20mA
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
SOT143 (derate 4mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$).....	320mW

Operating Temperature Range..... -40°C to $+85^\circ\text{C}$

Junction Temperature..... $+150^\circ\text{C}$

Storage Temperature Range..... -65°C to $+160^\circ\text{C}$

Lead Temperature (soldering, 10sec)..... $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{CC} = 5V$ for L/M versions, $V_{CC} = 3.3V$ for T/S versions, $V_{CC} = 3V$ for R version, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.

Typical values are at $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	T _A = 0°C to +70°C		1.0		5.5	V
		T _A = -40°C to +85°C		1.2			
Supply Current	I _{CC}	MAX81_L/M, V _{CC} = 5.5V, I _{OUT} = 0			6	15	μA
		MAX81_R/S/T, V _{CC} = 3.6V, I _{OUT} = 0			2.7	10	
Reset Threshold	V _{TH}	MAX81_L	T _A = +25°C	4.54	4.63	4.72	V
			T _A = -40°C to +85°C	4.50		4.75	
		MAX81_M	T _A = +25°C	4.30	4.38	4.46	
			T _A = -40°C to +85°C	4.25		4.50	
		MAX81_T	T _A = +25°C	3.03	3.08	3.14	
			T _A = -40°C to +85°C	3.00		3.15	
		MAX81_S	T _A = +25°C	2.88	2.93	2.98	
			T _A = -40°C to +85°C	2.85		3.00	
		MAX81_R	T _A = +25°C	2.58	2.63	2.68	
			T _A = -40°C to +85°C	2.55		2.70	
Reset Threshold Tempco					30		ppm/°C
V _{CC} to Reset Delay (Note 2)		V _{OD} = 125mV, MAX81_L/M			40		μs
		V _{OD} = 125mV, MAX81_R/S/T			20		
Reset Active Timeout Period	t _{RP}	V _{CC} = V _{TH} (MAX)		140		560	ms
MR Minimum Pulse Width	t _{MR}			10			μs
MR Glitch Immunity (Note 3)					100		ns
MR to Reset Propagation Delay (Note 2)	t _{MD}				0.5		μs
MR Input Threshold	V _{IH}	V _{CC} > V _{TH} (MAX), MAX81_L/M	2.3				V
	V _{IL}				0.8		
	V _{IH}	V _{CC} > V _{TH} (MAX), MAX81_R/S/T	0.7 x V _{CC}				
	V _{IL}		0.25 x V _{CC}				
MR Pull-Up Resistance				10	20	30	kΩ
RESET Output Voltage (MAX812)	V _{OH}	I _{SOURCE} = 150μA, 1.8V < V _{CC} < V _{TH} (MIN)		0.8 x V _{CC}			V
	V _{OL}	MAX812R/S/T only, I _{SINK} = 1.2mA, V _{CC} = V _{TH} (MAX)		0.3			
		MAX812L/M only, I _{SINK} = 3.2mA, V _{CC} = V _{TH} (MAX)		0.4			

Electrical Characteristics (continued)

(V_{CC} = 5V for L/M versions, V_{CC} = 3.3V for T/S versions, V_{CC} = 3V for R version, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

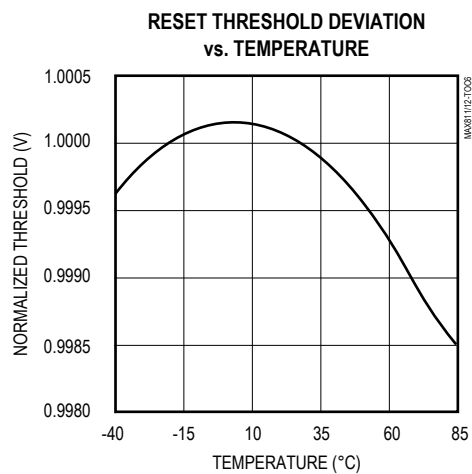
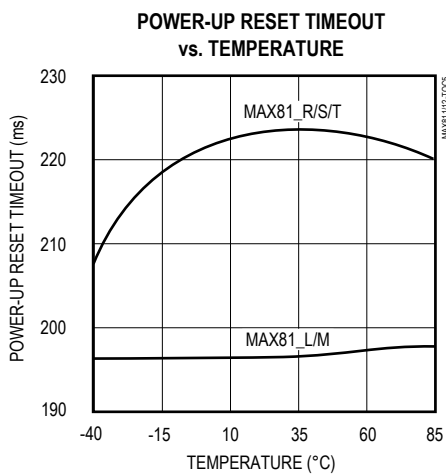
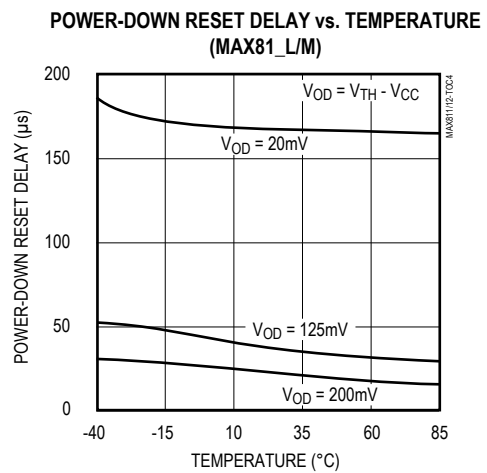
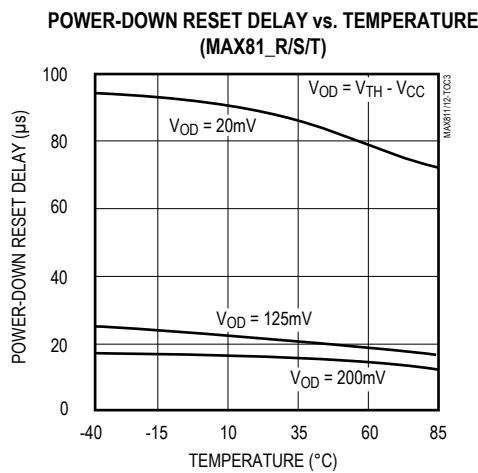
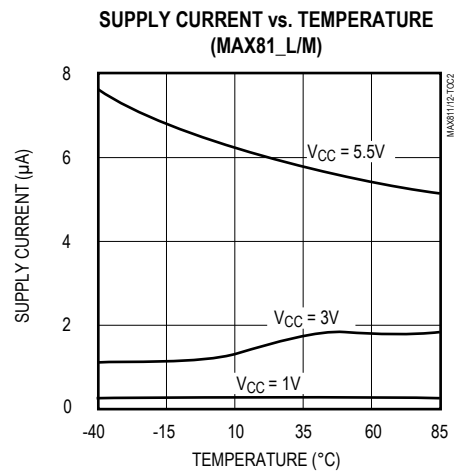
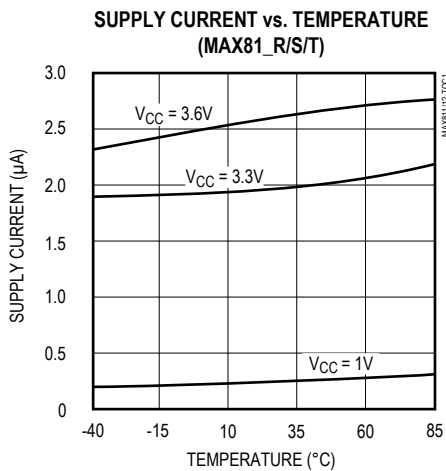
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX811)	V_{OL}	MAX811R/S/T only, $I_{SINK} = 1.2mA$, $V_{CC} = V_{TH(MIN)}$			0.3	V
		MAX811L/M only, $I_{SINK} = 3.2mA$, $V_{CC} = V_{TH(MIN)}$			0.4	
		$I_{SINK} = 50\mu A$, $V_{CC} > 1.0V$			0.3	
	V_{OH}	MAX811R/S/T only, $I_{SOURCE} = 500\mu A$, $V_{CC} > V_{TH(MAX)}$	$0.8 \times V_{CC}$			
		MAX811L/M only, $I_{SOURCE} = 800\mu A$, $V_{CC} > V_{TH(MAX)}$	$V_{CC} - 1.5$			

Note 1: Production testing done at T_A = +25°C, over temperature limits guaranteed by design using six sigma design limits.

Note 2: RESET output for MAX811, RESET output for MAX812.

Note 3: "Glitches" of 100ns or less typically will not generate a reset pulse.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

Pin Description

PIN		NAME	FUNCTION
MAX811	MAX812		
1	1	GND	Ground
2	—	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low. $\overline{\text{RESET}}$ remains low for the Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated.
—	2	RESET	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low. RESET remains high for Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated.
3	3	$\overline{\text{MR}}$	Manual Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for 180ms after $\overline{\text{MR}}$ returns high. This active-low input has an internal 20k Ω pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused.
4	4	V_{CC}	+5V, +3.3V, or +3V Supply Voltage

Detailed Description

Reset Output

A microprocessor's (μ P's) reset input starts the μ P in a known state. These μ P supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ is guaranteed to be a logic low for $V_{CC} > 1V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high.

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{\text{RESET}}$ goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer starts after V_{CC} returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

The manual reset input ($\overline{\text{MR}}$) can also initiate a reset. See the *Manual Reset Input* section.

The MAX812 has an active-high RESET output that is the inverse of the MAX811's $\overline{\text{RESET}}$ output.

Manual Reset Input

Many μ P-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for the Reset Active Timeout Period (t_{RP}) after $\overline{\text{MR}}$ returns high. This input has an internal 20k Ω pull-up resistor, so it can be left open if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1 μ F capacitor from $\overline{\text{MR}}$ to ground provides additional noise immunity.

Reset Threshold Accuracy

The MAX811/MAX812 are ideal for systems using a 5V $\pm 5\%$ or 3V $\pm 5\%$ power supply with ICs specified for 5V $\pm 10\%$ or 3V $\pm 10\%$, respectively. They are designed to meet worst-case specifications over temperature. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range for the system ICs. The thresholds are pre-trimmed and exhibit tight distribution, reducing the range over which an undesirable reset may occur.

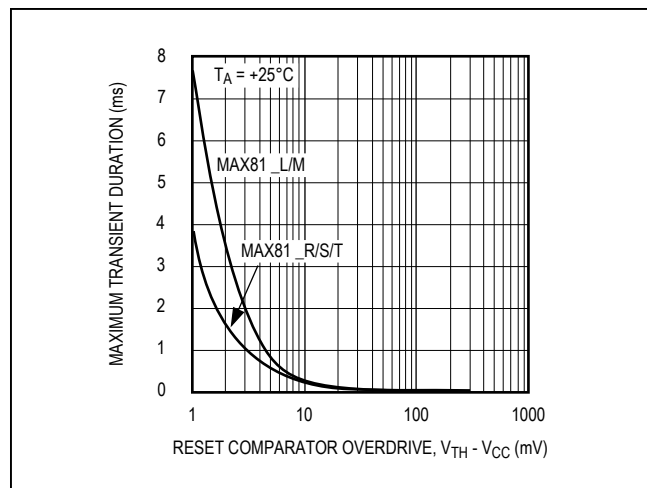


Figure 1. Maximum Transient Duration without Causing a Reset Pulse vs. Comparator Overdrive

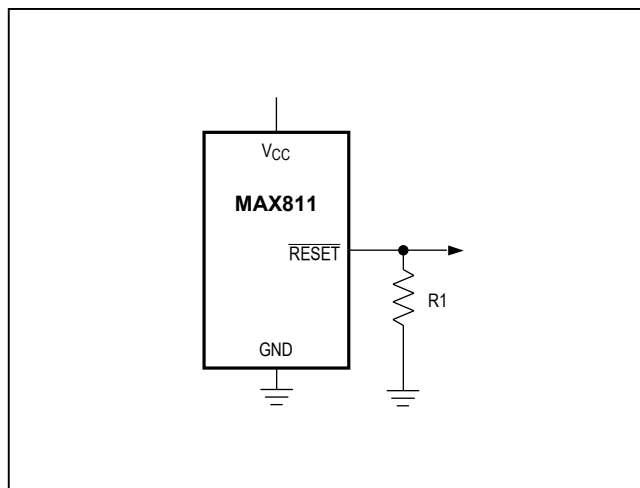


Figure 2. $\overline{\text{RESET}}$ Valid to $V_{CC} = \text{Ground}$ Circuit

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, the MAX811/MAX812 are relatively immune to short duration negative-going V_{CC} transients (glitches).

Figure 1 shows typical transient durations vs. reset comparator overdrive, for which the MAX811/MAX812 do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{CC} , starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 125mV below the reset threshold and lasts 40 μ s or less (MAX81_L/M) or 20 μ s or less (MAX81_T/S/R) will not cause a reset pulse to be issued. A 0.1 μ F capacitor mounted as close as possible to V_{CC} provides additional transient immunity.

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to $V_{CC} = 0\text{V}$

When V_{CC} falls below 1V, the MAX811 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to the $\overline{\text{RESET}}$ output can drift to undetermined voltages. This presents no problem in most applications, since most μ P and other circuitry is inoperative with V_{CC} below 1V. However, in applications where the $\overline{\text{RESET}}$ output must be valid down to 0V, adding a pull-down resistor to the $\overline{\text{RESET}}$ pin will cause any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Figure 2). R1's value is not critical; 100k Ω is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

A 100k Ω pull-up resistor to V_{CC} is also recommended for the MAX812 if RESET is required to remain valid for $V_{CC} < 1\text{V}$.

Interfacing to μ Ps with Bidirectional Reset Pins

μ Ps with bidirectional reset pins (such as the Motorola 68HC11 series) can contend with the MAX811/MAX812 reset outputs. If, for example, the MAX811 $\overline{\text{RESET}}$ output is asserted high and the μ P wants to pull it low, indeterminate logic levels may result. To correct such cases, connect a 4.7k Ω resistor between the MAX811 $\overline{\text{RESET}}$ (or MAX812 $\overline{\text{RESET}}$) output and the μ P reset I/O (Figure 3). Buffer the reset output to other system components.

Chip Information

TRANSISTOR COUNT: 341

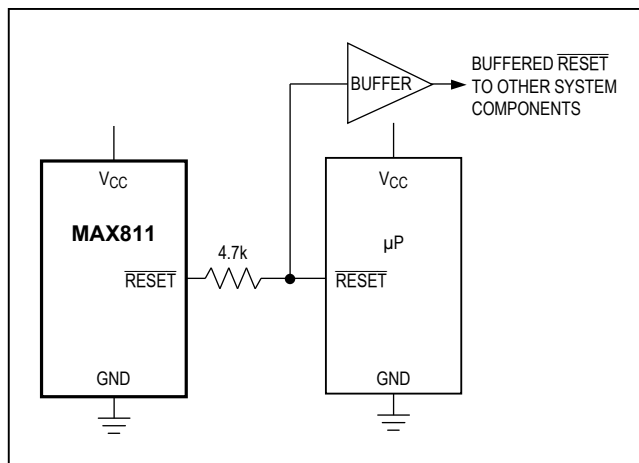


Figure 3. Interfacing to μ Ps with Bidirectional Reset I/O

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
4 SOT143	U4+1	21-0052	90-0183

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	6/15	Updated <i>Benefits and Features</i> and <i>Package Information</i> sections	1, 8
6	5/18	Updated <i>Absolute Maximum Ratings</i>	2

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