

Microprocessor Supervisory Circuit

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)

V _{CC}	-0.3V to +6V
VBATT	-0.3V to +6V
All Other Inputs	-0.3V to (V _{OUT} + 0.3V)

Input Current

V _{CC} Peak	1.0A
V _{CC} Continuous	250mA
VBATT Peak	250mA
VBATT Continuous	25mA
GND, BATT ON	100mA
All Other Outputs	25mA

Continuous Power Dissipation (T_A = +70°C)

Plastic DIP (derate 10.53mW/°C above +70°C)	842mW
Narrow SO (derate 8.70mW/°C above +70°C)	696mW
CERDIP (derate 10.00mW/°C above +70°C)	800mW
TSSOP (derate 6.70mW/°C above +70°C)	533mW

Operating Temperature Ranges

MAX791C_	0°C to +70°C
MAX791E_	-40°C to +85°C
MAX791MJE	-55°C to +125°C

Storage Temperature Range

Lead Temperature (soldering, 10s)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range V _{CC} , V _{BATT} (Note 1)				0		5.5	V
V _{OUT} in Normal Operating Mode	V _{CC} = 4.5V	I _{OUT} = 25mA		V _{CC} - 0.05	V _{CC} - 0.02		V
		I _{OUT} = 250mA	MAX791C/E	V _{CC} - 0.3	V _{CC} - 0.2		
			MAX791M	V _{CC} - 0.40			
	V _{CC} = 3V, V _{BATT} = 2.8V, I _{OUT} = 100mA			V _{CC} - 0.2	V _{CC} - 0.12		
V _{CC} -to-V _{OUT} On-Resistance	V _{CC} = 4.5V	MAX791C/E			0.8	1.2	Ω
		MAX791M			0.8	1.6	
	V _{CC} = 3V			1.2	2.0		
V _{OUT} in Battery-Backup Mode	V _{BATT} = 4.5V, I _{OUT} = 20mA			V _{BATT} - 0.3			V
	V _{BATT} = 2.8V, I _{OUT} = 10mA			V _{BATT} - 0.25			
	V _{BATT} = 2.0V, I _{OUT} = 5mA			V _{BATT} - 0.15			
V _{BATT} -to-V _{OUT} On-Resistance	V _{BATT} = 4.5V				8	15	Ω
	V _{BATT} = 2.8V				13	25	
	V _{BATT} = 2.0V				17	30	
Supply Current in Normal Operating Mode (excludes I _{OUT})	V _{CC} > V _{BATT} - 1V				50	150	μA
Supply Current in Battery-Backup Mode (excludes I _{OUT}) (Note 2)	V _{CC} < V _{BATT} - 1.2V, V _{BATT} = 2.8V	T _A = +25°C			0.04	1	μA
		T _A = T _{MIN} to T _{MAX}				5	
V _{BATT} Standby Current (Note 3)	V _{BATT} + 0.2V ≤ V _{CC}	T _A = +25°C		-0.1		0.02	μA
		T _A = T _{MIN} to T _{MAX}		-1.0		0.02	
Battery-Switchover Threshold	Power up			V _{BATT} + 0.03			V
	Power down			V _{BATT} - 0.03			
Battery-Switchover Hysteresis					60		mV
Low-Battery Detector Threshold					2		V

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MAX791

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 4.75V$ to $5.5V$, $V_{BATT} = 2.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATT ON Output Low Voltage	$I_{SINK} = 3.2mA$		0.1	0.4	V
	$I_{SINK} = 25mA$		0.7	1.5	
BATT ON Output Short-Circuit Current	Sink current		60		mA
	Source current	1	15	100	μA
RESET, LOW-LINE, AND WATCHDOG TIMER					
$\overline{RESET}$ Threshold Voltage		4.50	4.65	4.75	V
$\overline{RESET}$ Threshold Hysteresis			15		mV
$\overline{LOWLINE}$ -to- $\overline{RESET}$ Threshold Voltage			150		mV
V_{CC} -to- $\overline{RESET}$ Delay	Power down		100		μs
V_{CC} -to- $\overline{LOWLINE}$ Delay	Power down		80		μs
$\overline{RESET}$ Active Timeout Period	Power up	140	200	280	ms
Watchdog Timeout Period	SWT connected to V_{OUT}	1.0	1.6	2.25	s
Minimum Watchdog Timeout Period	4.7nF capacitor connected from SWT to GND		10		ms
Minimum Watchdog Input Pulse Width	$V_{IL} = 0.8V$, $V_{IH} = 0.75 \times V_{CC}$	100			ns
$\overline{WDPO}$ Pulse Width			1		ms
$\overline{WDPO}$ -to- $\overline{WDO}$ Delay			70		ns
$\overline{RESET}$ Output Voltage	MAX791C, $I_{SINK} = 50\mu A$, $V_{CC} = 1.0V$, V_{CC} falling		0.004	0.3	V
	MAX791E/M, $I_{SINK} = 50\mu A$, $V_{CC} = 1.2V$, V_{CC} falling		0.004	0.3	
	$I_{SINK} = 3.2mA$, $V_{CC} = 4.25V$		0.1	0.4	
	$I_{SOURCE} = 1.6mA$, $V_{CC} = 5V$	3.5			
$\overline{RESET}$ Output Short-Circuit Current	Output source current		7	20	mA
$\overline{LOWLINE}$ Output Voltage	$I_{SINK} = 3.2mA$, $V_{CC} = 4.25V$			0.4	V
	$I_{SOURCE} = 1\mu A$, $V_{CC} = 5V$	3.5			
$\overline{LOWLINE}$ Output Short-Circuit Current	Output source current		15	100	μA
$\overline{WDO}$ Output Voltage	$I_{SINK} = 3.2mA$			0.4	V
	$I_{SOURCE} = 500\mu A$, $V_{CC} = 5V$	3.5			
$\overline{WDO}$ Output Short-Circuit Current	Output source current		3	10	mA
$\overline{WDPO}$ Output Voltage	$I_{SINK} = 3.2mA$			0.4	V
	$I_{SOURCE} = 1mA$	3.5			
$\overline{WDPO}$ Output Short-Circuit Current	Output source current		7	20	mA

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 4.75V$ to $5.5V$, $V_{BATT} = 2.8V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WDI Threshold Voltage (Note 4)	V _{IH}	0.75 x V _{CC}			V
	V _{IL}	0.8			
WDI Input Current	WDI = 0V	-50	-10		μA
	WDI = V _{OUT}		20	50	
POWER-FAIL COMPARATOR					
PFI Input Threshold	V _{CC} = 5V	1.20	1.25	1.30	V
PFI Leakage Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I _{SINK} = 3.2mA			0.4	V
	I _{SOURCE} = 1μA, V _{CC} = 5V	3.5			
$\overline{PFO}$ Short-Circuit Current	Output sink current		60		mA
	Output source current	1	15	100	μA
PFI-to- $\overline{PFO}$ Delay	V _{IN} = -20mV, V _{OD} = 15mV		15		μs
	V _{IN} = 20mV, V _{OD} = 15mV		55		
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current	Disabled mode		±0.005	±1	μA
$\overline{CE}$ IN-to- $\overline{CE}$ OUT Resistance (Note 5)	Enabled mode		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disabled mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN-to- $\overline{CE}$ OUT Propagation Delay (Note 6)	50Ω source impedance driver, C _{LOAD} = 50pF		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	V _{CC} = 5V, I _{OUT} = -100μA	3.5			V
	V _{CC} = 0V, V _{BATT} = 2.8V, I _{OUT} = 1μA	2.7			
$\overline{RESET}$ -to- $\overline{CE}$ OUT Delay	Power down		15		μs
MANUAL RESET INPUT					
$\overline{MR}$ Minimum Pulse Width		25	15		μs
$\overline{MR}$ -to- $\overline{RESET}$ Propagation Delay			7		μs
$\overline{MR}$ Threshold	V _{CC} = 5V		1.25		V
$\overline{MR}$ Pull-Up Current	$\overline{MR}$ = 0V		23	250	μA

Note 1: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.

Note 2: The supply current drawn by the MAX791 from the battery (excluding I_{OUT}) typically goes to $10\mu A$ when $(V_{BATT} - 1V) < V_{CC} < V_{BATT}$. In most applications, this is a brief period as V_{CC} falls through this region.

Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: WDI is internally connected to a voltage-divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

Note 5: The chip-enable resistance is tested with $V_{CC} = 4.75V$, $\overline{CE}$ IN = V , $\overline{CE}$ OUT = $V_{CC} / 2$.

Note 6: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

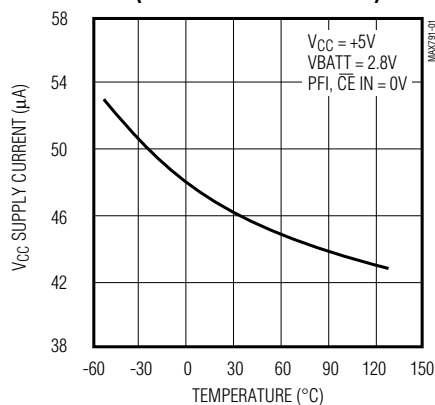
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Typical Operating Characteristics

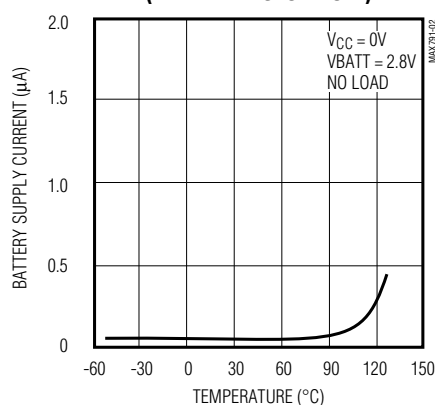
($T_A = +25^\circ\text{C}$, unless otherwise noted.)

MAX791

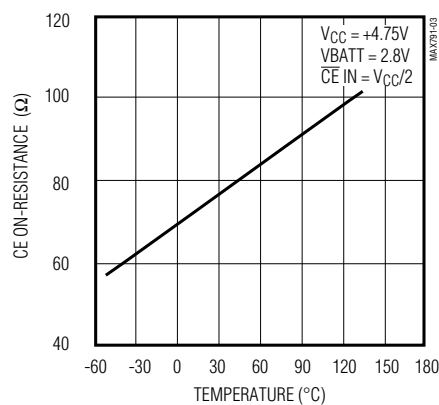
**V_{CC} SUPPLY CURRENT vs. TEMPERATURE
(NORMAL OPERATING MODE)**



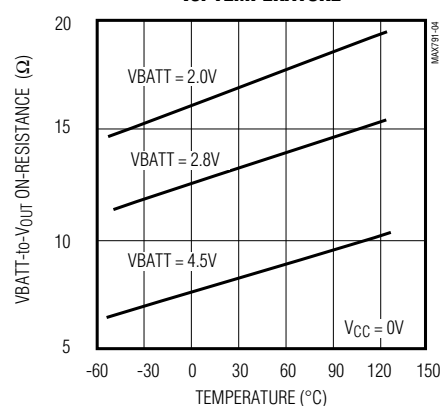
**BATTERY-SUPPLY CURRENT vs. TEMPERATURE
(BATTERY-BACKUP MODE)**



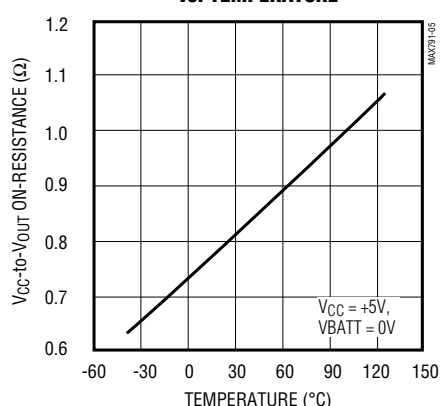
**CHIP-ENABLE ON-RESISTANCE
vs. TEMPERATURE**



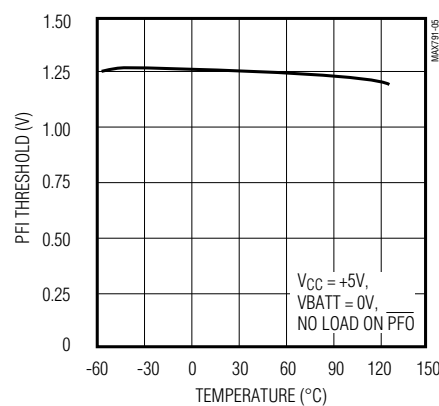
**VBATT-to-V_{OUT} ON-RESISTANCE
vs. TEMPERATURE**



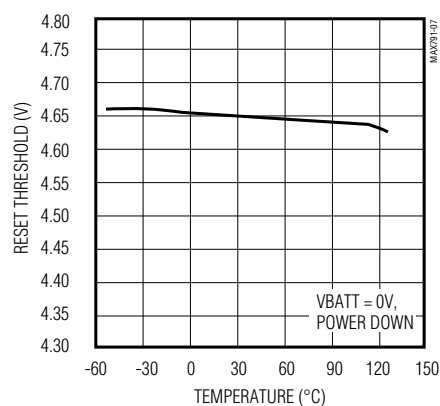
**V_{CC}-to-V_{OUT} ON-RESISTANCE
vs. TEMPERATURE**



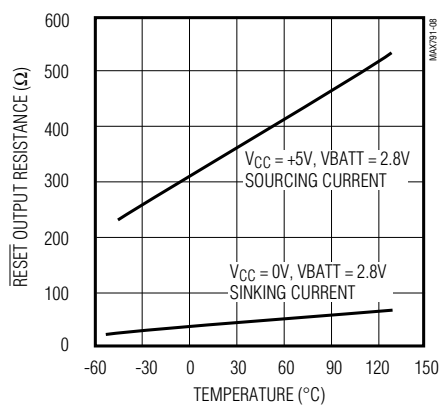
**PFI THRESHOLD
vs. TEMPERATURE**



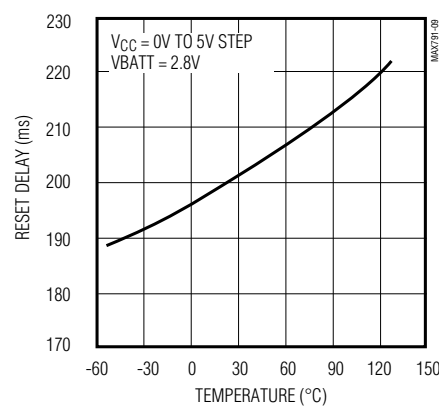
**RESET THRESHOLD
vs. TEMPERATURE**



**RESET OUTPUT RESISTANCE
vs. TEMPERATURE**



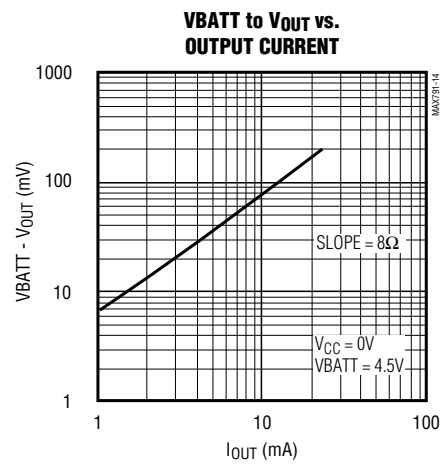
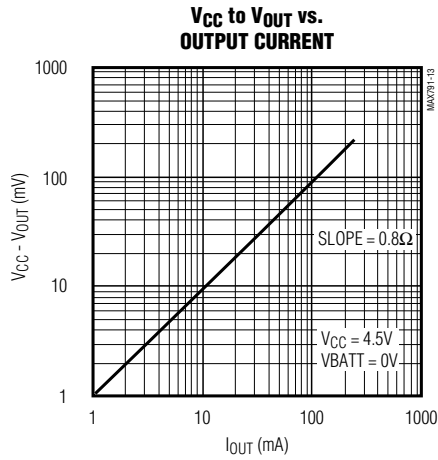
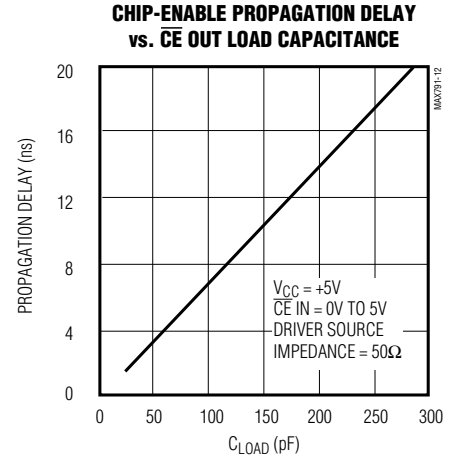
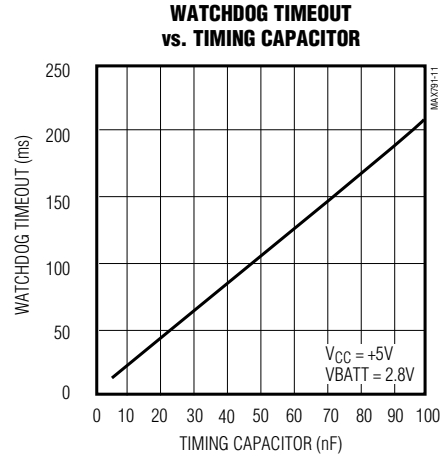
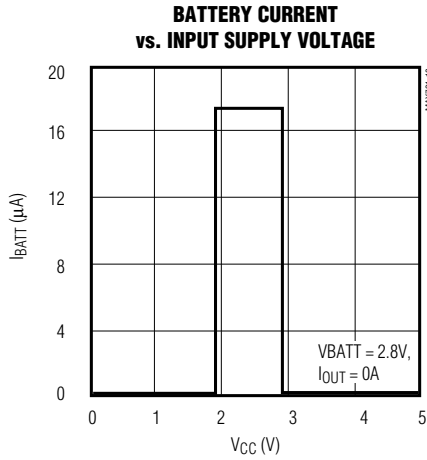
**RESET DELAY
vs. TEMPERATURE**



Microprocessor Supervisory Circuit

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Pin Description

MAX791

PIN	NAME	FUNCTION
1	VBATT	Backup-Battery Input. Connect to external battery or capacitor and charging circuit.
2	V _{OUT}	Output Supply Voltage. V _{OUT} connects to V _{CC} when V _{CC} is greater than VBATT and V _{CC} is above the reset threshold. When V _{CC} falls below VBATT and V _{CC} is below the reset threshold, V _{OUT} connects to VBATT. Connect a 0.1µF capacitor from V _{OUT} to GND.
3	V _{CC}	Input Supply Voltage—+5V input
4	GND	Ground. 0V reference for all signals.
5	BATT ON	Battery-On Output. Goes high when V _{OUT} switches to VBATT. Goes low when V _{OUT} switches to V _{CC} . Connect the base of a PNP through a current-limiting resistor to BATT ON for V _{OUT} current requirements greater than 250mA.
6	P _{FO}	Power-Fail Output. This is the output of the power-fail comparator. P _{FO} goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.
7	PFI	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, P _{FO} goes low. Connect PFI to GND or V _{OUT} when not used.
8	SWT	Set Watchdog-Timeout Input. Connect this input to V _{OUT} to select the default 1.6s watchdog-timeout period. Connect a capacitor between this input and GND to select another watchdog-timeout period. Watchdog-timeout period = 2.1 x (capacitor value in nF) ms.
9	M _R	Manual-Reset Input. This input can be tied to an external momentary pushbutton switch, or to a logic gate output. RESET remains low as long as M _R is held low and for 200ms after M _R returns high.
10	LOWLINE	LOWLINE Output goes low when V _{CC} falls to 150mV above the reset threshold. The output can be used to generate an NMI if the unregulated supply is inaccessible.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog time-out period, WDO goes low. WDO remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage-divider between V _{OUT} and GND, which sets it to mid-supply when left unconnected.
12	C _E OUT	Chip-Enable Output. C _E OUT goes low only when C _E IN is low and V _{CC} is above the reset threshold. If C _E IN is low when reset is asserted, C _E OUT will stay low for 15µs or until C _E IN goes high, whichever occurs first.
13	C _E IN	Chip-Enable Input. The input to chip-enable gating circuit. Connect to GND or V _{OUT} if not used.
14	WDO	Watchdog Output. WDO goes low if WDI remains either high or low longer than the watchdog-timeout period. WDO returns high on the next transition at WDI. WDO remains high if WDI is unconnected. WDO is also high when RESET is asserted.
15	RESET	RESET Output goes low whenever V _{CC} falls below the reset threshold. RESET will remain low for typically 200ms after V _{CC} crosses the reset threshold on power-up.
16	WDPO	Watchdog-Pulse Output. Upon the absence of a transition at WDI, WDPO will pulse low for a minimum of 1ms. WDPO precedes WDO by 70ns.

Microprocessor Supervisory Circuit

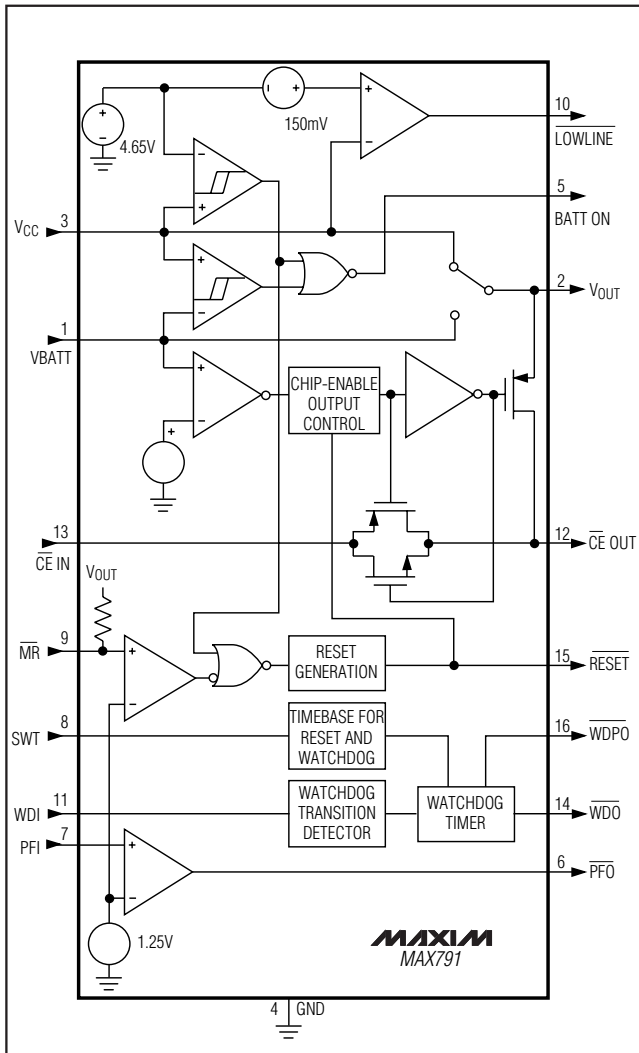


Figure 1. MAX791 Block Diagram

Detailed Description

Manual Reset Input

Many μ P-based products require manual-reset capability, allowing the operator or test technician to initiate a reset. The Manual Reset Input (MR) can be connected directly to a switch, without an external pull-up resistor or debouncing network. It connects to a 1.25V comparator, and has a pull-up to V_{OUT} as shown in Figure 1. The propagation delay from asserting MR to RESET asserted is 4 μ s typ. Pulsing MR low for a minimum of 15 μ s resets all the internal counters, sets the Watchdog Output (WDO) and Watchdog-Pulse Output (WDPO)

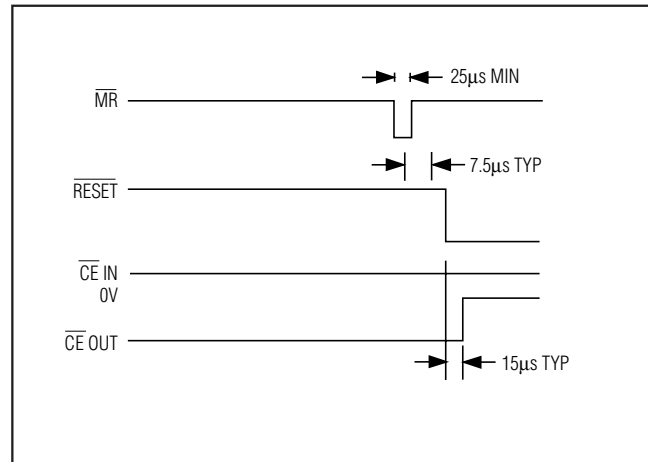


Figure 2. Manual-Reset Timing Diagram

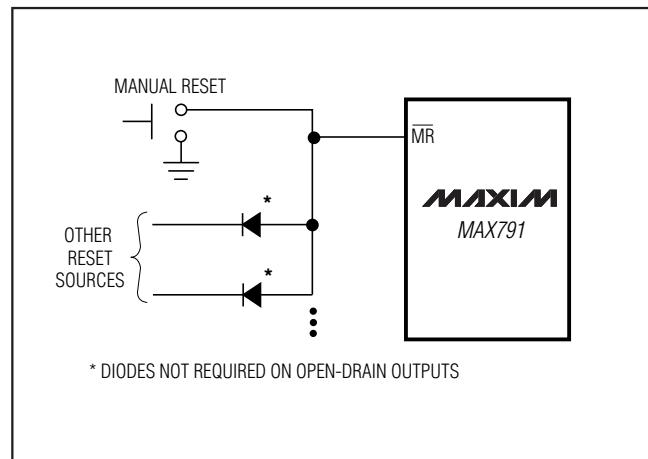


Figure 3. Diode "OR" Connections Allow Multiple Reset Sources to Connect to MR

high, and sets the Set Watchdog-Timeout (SWT) input to $V_{OUT} - 0.6V$, if it is not already connected to V_{OUT} (for internal timeouts). It also disables the chip-enable function, setting the Chip-Enable Output (CE OUT) to a high state. The RESET output remains active as long as MR is held low, and the reset-timeout period begins after MR returns high (Figure 2).

Use this input as either a digital-logic input or a second low-line comparator. Normal TTL/CMOS levels can be wire-OR connected via pull-down diodes (Figure 3), and open-drain/collector outputs can be wire-ORed directly.

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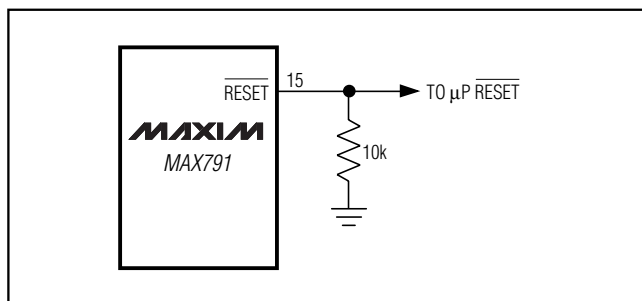


Figure 4. Adding an External Pull-Down Resistor Ensures RESET is Valid with VCC Down to GND

RESET Output

The MAX791's RESET output ensures that the μP powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The RESET output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, RESET sources 1.6mA at typically $V_{OUT} - 0.5V$. When no backup battery is used, RESET output is guaranteed to be valid down to $V_{CC} = 1V$, and an external 10k Ω pull-down resistor on RESET ensures that RESET will be valid with V_{CC} down to GND (Figure 4). As V_{CC} goes below 1V, the gate drive to the RESET output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10k Ω pull-down resistor ensures the parallel combination of switch plus resistor is around 10k Ω and the output saturation voltage is below 0.4V while sinking 40 μA . When using a 10k Ω external pull-down resistor, the high state for the RESET output with $V_{CC} = 4.75V$ is 4.5V typ. For battery voltages $\geq 2V$ connected to VBATT, RESET remains valid for V_{CC} from 0V to 5.5V.

RESET will be asserted during the following conditions:

- $V_{CC} < 4.65V$ (typ).
- $MR < 1.25V$ (typ).
- RESET remains asserted for 200ms (typ) after V_{CC} rises above 4.65V or after MR has exceeded 1.25V.

The MAX791 battery-switchover comparator does not affect RESET assertion. However, RESET is asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter this mode.

Watchdog Function

The watchdog monitors μP activity via the Watchdog Input (WDI). If the μP becomes inactive, WDO and WDPO are asserted. To use the watchdog function, connect WDI to a bus line or μP I/O line. If WDI remains

high or low for longer than the watchdog timeout period (1.6s nominal), WDPO and WDO are asserted, indicating a software fault condition (see *Watchdog Output* and *Watchdog-Pulse Output* sections).

Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at WDI during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6s. Select alternative timeout periods by connecting an external capacitor from SWT to GND (see *Selecting an Alternative Watchdog Timeout Period* section).

To disable the watchdog function, leave WDI floating. An internal resistor network (100k Ω equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Watchdog Output

WDO remains high if there is a transition or pulse at WDI during the watchdog-timeout period. The watchdog function is disabled and WDO is a logic high when V_{CC} is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog-timeout period, WDO goes low 70ns after the falling edge of WDPO and remains low until the next transition at WDI (Figure 5). A flip-flop can force the system into a hardware shutdown if there are two successive watchdog faults (Figure 6). WDO has a 2 x TTL output characteristic.

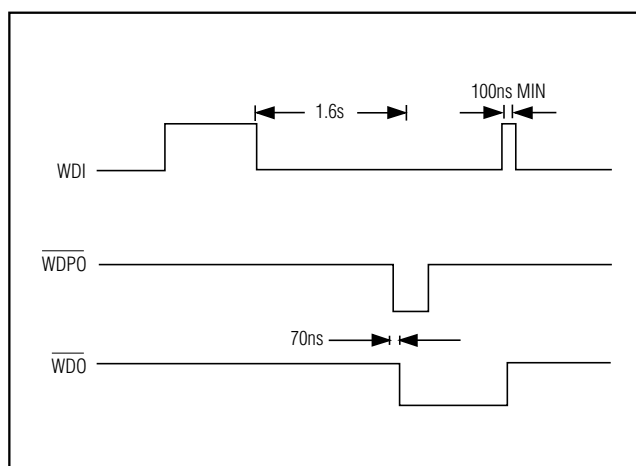


Figure 5. WDI, $\overline{WDO}$, and $\overline{WDPO}$ Timing Diagram (V_{CC} Mode)

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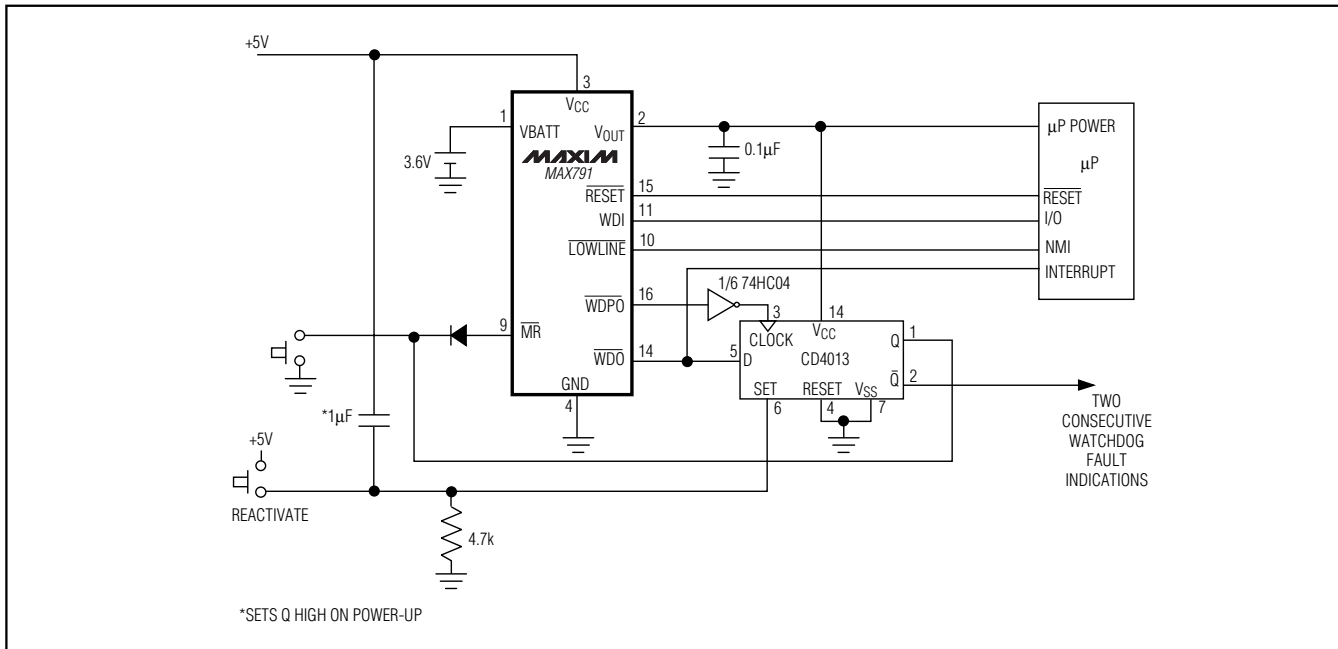


Figure 6. Two Consecutive Watchdog Faults Latch the System in Reset

Watchdog-Pulse Output

As described in the preceding section, WDPO can be used as the clock input to an external D flip-flop. Upon the absence of a watchdog edge or pulse at WDI at the end of a watchdog-timeout period, WDPO will pulse low for 1ms. The falling edge of WDPO precedes WDO by 70ns. Since WDO is high when WDPO goes low, the flip-flop's Q output remains high as WDO goes low (Figure 5). If the watchdog timer is not reset by a transition at WDI, WDO remains low and WDPO clocks a logic low to the Q output, causing the MAX791 to latch in reset. If the watchdog timer is reset by a transition at WDI, WDO goes high and the flip-flop's Q output remains high. Thus, a system shutdown is only caused by two successive watchdog faults.

The internal pull-up resistors associated with WDO and WDPO connect to VOUT. Therefore, do not connect these outputs directly to CMOS logic that is powered from VCC since, in the absence of VCC (i.e., battery mode), excessive current will flow from WDO or WDPO through the protection diode(s) of the CMOS-logic inputs to ground.

Selecting an Alternative Watchdog-Timeout Period

SWT input controls the watchdog-timeout period. Connecting SWT to VOUT selects the internal 1.6s watch-

dog-timeout period. Select an alternative timeout period by connecting a capacitor between SWT and GND. Do not leave SWT floating, and do not connect it to ground. The following formula determines the watchdog-timeout period:

$$\text{Watchdog-timeout period} = 2.1 \times (\text{capacitor value in nF}) \text{ ms}$$

This formula is valid for capacitance values between 4.7nF and 100nF (see the Watchdog Timeout vs. Timing Capacitor graph in the *Typical Operating Characteristics*). SWT is internally connected to a $\pm 100\text{nA}$ (typ) current source, which charges and discharges the timing capacitor to create the oscillator frequency that sets the watchdog-timeout period (see *Connecting a Timing Capacitor to SWT* section).

Chip-Enable Signal Gating

The MAX791 provides internal gating of chip-enable (CE) signals to prevent erroneous data from corrupting the CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX791 uses a series transmission gate from the Chip-Enable Input (CE IN) to CE OUT (Figure 1).

The 10ns max CE propagation from CE IN to CE OUT

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MAX791

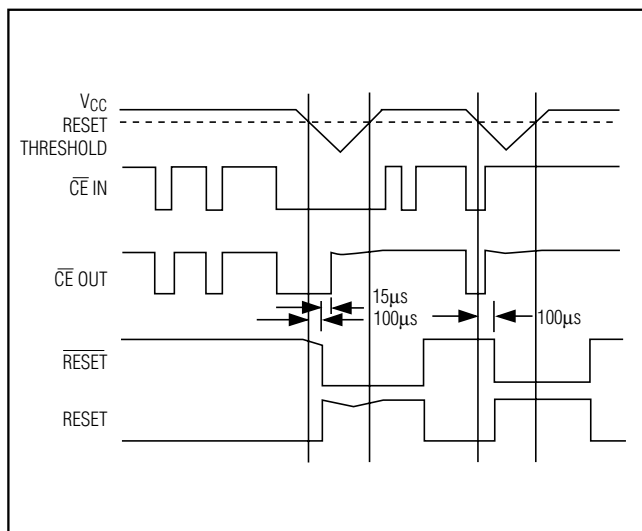


Figure 7. Reset and Chip-Enable Timing

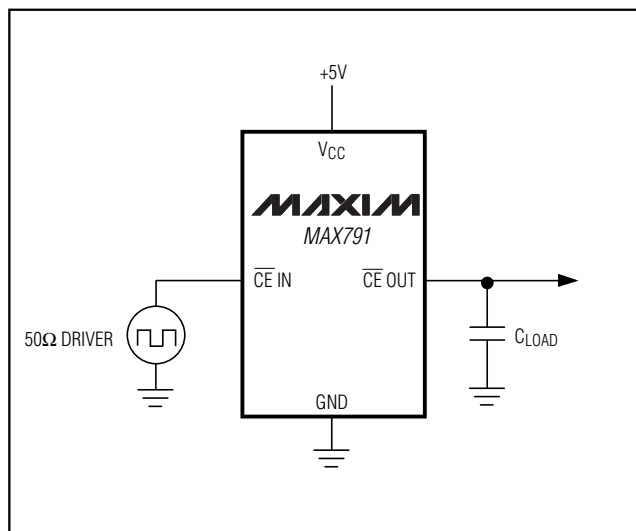


Figure 8. CE Propagation Delay Test Circuit

enables the MAX791 to be used with most μ Ps.

Chip-Enable Input

CE IN is high impedance (disabled mode) while RESET is asserted.

During a power-down sequence where V_{CC} passes 4.65V, CE IN assumes a high-impedance state when the voltage at CE IN goes high or 15 μ s after reset is asserted, whichever occurs first (Figure 7).

During a power-up sequence, CE IN remains high impedance, regardless of CE IN activity, until reset is deasserted following the reset-timeout period.

In the high-impedance mode, the leakage currents into this input are $\pm 1\mu$ A max over temperature. In the low-impedance mode, the impedance of CE IN appears as a 75 Ω resistor in series with the load at CE OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to CE IN and the capacitive loading on CE OUT (see the Chip-Enable Propagation Delay vs. CE OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on CE IN to the 50% point on CE OUT using a 50 Ω driver and 50pF of load capacitance (Figure 8). For minimum propagation delay, minimize the capacitive load at CE OUT and use

a low output-impedance driver.

Chip-Enable Output

In the enabled mode, the impedance of CE OUT is equivalent to 75 Ω in series with the source driving CE IN. In the disabled mode, the 75 Ω transmission gate is off and CE OUT is actively pulled to V_{OUT} . This source turns off when the transmission gate is enabled.

LOWLINE Output

The low-line comparator monitors V_{CC} with a typical threshold voltage 150mV above the reset threshold, and has 15mV of hysteresis. LOWLINE typically sinks 3.2mA at 0.1V. For normal operation (V_{CC} above the LOWLINE threshold), LOWLINE is pulled to V_{OUT} . If access to the unregulated supply is unavailable, use LOWLINE to provide a nonmaskable interrupt (NMI) to the μ P as V_{CC} begins to fall (Figure 9a).

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include monitoring supplies other than 5V (see the *Typical Operating Circuit* and the *Monitoring a Negative Voltage* section) and early power-fail detection when the unregulated power is easily accessible (Figure 9b).

Microprocessor Supervisory Circuit

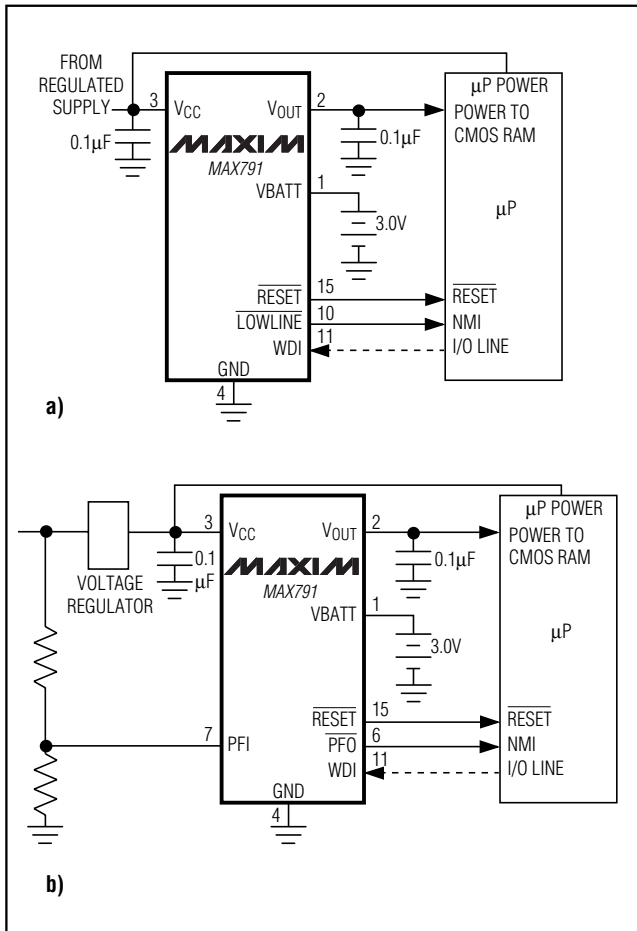


Figure 9. a) If the unregulated supply is inaccessible, LOWLINE generates the NMI for the μP . b) Use PFO to generate the μP NMI if the unregulated supply is inaccessible.

Power-Fail Input

PFI is the input to the power-fail comparator. PFI has a guaranteed input leakage of $\pm 25\text{nA}$ max over temperature. The typical comparator delay is $15\mu\text{s}$ from V_{IL} to V_{OL} (power failing), and $55\mu\text{s}$ from V_{IH} to V_{OH} (power being restored). If unused, connect this input to ground.

Power-Fail Output

The Power-Fail Output (PFO) goes low when PFI goes below 1.25V . It typically sinks 3.2mA with a saturation voltage of 0.1V . With PFI above 1.25V , PFO is actively pulled to V_{OUT} . Connecting PFI through a voltage-divider to an unregulated supply allows PFO to generate an NMI as the unregulated power begins to fall (Figure 9b). If the unregulated supply is inaccessible,

Table 1. Input and Output States in Battery-Backup Mode

PIN	NAME	STATUS
1	VBATT	Supply current is $1\mu\text{A}$ maximum.
2	VOUT	V_{OUT} is connected to VBATT through an internal PMOS switch.
3	VCC	Battery-switchover comparator monitors V_{CC} for active switchover.
4	GND	GND— 0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V_{OUT} .
6	PFO	The power-fail comparator remains active in the battery-backup mode for $V_{CC} \geq V_{BATT} - 1.2\text{V}$ typ. Below this voltage, PFO is forced low.
7	PFI	The power-fail comparator remains active in the battery-backup mode for $V_{CC} \geq V_{BATT} - 1.2\text{V}$ typ.
8	SWT	SWT is ignored.
9	MR	MR is ignored.
10	LOWLINE	Logic low*
11	WDI	WDI is ignored, and goes high impedance.
12	CE OUT	Logic high. The open-circuit output voltage is equal to V_{OUT} .
13	CE IN	High impedance
14	WDO	Logic high. The open-circuit output voltage is equal to V_{OUT} .
15	RESET	Logic low*
16	WDPO	Logic high. The open-circuit output voltage is equal to V_{OUT} .

* V_{CC} must be below the reset threshold to enter battery-backup mode.

use LOWLINE to generate the NMI. The LOWLINE threshold is typically 150mV above the reset threshold (see LOWLINE Output section).

Battery-Backup Mode

The MAX791 requires two conditions to switch to battery-backup mode: 1) V_{CC} must be below the reset threshold; 2) V_{CC} must be below V_{BATT} . Table 1 lists the status of the inputs and outputs in battery-backup mode.

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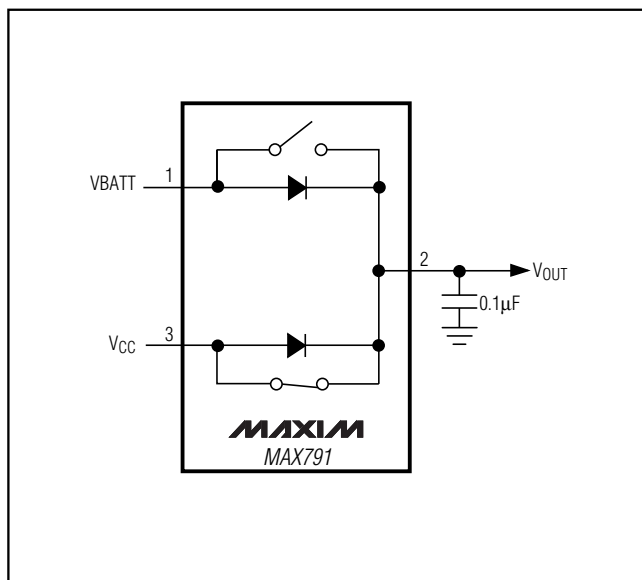


Figure 10. VCC and VBATT-to-VOUT Switch

Battery On Output

The Battery On (BATT ON) output indicates the status of the internal VCC/battery-switchover comparator, which controls the internal VCC and VBATT switches. For VCC greater than VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from VOUT. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The Input Supply Voltage (VCC) should be a regulated +5V. VCC connects to VOUT via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each (Figure 10). The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

Backup-Battery Input

The Backup-Battery Input (VBATT) is similar to VCC, except the PMOS switch and parallel diode are much smaller. Accordingly, the on-resistances of the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The

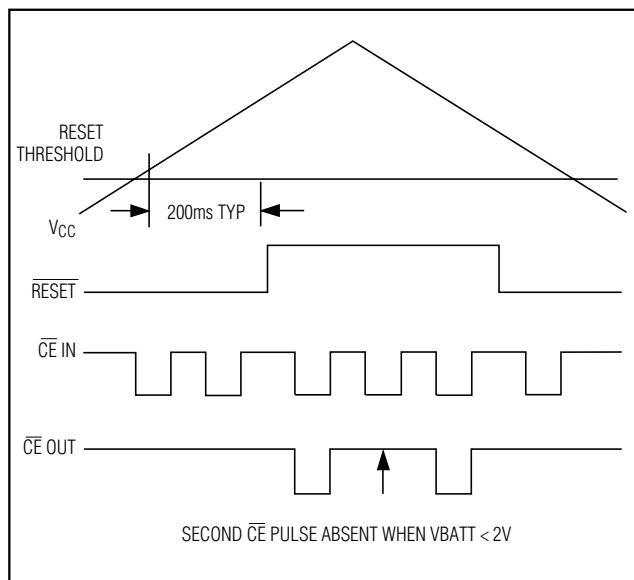


Figure 11. Backup-Battery Monitor Timing Diagram

reverse leakage of this input is less than 1µA over temperature and supply voltage.

Output Supply Voltage

The Output Supply Voltage (VOUT) is internally connected to the substrate of the IC and supplies all the current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the VOUT voltage in their high states rather than the VCC voltage. At the maximum source current of 250mA, VOUT will typically be 200mV below VCC. Decouple this terminal with a 0.1µF capacitor.

Low-Battery Monitor

The MAX791 low-battery voltage function monitors VBATT. Low-battery detection of 2.0V ±0.15V is monitored only during the reset-timeout period (200ms) that occurs either after a normal power-up sequence or after the MR reset input has been returned to its high state. If the battery voltage is below 2.0V, the second CE pulse is inhibited after reset timeout. If the battery voltage is above 2.0V, all CE pulses are allowed through the CE gate after the reset timeout period. To use this function, after the 200ms reset delay, write 00 (HEX) to a location using the first CE pulse, and write FF (HEX) to the same location using the second CE pulse following RESET going inactive on power-up. The contents of the memory then indicates a good battery (FF) or a low battery (00) (Figure 11).

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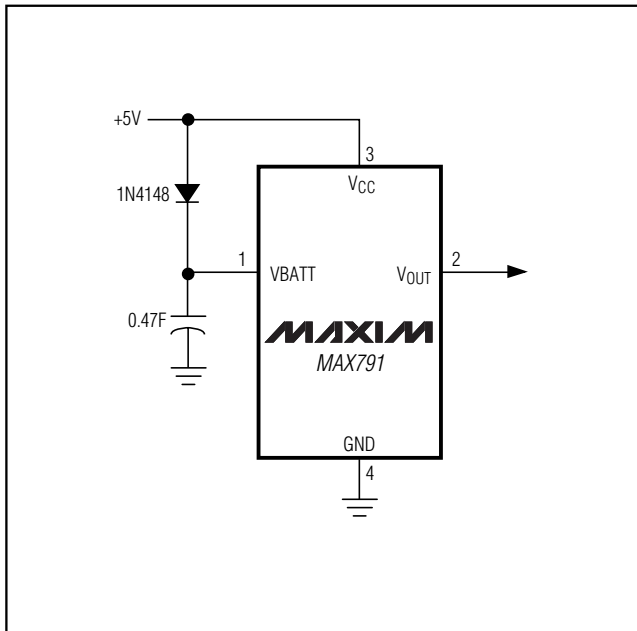


Figure 12. SuperCap or MaxCap on VBATT

Applications Information

The MAX791 is not short-circuit protected. Shorting VOUT to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between VOUT and GND rather than VCC and GND.

If long leads connect to the chip inputs, ensure that these lines are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

- 1) Normal operating mode with all circuitry powered up. Typical supply current from VCC is 60μA, while only leakage currents flow from the battery.
- 2) Battery-backup mode where VCC is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than 60μA.
- 3) Battery-backup mode where VCC is less than VBATT by at least 0.7V. VBATT supply current is less than 1μA max.

Using SuperCaps or MaxCaps with the MAX791

VBATT has the same operating voltage range as VCC, and the battery-switchover threshold voltages are typi-

cally $\pm 30\text{mV}$ centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 12).

If VCC is above the reset threshold and VBATT is 0.5V above VCC, current flows to VOUT and VCC from VBATT until the voltage at VBATT is less than 0.5V above VCC. For example, with a SuperCap connected to VBATT and through a diode to VCC, if VCC quickly changes from 5.4V to 4.9V, the capacitor discharges through VOUT and VCC until VBATT reaches 5.3V typ. Leakage current through the SuperCap charging diode and MAX791 internal power diode eventually discharges the SuperCap to VCC. Also, if VCC and VBATT start from 0.5V above the reset threshold and power is lost at VCC, the SuperCap on VBATT discharges through VCC until VBATT reaches the reset threshold; the MAX791 then switches to battery-backup mode and the current through VCC goes to zero (Figure 10).

Using Separate Power Supplies for VBATT and VCC

If using separate power supplies for VCC and VBATT, VBATT must be less than 0.3V above VCC when VCC is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at VCC, current flows continuously from VBATT to VCC via the VBATT-to-VOUT diode and the VOUT-to-VCC switch until the circuit is broken (Figure 10).

Alternative Chip-Enable Gating

Using memory devices with CE and $\overline{\text{CE}}$ inputs allows the MAX791 CE loop to be bypassed. To do this, connect CE IN to ground, pull up CE OUT to VOUT, and connect CE OUT to the CE input of each memory device (Figure 13). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated by the MAX791.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 14 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 so that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1μA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the PFO pin. Capacitor C1 adds additional noise rejection.

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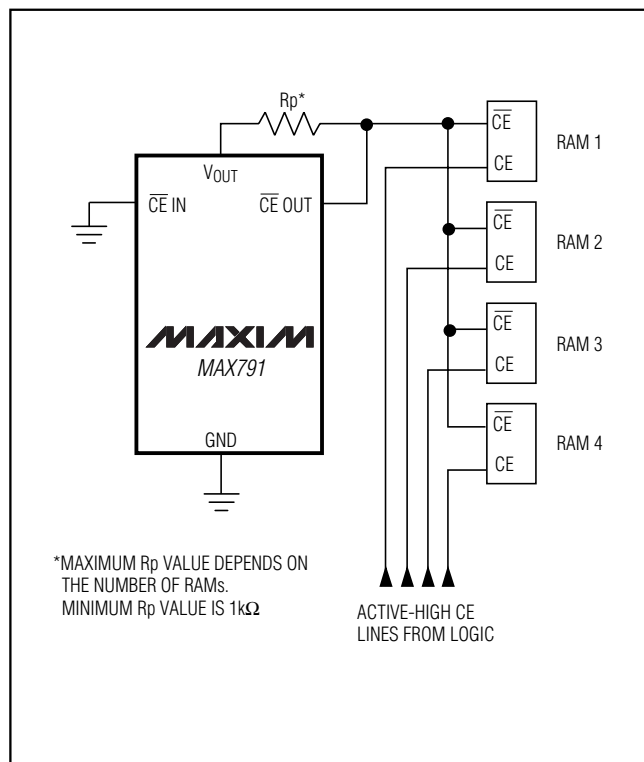


Figure 13. Alternate CE Gating

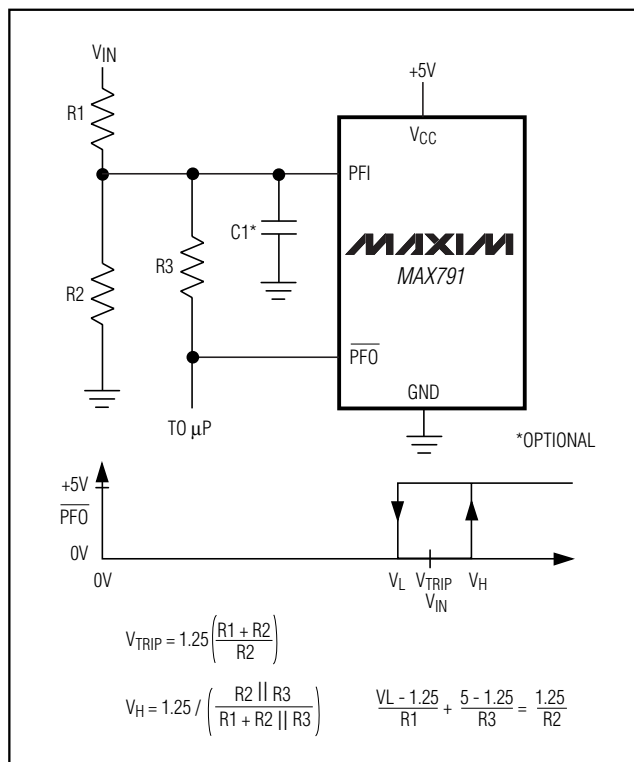


Figure 14. Adding Hysteresis to the Power-Fail Comparator

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 15's circuit. When the negative supply is valid, PFO is low. When the negative supply voltage drops, PFO goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

Backup-Battery Replacement

The backup battery may be disconnected while VCC is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

Negative-Going VCC Transients

While issuing resets to the μ P during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going VCC transients (glitches). It is usually undesirable to reset the μ P when VCC experiences only small glitches.

Figure 16 shows maximum transient duration vs. reset comparator overdrive, for which reset pulses are not generated. The graph was produced using negative-

going VCC pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width that a negative-going VCC transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a VCC transient that goes 100mV below the reset threshold and lasts for 40 μ s or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the VCC pin provides additional transient immunity.

Connecting a Timing Capacitor to SWT

SWT is internally connected to a $\pm$ 100nA current source. When a capacitor is connected from SWT to ground (to select an alternative watchdog-timeout period), the current source charges and discharges the timing capacitor to create the oscillator that controls the watchdog-timeout period. To prevent timing errors or oscillator start-up problems, minimize external current leakage sources at this pin, and locate the capacitor as

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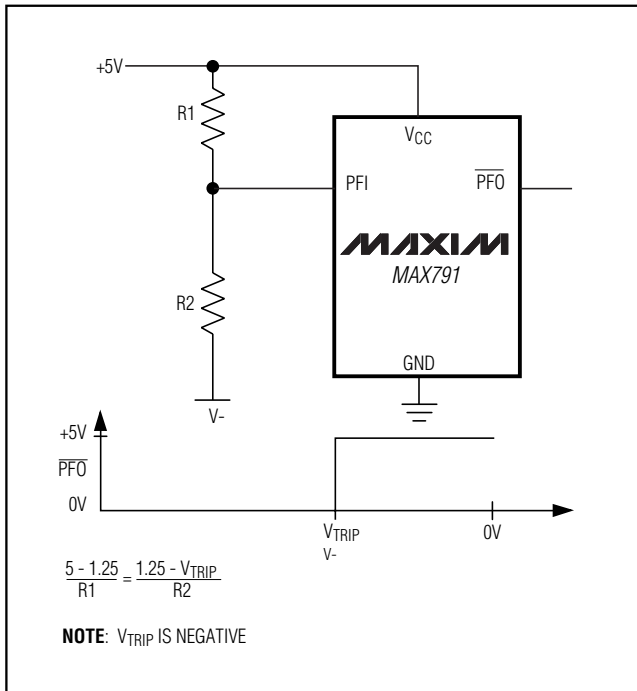


Figure 15. Monitoring a Negative Voltage

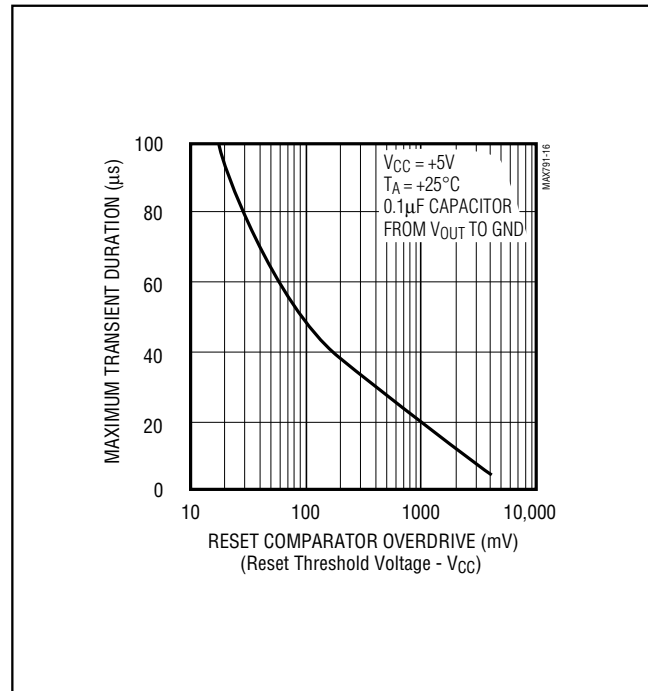


Figure 16. Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

close to SWT as possible. The sum of PC board leakage + SWT capacitor leakage must be small compared to $\pm 100nA$.

Watchdog Software Considerations

A way to help the watchdog timer keep a closer watch on software execution involves setting and resetting the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 17 shows an example flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the pro-

gram returns to the beginning. If the program should "hang" in any subroutine, the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

Maximum VCC Fall Time

The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed $0.03V/\mu s$. A standard rule of thumb for filter capacitance on most regulators is on the order of $100\mu F$ per amp of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse or $1A / 100\mu F = 0.01V/\mu s$. The V_{CC} fall rate decreases with time as V_{CC} falls exponentially, which more than satisfies the maximum fall-time requirement.

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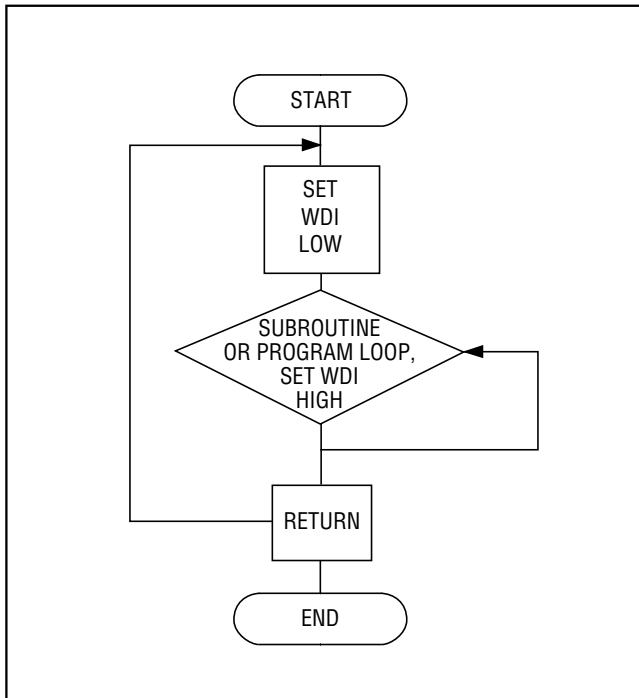
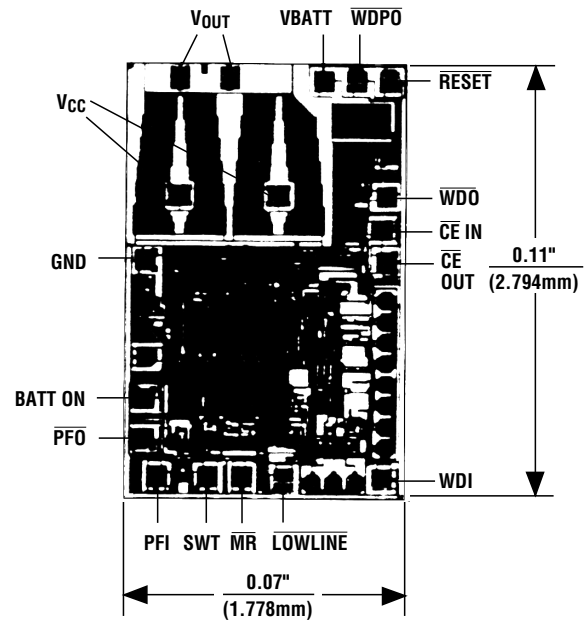


Figure 17. Watchdog Flow Diagram

Chip Topography



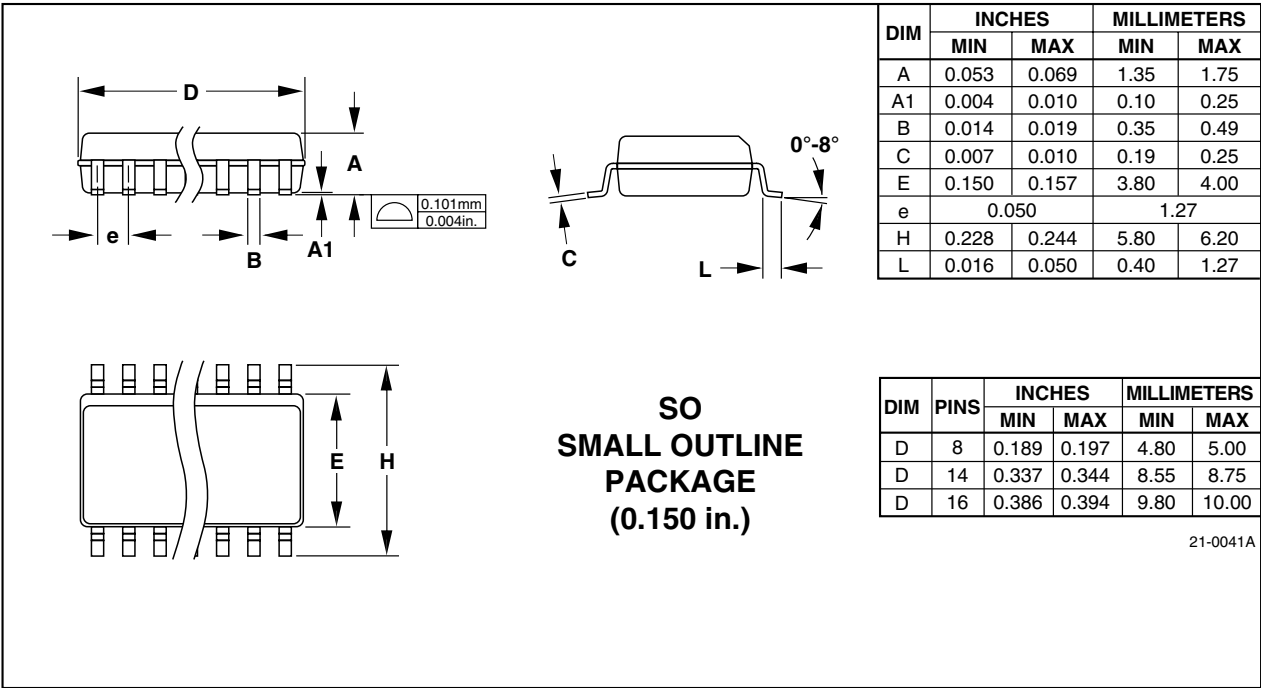
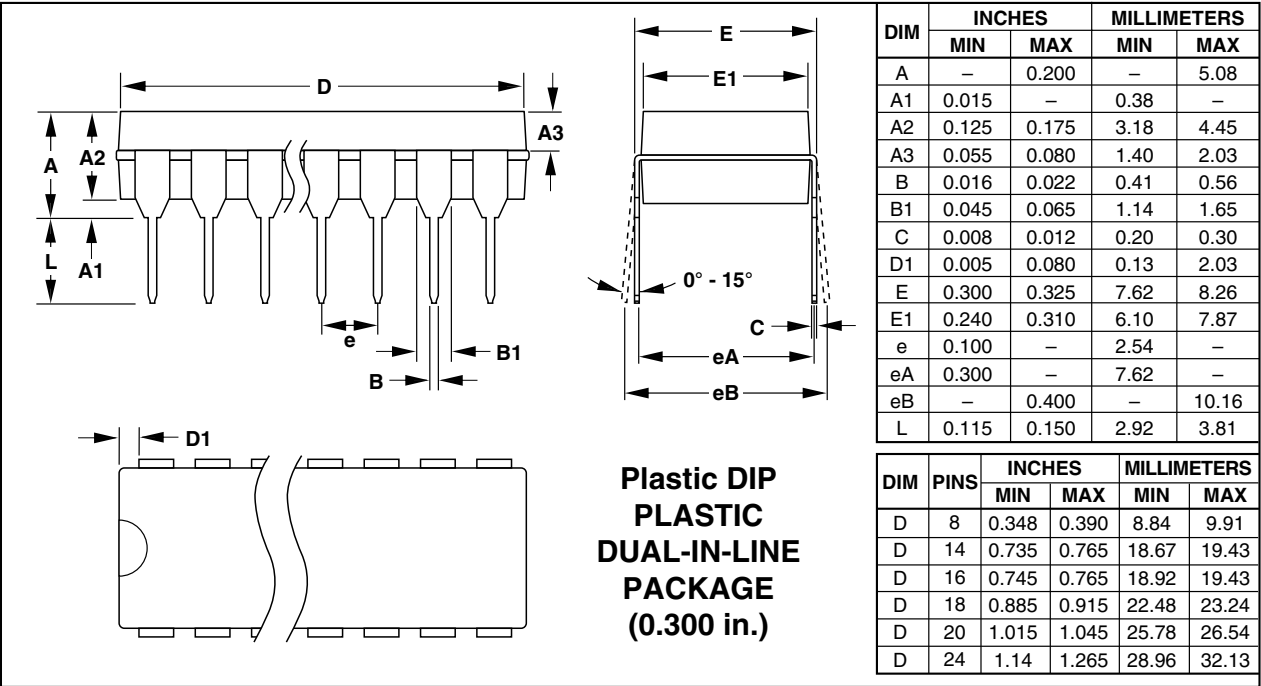
MAX791

TRANSISTOR COUNT: 729
SUBSTRATE CONNECTED TO V_{OUT}

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



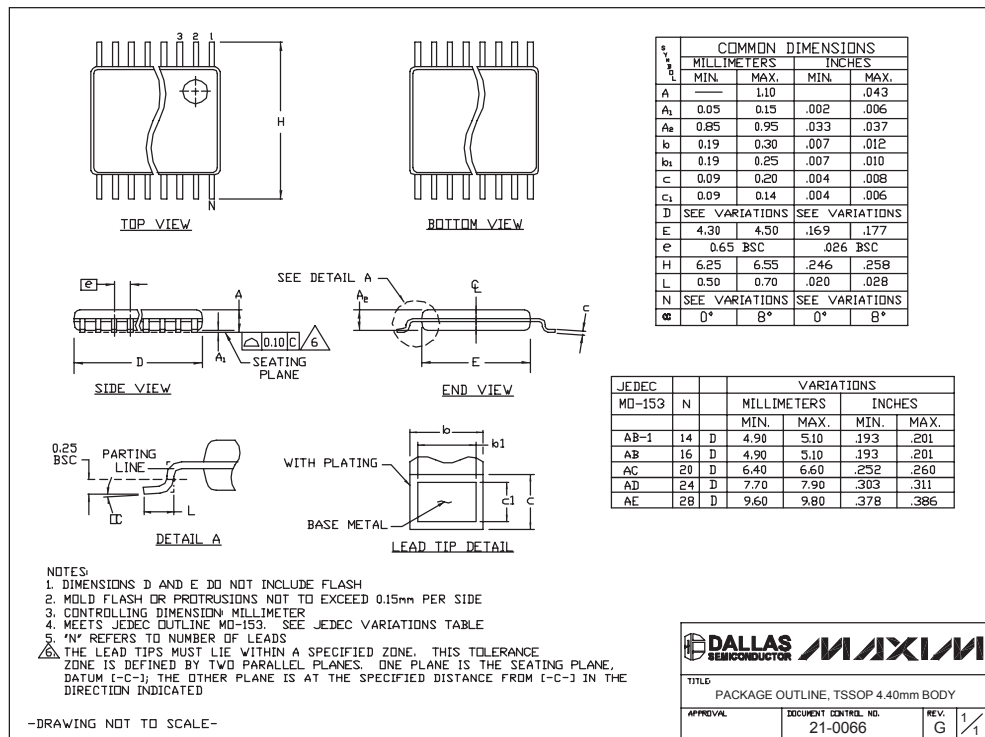
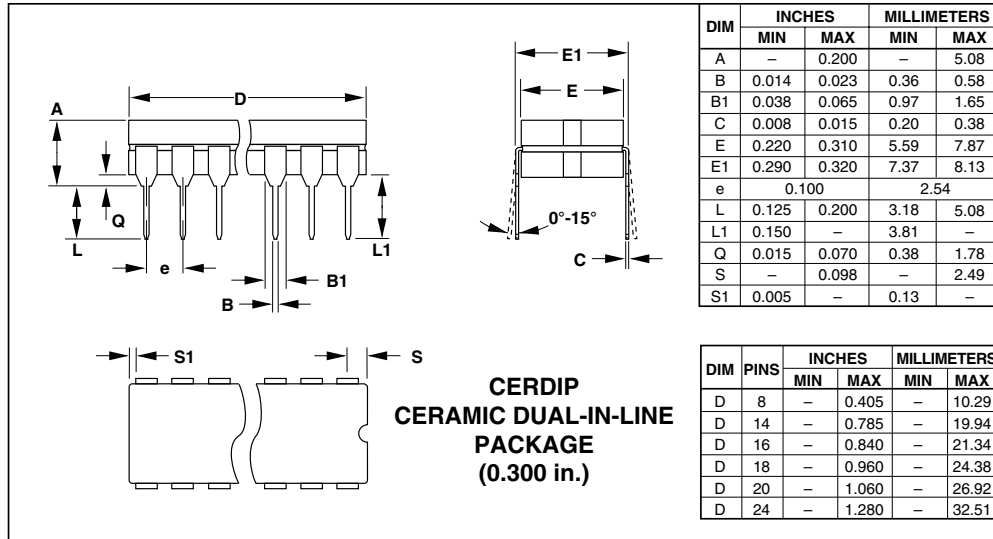
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Microprocessor Supervisory Circuit

Package Information (continued)

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MAX791



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