+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +7.0V
RESET IN, SWT, SRT ..... -0.3V to (V_{CC} + 0.3V)
WDI, WDS ..... -0.3V to +7.0V
RESET, $\overline{RESET}$
  MAX6301… ..... -0.3V to +7.0V
  MAX6302/MAX6303/MAX6304 ..... -0.3V to (V_{CC} + 0.3V)
Input Current
  V_{CC} ..... ±20mA
  GND ..... ±20mA
Output Current
  RESET, $\overline{RESET}$ ..... ±20mA

Continuous Power Dissipation (T_A = +70°C)
  PDIP (derate 9.09mW/°C above +70°C) 727mW
  SO (derate 5.88mW/°C above +70°C) 471mW
  µMAX (derate 4.10mW/°C above +70°C) 330mW
Operating Temperature Range
  MAX630_C_A ..... 0°C to +70°C
  MAX630_E_A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow)
  Lead(Pb)-free ..... +260°C
  Containing Lead (Pb) ..... +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 1)	V_{CC}	MAX6301C/MAX6303C	1.00		5.50	V
		MAX6301E/MAX6303E	1.20		5.50	
		MAX6302/MAX6304	1.31		5.50	
Supply Current (Note 2)	I_{CC}	No load		4.0	7.0	µA
RESET TIMER						
Reset Input Threshold Voltage	V_{TH}	$V_{RESET\ IN}$ falling, V_{CC} = 5.0V	1.195	1.220	1.245	V
		$V_{RESET\ IN}$ rising, V_{CC} = 5.0V		1.240	1.265	
Reset Input Hysteresis	V_{HYST}			20		mV
Reset Input Leakage Current	$I_{RESET\ IN}$			±0.01	±1	nA
Reset Output-Voltage High (MAX6302/MAX6303/MAX6304)	V_{OH}	V_{CC} ≥ 4.5V, I_{SOURCE} = 0.8mA	V_{CC} - 0.4			V
		V_{CC} = 2V, I_{SOURCE} = 0.4mA		V_{CC} - 0.4		
		MAX6302/MAX6304, V_{CC} = 1.31V, R_L = 10kΩ	V_{CC} - 0.3			
Reset Output-Voltage Low (MAX6301/MAX6303/MAX6304	V_{OL}	V_{CC} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	V
		V_{CC} = 2V, I_{SINK} = 1.6mA			0.4	
		MAX6301/MAX6303: V_{CC} = 1V, I_{SINK} = 50µA, T_A = 0°C to +70°C			0.3	
		MAX6301/MAX6303: V_{CC} = 1.2V, I_{SINK} = 100µA, T_A = -40°C to +85°C			0.3	
V_{CC} to Reset Delay	t_{RD}	V_{CC} = falling at 1mV/µs		63		µs
Reset Input Pulse Width	t_{RI}	Comparator overdrive = 50mV		26		µs
Reset Timeout Period (Note 3)	t_{RP}	C_{SRT} = 1500pF	2.8	4.0	5.2	ms
Reset Output Leakage Current		MAX6301, $V_{\overline{RESET}}$ = V_{CC}			±1	µA
		MAX6302, V_{RESET} = V_{GND}			±1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

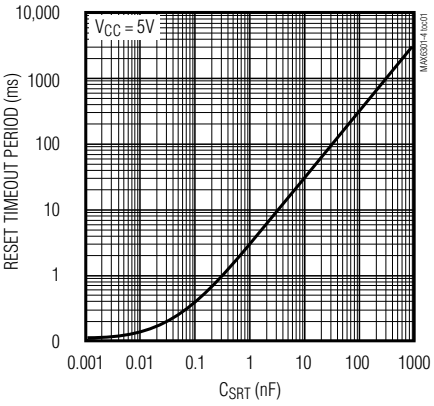
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG TIMER						
WDI, WDS Input Threshold	V_{IH}		0.7 x V_{CC}			V
	V_{IL}				0.3 x V_{CC}	
WDI Pulse Width	t_{WP}	V_{CC} = 4.5V to 5.5V	30			ns
		V_{CC} = 2V to 4.5V	60			
WDI, WDS Leakage Current		Extended mode disabled			±1	µA
WDI Sink/Source Current (Note 4)		Extended mode enabled		±70		µA
Watchdog Timeout Period (Note 3)	t_{WD}	WDS = GND, C_{SWT} = 1500pF	2.8	4.0	5.2	ms
		WDS = V_{CC}, C_{SWT} = 1500pF	1.4	2.0	2.6	s

Note 1: Reset is guaranteed valid from the selected reset threshold voltage down to the minimum V_{CC}.
Note 2: WDS = V_{CC}, WDI unconnected.
Note 3: Precision timing currents of 500nA are present at both the SRT and SWT pins. Timing capacitors connected to these nodes must have low leakage consistent with these currents to prevent timing errors.
Note 4: The sink/source is supplied through a resistor, and is proportional to V_{CC} (Figure 8). At V_{CC} = 2V, it is typically ±24µA.

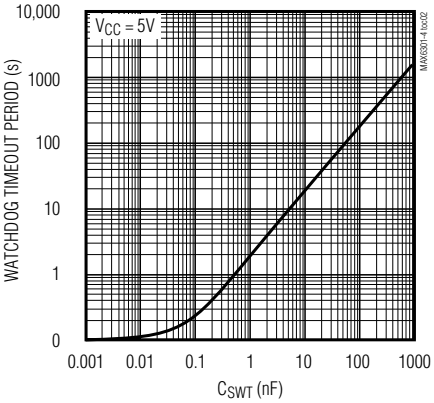
Typical Operating Characteristics

(C_{SWT} = C_{SRT} = 1500pF, T_A = +25°C, unless otherwise noted.)

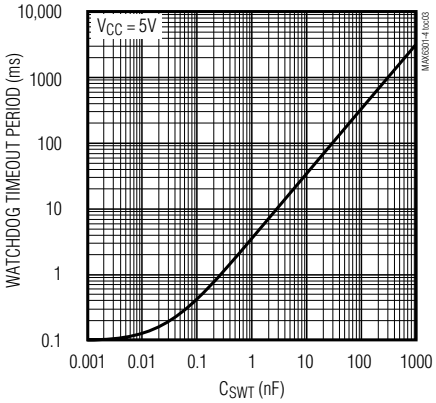
RESET TIMEOUT PERIOD vs. C_{SRT}



EXTENDED-MODE WATCHDOG TIMEOUT PERIOD vs. C_{SWT} (WDS = V_{CC})



NORMAL-MODE WATCHDOG TIMEOUT PERIOD vs. C_{SWT} (WDS = GND)



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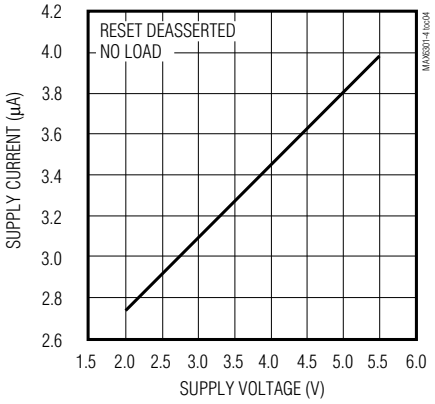
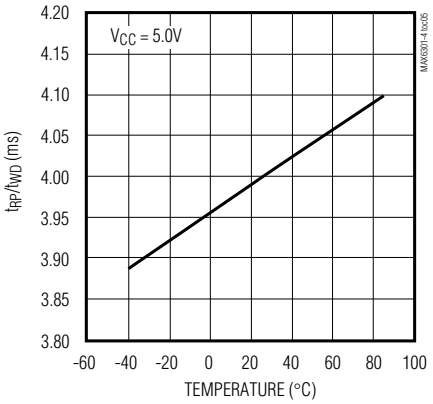
Typical Operating Characteristics (continued)

(C_{SWT} = C_{SRT} = 1500pF, T_A = +25°C, unless otherwise noted.)

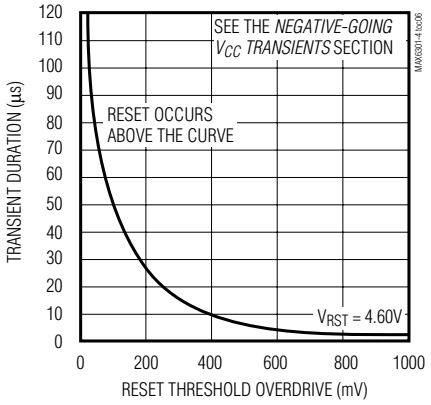
SUPPLY CURRENT vs. SUPPLY VOLTAGE



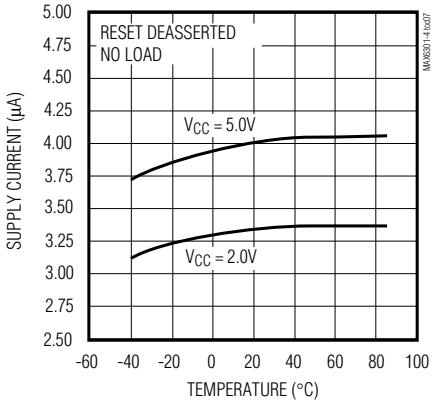
RESET AND NORMAL-MODE WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



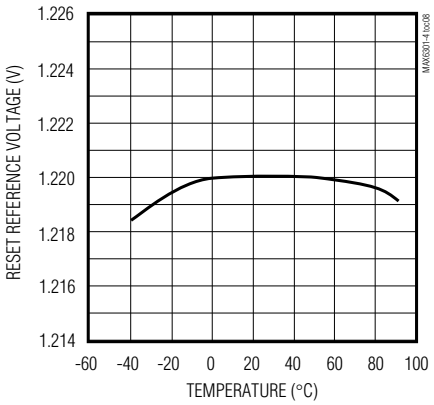
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE (V_{RST})



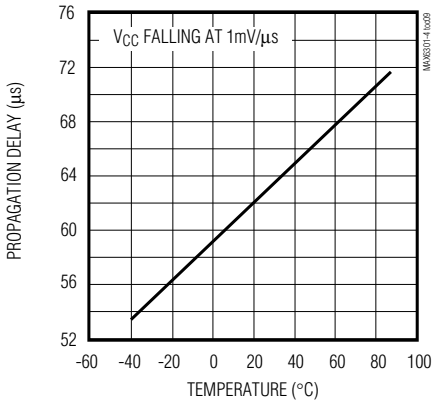
SUPPLY CURRENT vs. TEMPERATURE



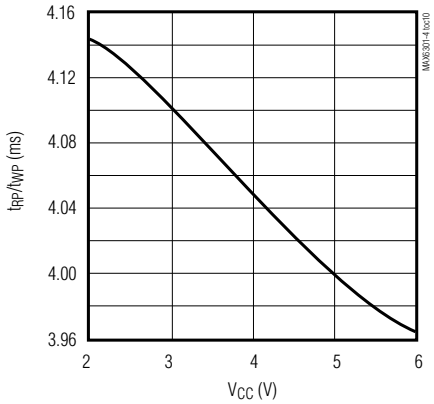
RESET IN THRESHOLD VOLTAGE vs. TEMPERATURE



V_{CC} TO RESET DELAY vs. TEMPERATURE (V_{CC} FALLING)



RESET AND WATCHDOG TIMEOUT vs. SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION	
1	RESET IN	Reset Input. High-impedance input to the reset comparator. Connect this pin to the center point of an external resistor voltage-divider network to set the reset threshold voltage. The reset threshold voltage is calculated as follows: V_{RST} = 1.22 x (R1 + R2)/R2 (see the *Typical Operating Circuit*).	
2	GND	Ground	
3	SRT	Set Reset-Timeout Input. Connect a capacitor between this input and ground to select the reset timeout period (t_{RP}). Determine the period as follows: t_{RP} = 2.67 x C_{SRT}, with C_{SRT} in pF and t_{RP} in µs (see the *Typical Operating Circuit*).	
4	SWT	Set Watchdog-Timeout Input. Connect a capacitor between this input and ground to select the basic watchdog timeout period (t_{WD}). Determine the period as follows: t_{WD} = 2.67 x C_{SWT}, with C_{SWT} in pF and t_{WD} in µs. The watchdog function can be disabled by connecting this pin to ground.	
5	WDS	Watchdog-Select Input. This input selects the watchdog mode. Connect to ground to select normal mode and the basic watchdog timeout period. Connect to V_{CC} to select extended mode, multiplying the basic timeout period by a factor of 500. A change in the state of this pin resets the watchdog timer to zero.	
6	WDI	Watchdog Input. A rising or falling transition must occur on this input within the selected watchdog timeout period, or a reset pulse will occur. The capacitor value selected for SWT and the state of WDS determine the watchdog timeout period. The watchdog timer clears and restarts when a transition occurs on WDI or WDS. The watchdog timer is cleared when reset is asserted and restarted after reset deasserts. In the extended watchdog mode (WDS = V_{CC}), the watchdog function can be disabled by driving WDI with a three-stated driver or by leaving WDI unconnected.	
7	$\overline{\text{RESET}}$ (MAX6301/ MAX6303)	Open-Drain, Active-Low Reset Output (MAX6301)	$\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage (V_{IN}) drops below the selected reset threshold (V_{RST}). $\overline{\text{RESET}}$ remains low as long as V_{IN} is below V_{RST}. Once V_{IN} exceeds V_{RST}, $\overline{\text{RESET}}$ remains low for the reset timeout period and then goes high. The watchdog timer triggers a reset pulse (t_{RP}) whenever the watchdog timeout period (t_{WD}) is exceeded.
		Push-Pull, Active-Low Reset Output (MAX6303)	
	RESET (MAX6302/ MAX6304	Open-Drain, Active-High Reset Output (MAX6302)	RESET changes from low to high whenever the monitored voltage (V_{IN}) drops below the selected reset threshold (V_{RST}). RESET remains high as long as V_{IN} is below V_{RST}. Once V_{IN} exceeds V_{RST}, RESET remains high for the reset timeout period and then goes low. The watchdog timer triggers a reset pulse (t_{RP}) whenever the watchdog timeout period (t_{WD}) is exceeded.
		Push-Pull, Active-High Reset Output (MAX6304)	
8	V_{CC}	Supply Voltage. Bypass to ground with a 0.1µF capacitor placed as close as possible to the pin.	

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Detailed Description

Reset Function/Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. The MAX6301–MAX6304 µP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Operating Circuit*).

For the MAX6301/MAX6303, $\overline{RESET}$ changes from high to low whenever the monitored voltage (V_{IN}) drops below the reset threshold voltage (V_{RST}). $\overline{RESET}$ remains low as long as V_{IN} is below V_{RST}. Once V_{IN} exceeds V_{RST}, $\overline{RESET}$ remains low for the reset timeout period, then goes high. When a reset is asserted due to a watchdog timeout condition, $\overline{RESET}$ stays low for the reset timeout period. Any time reset asserts, the watchdog timer clears. At the end of the reset timeout period, $\overline{RESET}$ goes high and the watchdog timer is restarted from zero. If the watchdog timeout period is exceeded again, then $\overline{RESET}$ goes low again. This cycle continues unless WDI receives a transition.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic-low. For information about applications where V_{CC} is less than 1V, see the *Ensuring a Valid $\overline{RESET}$/RESET Output Down to V_{CC} = 0V (MAX6303/MAX6304)* section. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{IN} rises above V_{RST}, the reset timer starts and $\overline{RESET}$ remains low. When the reset timeout period ends, $\overline{RESET}$ goes high.

On power-down, once V_{IN} goes below V_{RST}, $\overline{RESET}$ goes low and is guaranteed to be low until V_{CC} drops below 1V. For information about applications where V_{CC} is less than 1V, see the *Ensuring a Valid $\overline{RESET}$/RESET Output Down to V_{CC} = 0V (MAX6303/MAX6304)* section.

The MAX6302/MAX6304 active-high RESET output is the inverse of the MAX6301/MAX6303 active-low $\overline{RESET}$ output, and is guaranteed valid for V_{CC} > 1.31V.

Reset Threshold

These supervisors monitor the voltage on RESET IN. The MAX6301–MAX6304 have an adjustable reset threshold voltage (V_{RST}) set with an external resistor voltage-divider (Figure 1). Use the following formula to calculate V_{RST} (the point at which the monitored voltage triggers a reset):

$$V_{RST} = \frac{V_{TH} \times (R1 + R2)}{R2} \ (V)$$

where V_{RST} is the desired reset threshold voltage and V_{TH} is the reset input threshold (1.22V). Resistors R1 and R2 can have very high values to minimize current consumption. Set R2 to some conveniently high value (1MΩ, for example) and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2 \times \left(\frac{VRST}{V_{TH}} - 1 \right) (\Omega)$$

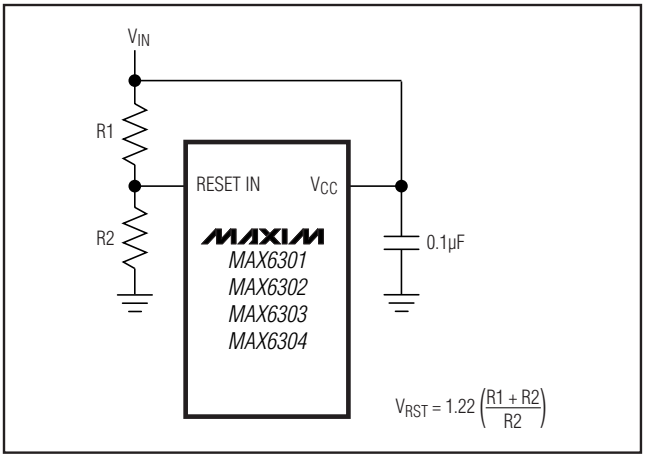

Figure 1. Calculating the Reset Threshold Voltage (V_{RST})

Watchdog Timer

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within t_{WD} (user selected), reset asserts. The internal watchdog timer is cleared by reset, by a transition at WDI (which can detect pulses as short as 30ns), or by a transition at WDS. The watchdog timer remains cleared while reset is asserted; as soon as reset is released, the timer starts counting (Figure 2).

The MAX6301–MAX6304 feature two modes of watchdog timer operation: normal mode and extended mode. In normal mode (WDS = GND), the watchdog timeout period is determined by the value of the capacitor connected between SWT and ground (see the *Selecting the Reset and Watchdog Timeout Capacitor* section). In extended mode (WDS = V_{CC}), the watchdog timeout period is multiplied by 500. For example, in the extended mode, a 1µF capacitor gives a watchdog timeout period of 22 minutes (see the Extended-Mode Watchdog Timeout Period vs. C_{SWT} graph in the *Typical Operating Characteristics*).

In extended mode, the watchdog function can be disabled by leaving WDI unconnected or by three-stating the driver connected to WDI. In this mode, the watchdog input is internally driven low during the watchdog timeout period, then momentarily pulses high, resetting the

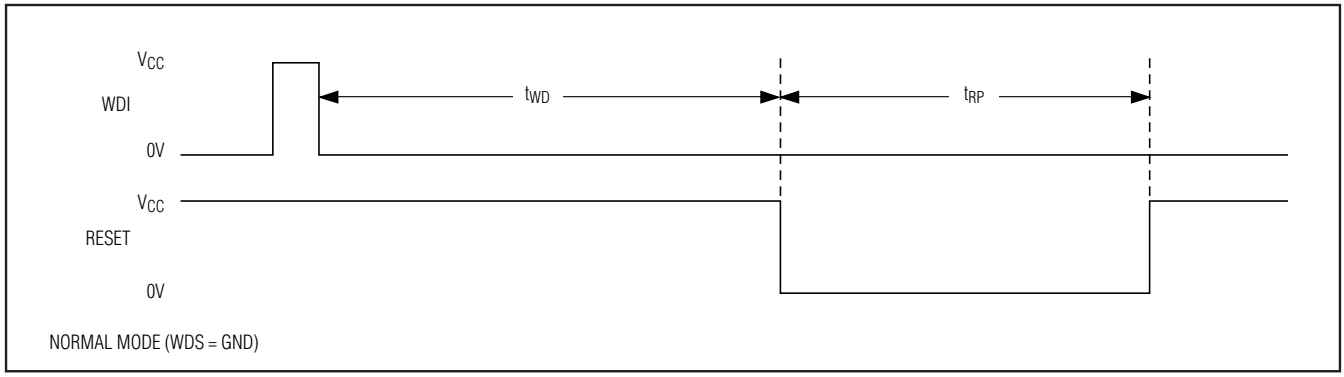

Figure 2a. Watchdog Timing Diagram, WDS = GND

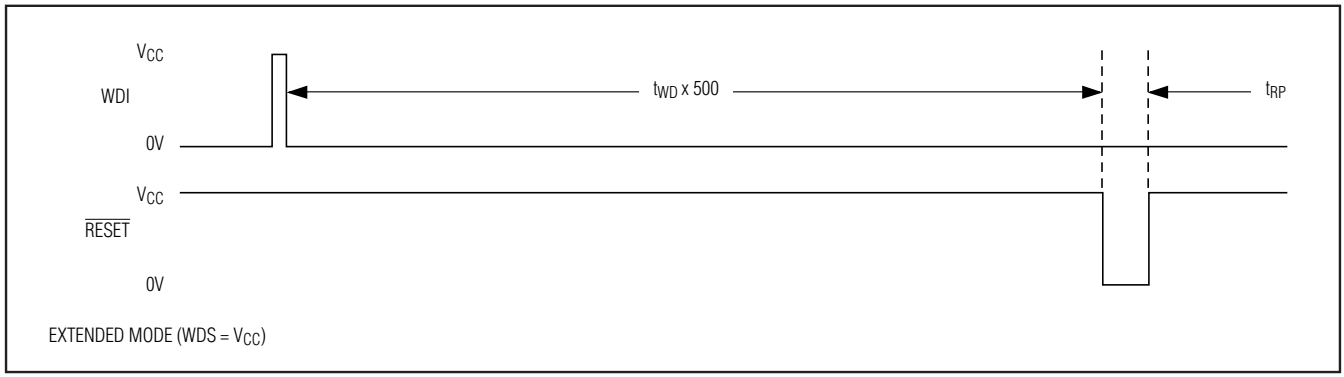

Figure 2b. Watchdog Timing Diagram, WDS = V_{CC}

watchdog counter. When WDI is left unconnected, the watchdog timer is cleared by this internal driver just before the timeout period is reached (the internal driver pulls WDI high at about 94% of t_{WD}). When WDI is three-stated, the maximum allowable leakage current of the device driving WDI is 10µA.

In normal mode (WDS = GND), the watchdog timer cannot be disabled by three-stating WDI. WDI is a high-impedance input in this mode. Do not leave WDI unconnected in normal mode.

Applications Information

Selecting the Reset and Watchdog Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period (t_{RP}) by connecting a specific value capacitor (C_{SRT}) between SRT and ground (Figure 3). Calculate the reset timeout capacitor as follows:

$$C_{SRT} = t_{RP}/2.67$$

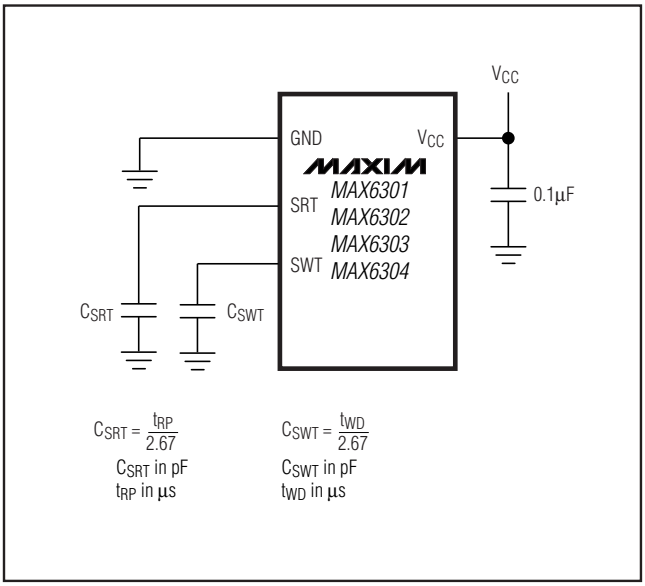

Figure 3. Calculating the Reset (C_{SRT}) and Watchdog (C_{SWT}) Timeout Capacitor Values

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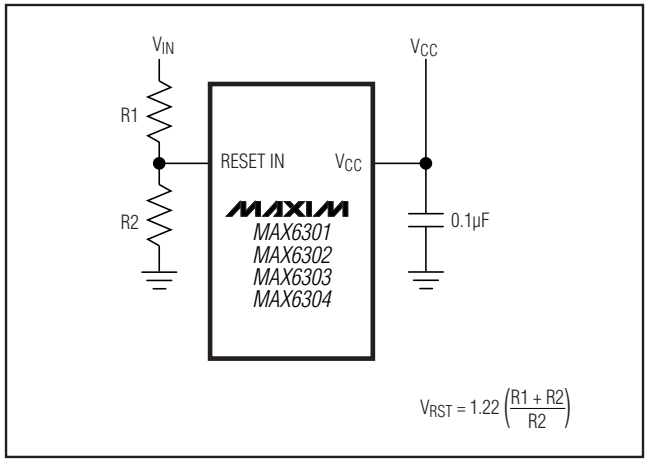

Figure 4. Monitoring Votlages Other than V_{CC}

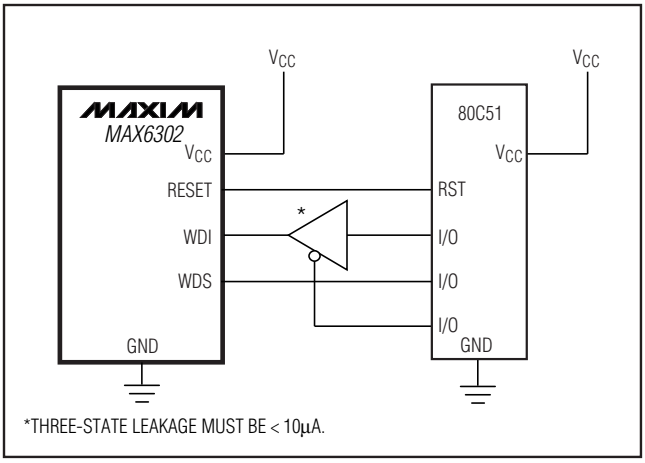

Figure 5. Wake-Up Timer

with C_{SRT} in pF and t_{RP} in µs. C_{SRT} must be a low-leakage (< 10nA) type capacitor. Ceramic is recommended.

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a specific value capacitor (C_{SWT}) between SWT and ground (Figure 3). For normal-mode operation, calculate the watchdog timeout capacitor as follows:

$$C_{SWT} = t_{WD}/2.67$$

where C_{SWT} is in pF and t_{WD} is in µs. C_{SWT} must be a low-leakage (< 10nA) type capacitor. Ceramic is recommended.

Monitoring Voltages Other than Vcc

The *Typical Operating Circuit* monitors V_{CC}. Voltages other than V_{CC} can easily be monitored, as shown in Figure 4. Calculate V_{RST} as shown in the *Reset Threshold* section.

Wake-Up Timer

In some applications, it is advantageous to put a µP into sleep mode, periodically wake it up to perform checks and/or tasks, then put it back into sleep mode. The MAX6301 family of supervisors can easily accommodate this technique. Figure 5 illustrates an example using the MAX6302 and an 80C51.

In Figure 5, just before the µC puts itself into sleep mode, it pulls WDS high. The µC's I/O pins maintain their logic levels while in sleep mode and WDS remains high. This places the MAX6302 in extended mode, increasing the watchdog timeout 500 times. When the watchdog timeout period ends, a reset is applied on the 80C51, waking it up to perform tasks. While the µP is performing tasks, the 80C51 pulls WDS low (selecting normal mode), and the MAX6302 monitors the µP for hang-ups. When the µP finishes its tasks, it puts itself back into sleep mode, drives WDS high, and starts the cycle over again. This is a power-saving technique, since the µP is operating only part of the time and the MAX6302 has very low quiescent current.

Adding a Manual Reset Function

A manual reset option can easily be implemented by connecting a normally open momentary switch in parallel with R2 (Figure 6). When the switch is closed, the voltage on RESET IN goes to zero, initiating a reset. When the switch is released, the reset remains asserted for the reset timeout period and then is cleared. The pushbutton switch is effectively debounced by the reset timer.

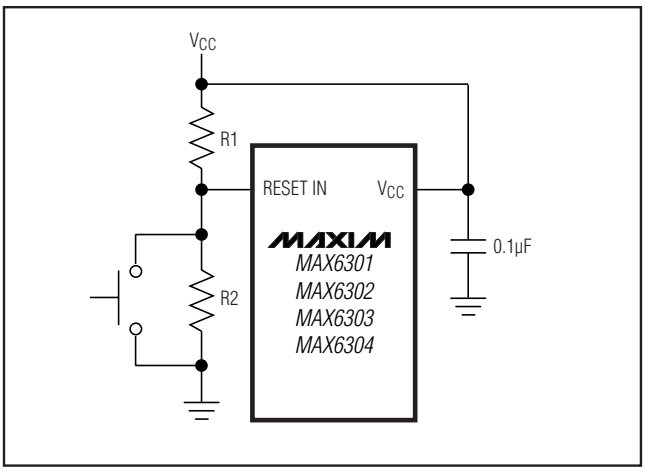

Figure 6. Adding a Manual Reset Function

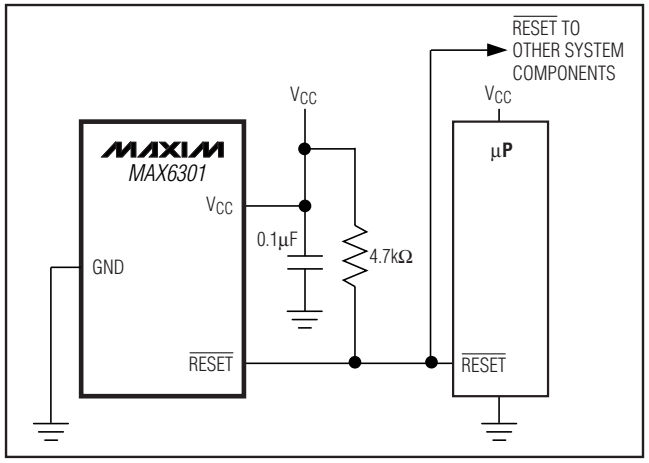

Figure 7. Interfacing to µPs with Bidirectional Reset I/O Pins

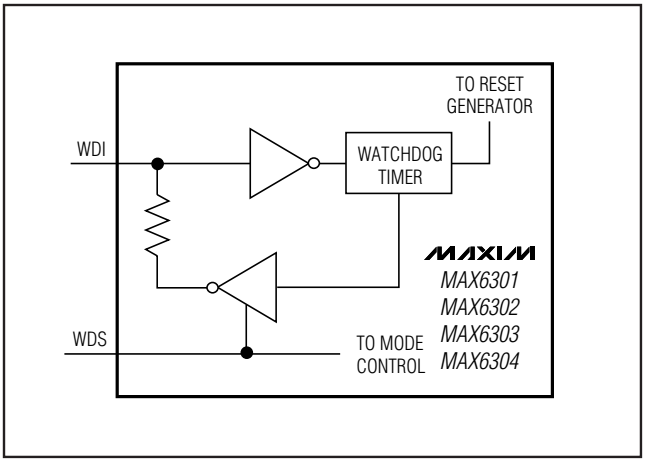

Figure 8. Watchdog Input Structure

Interfacing to µPs with Bidirectional Reset Pins

Since $\overline{\text{RESET}}$ is open-drain, the MAX6301 interfaces easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11 (Figure 7). Connecting $\overline{\text{RESET}}$ directly to the µP's reset pin with a single pullup allows either device to assert reset.

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going transients (glitches). The Maximum Transient Duration vs. Reset Threshold Overdrive graph in the *Typical Operating Characteristics* shows this relationship.

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{IN}, starting above the actual reset threshold (V_{RST}) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient increases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50µs or less will not cause a reset pulse to be issued.

Watchdog Input Current

Extended Mode

In extended mode (WDS = V_{CC}), the WDI input is internally driven through a buffer and series resistor from the watchdog counter (Figure 8). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a very brief low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low (> 30ns) once within the period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, typically 70µA can flow into WDI.

Normal Mode

In normal mode (WDS = GND), the internal buffer that drives WDI is disabled. In this mode, WDI is a standard CMOS input and leakage current is typically 100pA, regardless of whether WDI is high or low.

Ensuring a Valid $\overline{\text{RESET}}$/RESET Output Down to V_{CC} = 0V (MAX6303/MAX6304)

When V_{CC} falls below 1V, $\overline{\text{RESET}}$/RESET current sinking (sourcing) capabilities decline drastically. In the case of the MAX6303, high-impedance CMOS-logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications, since most µPs and other circuitry do not operate with V_{CC} below 1V.

+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

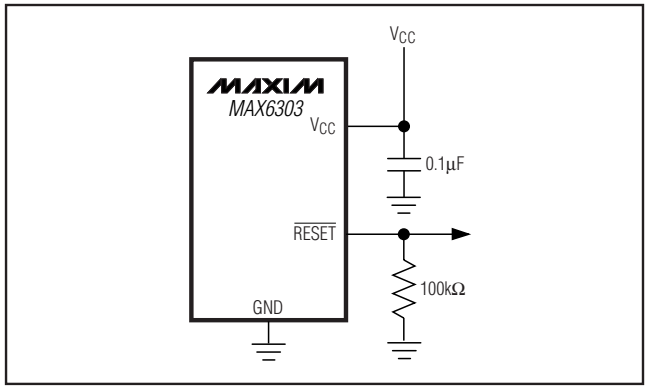

Figure 9. Ensuring $\overline{RESET}$ Valid to V_{CC} = 0V

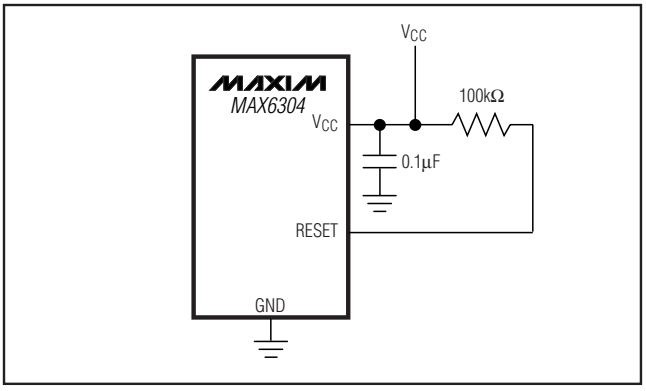

Figure 10. Ensuring RESET Valid to V_{CC} = 0V

In those applications where $\overline{RESET}$ must be valid down to 0V, adding a pulldown resistor between $\overline{RESET}$ and ground sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 9). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. For applications using the MAX6304, a 100kΩ pullup resistor between RESET and V_{CC} will hold RESET high when V_{CC} falls below 1V (Figure 10).

Watchdog-Software Considerations

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out.

Figure 11 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. When using extended mode, as described in the *Watchdog Input Current* section, this scheme does result in higher average WDI input current than does the method of leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

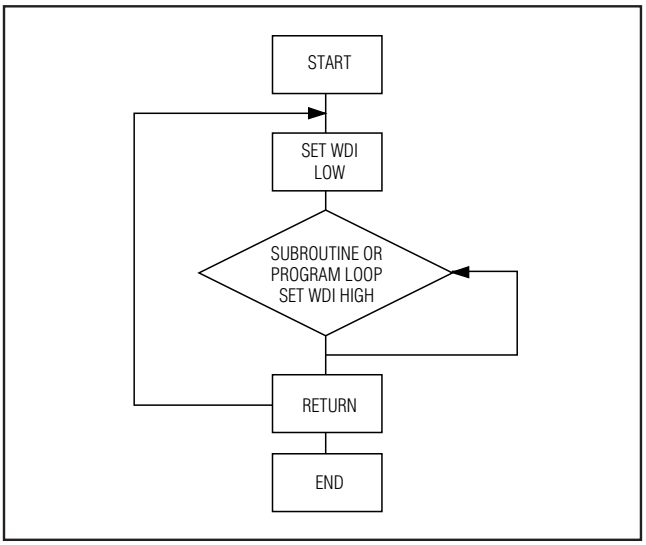

Figure 11. Watchdog Flow Diagram

Layout Considerations

SRT and SWT are precision current sources. When developing the layout for the application, be careful to minimize board capacitance and leakage currents around these pins. Traces connected to these pins should be kept as short as possible. Traces carrying high-speed digital signals and traces with large voltage potentials should be routed as far from these pins as possible. Leakage currents and stray capacitance (e.g., a scope probe) at these pins could cause errors in the reset and/or watchdog timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset and watchdog timeout periods.

RESET IN is a high-impedance input that is typically driven by a high-impedance resistor-divider network (e.g., 1MΩ to 10MΩ). Minimize coupling to transient signals by keeping the connections to this input short. Any DC leakage current at RESET IN (e.g., a scope probe) causes errors in the programmed reset threshold. Note that sensitive pins are located on the GND side of the device, away from the digital I/O, to simplify board layout.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX6302CPA	0°C to +70°C	8 PDIP
MAX6302CSA	0°C to +70°C	8 SO
MAX6302CUA	0°C to +70°C	8 µMAX
MAX6302EPA	-40°C to +85°C	8 PDIP
MAX6302ESA	-40°C to +85°C	8 SO
MAX6303CPA	0°C to +70°C	8 PDIP
MAX6303CSA	0°C to +70°C	8 SO
MAX6303CUA	0°C to +70°C	8 µMAX
MAX6303EPA	-40°C to +85°C	8 PDIP
MAX6303ESA	-40°C to +85°C	8 SO
MAX6304CPA	0°C to +70°C	8 PDIP
MAX6304CSA	0°C to +70°C	8 SO
MAX6304CUA	0°C to +70°C	8 µMAX
MAX6304EPA	-40°C to +85°C	8 PDIP
MAX6304ESA	-40°C to +85°C	8 SO

Devices are available in both leaded and lead(Pb)-free/RoHS-compliant packaging. Specify lead-free by adding the "+" symbol at the end of the part number when ordering.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP	P8-1	21-0043	—
8 SO	S8-2	21-0041	90-0096
8 µMAX	U8-1	21-0036	90-0092

+5V, Low-Power µP Supervisory Circuits with Adjustable Reset/Watchdog

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/96	Initial release	—
1	12/05	Added lead-free notation.	1, 11
2	3/07	Updated *Typical Operating Circuit*.	1
3	3/09	Updated *Pin Description*, *Applications Information*, Figure 3, and *Package Information*.	5, 7, 11
4	9/10	Updated *Absolute Maximum Ratings*, correct part number.	2, 9, 11, 12