

45Ω, SPDT Analog Switch in SOT23-8

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V+	-0.3V to +44.0V
V-	-44.0V to +0.3V
V+ to V-	-0.3V to +44.0V
All Other Pins (Note 1)	(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into any Terminal	±10mA
Continuous Current (COM, NO, NC)	±30mA
Peak Current (COM, NO, NC) (pulsed at 1ms, 10% duty cycle)	±60mA

Continuous Power Dissipation (T _A = +70°C) 8-Pin SOT23 (derate 8.9mW/°C above +70°C)	714mW
Operating Temperature Range MAX4649EKA	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual ±15V Supplies

(V+ = +15V, V- = -15V, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{NO} , V _{NC} , V _{COM}			V-		V+	V
On-Resistance	R _{ON}	I _{COM} = 1mA; V _{NO} or V _{NC} = ±10V	+25°C		33	45	Ω
			T _{MIN} to T _{MAX}			60	
On-Resistance Matching Between Channels	ΔR _{ON}	I _{COM} = 1mA; V _{NO} or V _{NC} = ±10V	+25°C		0.6	5	Ω
			T _{MIN} to T _{MAX}			6	
On-Resistance Flatness (Note 4)	R _{FLAT} (ON)	I _{COM} = 1mA; V _{NO} or V _{NC} = +5V, 0, -5V	+25°C		1.5	7	Ω
			T _{MIN} to T _{MAX}			10	
NO or NC Off-Leakage Current	I _{NO} (OFF) or I _{NC} (OFF)	V _{COM} = -14V, +14V; V _{NO} or V _{NC} = +14V, -14V	+25°C	-2	0.01	2	nA
			T _{MIN} to T _{MAX}	-10		10	
COM On-Leakage Current	I _{COM} (ON)	V _{COM} = +14V, -14V; V _{NO} or V _{NC} = +14V, -14V or floating	+25°C	-4		4	nA
			T _{MIN} to T _{MAX}	-20		20	
DIGITAL I/O							
Input Logic High Voltage	V _{IH}			2.4			V
Input Logic Low Voltage	V _{IL}					0.8	V
Input Leakage	I _{IN}	V _{IN} = 0 or +5V		-1		1	μA

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ELECTRICAL CHARACTERISTICS—Dual ±15V Supplies (continued)

(V₊ = +15V, V₋ = -15V, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Transition Time	t _{TRANS}	V _{NO} or V _{NC} = ±10V; R _L = 1kΩ; C _L = 35pF; Figure 2	+25°C	90	130	ns	
			T _{MIN} to T _{MAX}	170			
Break-Before-Make Delay	t _D	V _{NO} or V _{NC} = ±10V; R _L = 300Ω; C _L = 35pF; Figure 3	+25°C	5	10	ns	
			T _{MIN} to T _{MAX}	2			
Charge Injection	Q	V _{GEN} = 0; R _{GEN} = 0; C _L = 1nF; Figure 4		2		pC	
Off-Isolation	V _{ISO}	f = 1MHz, R _L = 50Ω, C _L = 5pF, V _{COM} = 1V _{RMS} ; Figure 5		92		dB	
Crosstalk		f = 1MHz, R _L = 50Ω, C _L = 5pF; Figure 6		92			
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, R _L = 600Ω, 5V _{RMS}		0.015		%	
V _{NO} or V _{NC} Off-Capacitance	C _{NO(OFF)} , C _{NC(OFF)}	f = 1MHz; Figure 7		6		pF	
COM On-Capacitance	C _{COM(ON)}	f = 1MHz; Figure 8		17		pF	
POWER SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I ₊	V _{IN} = 5V	+25°C	38	75	μA	
			T _{MIN} to T _{MAX}	100			
		V _{IN} = 0 or V ₊	+25°C	0.01	1		
			T _{MIN} to T _{MAX}	10			
Negative Supply Current	I ₋	V _{IN} = 0 or 5V	+25°C	0.01	1	μA	
			T _{MIN} to T _{MAX}	10			

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ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = +12V, V- = 0, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T _A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V _{NO} , V _{NC} , V _{COM}			0		V+	V
On-Resistance	R _{ON}	I _{COM} = 1mA; V _{NO} or V _{NC} = +10V	+25°C	68	90	Ω	
			T _{MIN} to T _{MAX}	115			
On-Resistance Matching Between Channels	ΔR _{ON}	I _{COM} = 1mA; V _{NO} or V _{NC} = +10V	+25°C	0.7	6	Ω	
			T _{MIN} to T _{MAX}	7			
On-Resistance Flatness (Note 4)	R _{FLAT} (ON)	I _{COM} = 1mA; V _{NO} or V _{NC} = +2V, +6V, +10V	+25°C	9	17	Ω	
			T _{MIN} to T _{MAX}	23			
DYNAMIC							
Transition Time	t _{TRANS}	V _{NO} or V _{NC} = 0, 10V or 10V, 0; R _L = 1kΩ; C _L = 35pF; Figure 2	+25°C	116	165	ns	
			T _{MIN} to T _{MAX}	200			
Break-Before-Make Delay	t _D	V _{NO} or V _{NC} = +10V; R _L = 300Ω; C _L = 35pF; Figure 3	+25°C	1	36	ns	
			T _{MIN} to T _{MAX}	1			
Charge Injection	Q	V _{GEN} = 0; R _{GEN} = 0; C _L = 1nF; Figure 4	+25°C	1		pC	
POWER SUPPLY							
Power Supply Range				9		36	V
Positive Supply Current	I ₊	V _{IN} = +5V	+25°C	22	40	μA	
			T _{MIN} to T _{MAX}	50			
		V _{IN} = 0 or V ₊	+25°C	0.01	1		
			T _{MIN} to T _{MAX}	10			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: All parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.

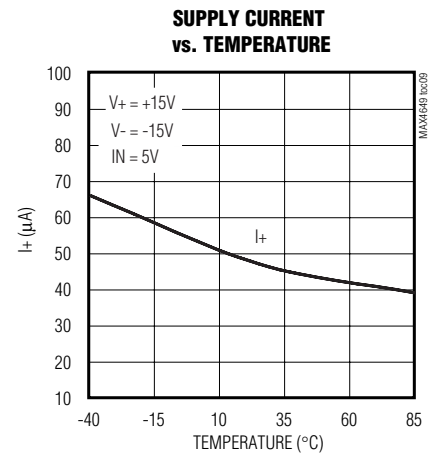
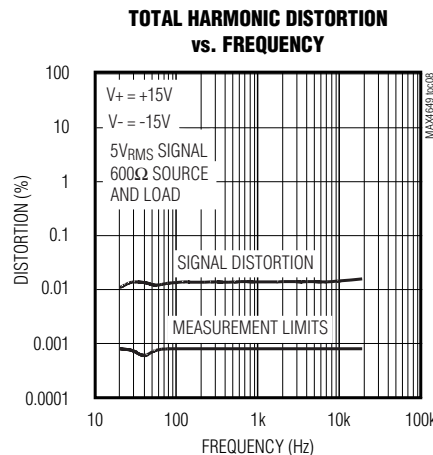
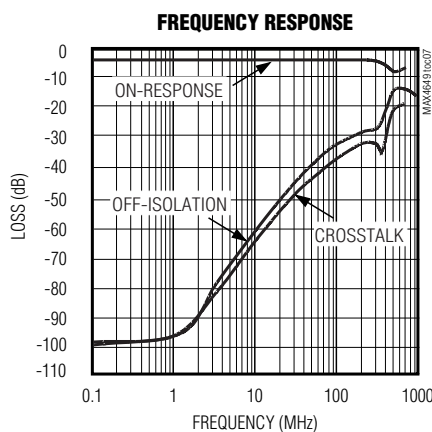
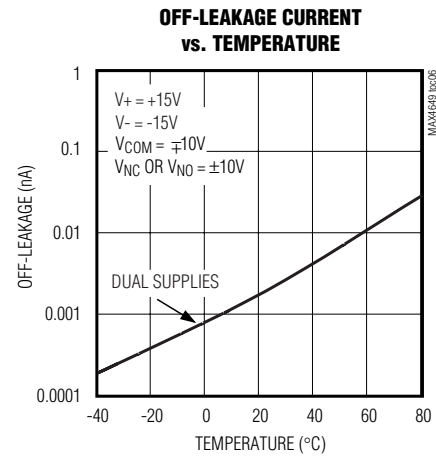
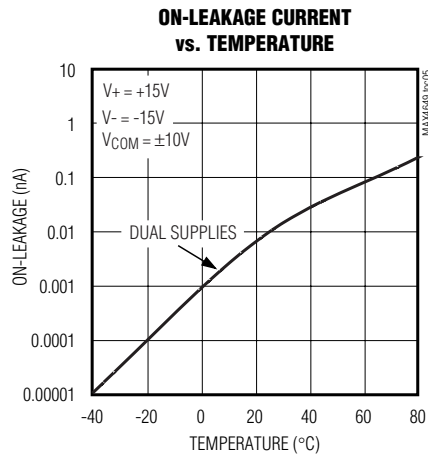
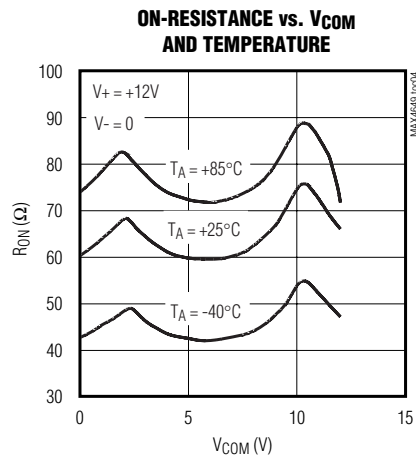
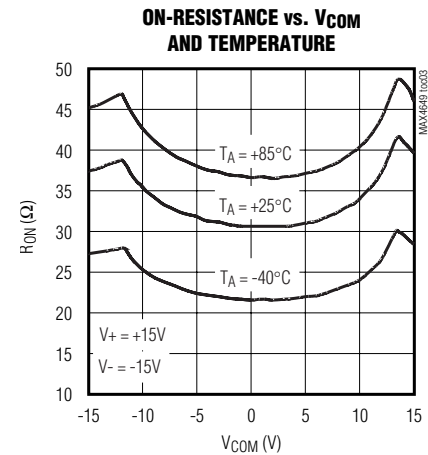
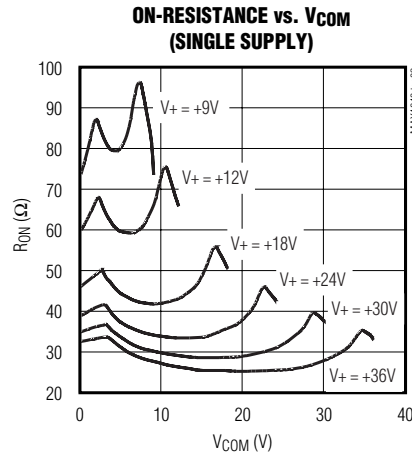
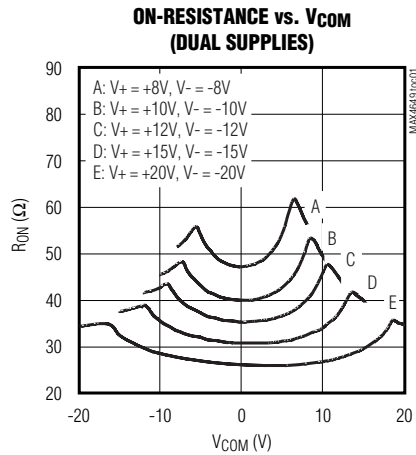
Note 4: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

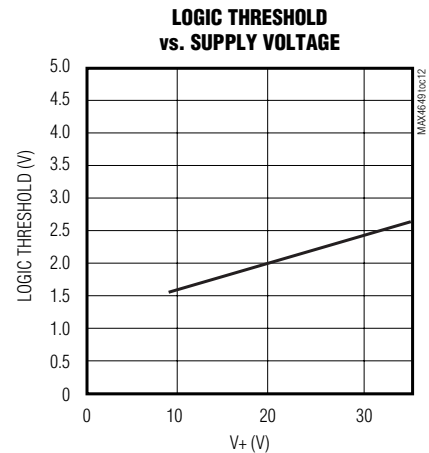
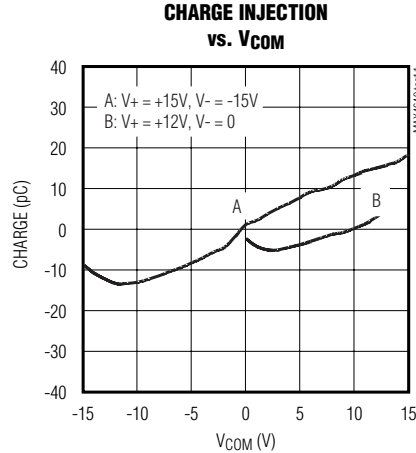
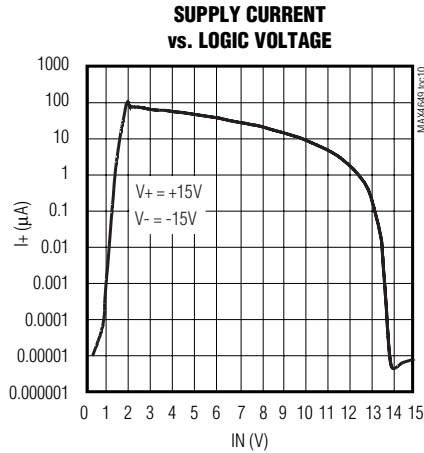
MAX4649



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Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	COM	Analog Switch Common
2	NC	Normally Closed Switch Terminal. NC is connected to COM when IN is low.
3	GND	Ground
4	V ₊	Positive Supply Voltage Input
5	N.C.	No Connection
6	IN	Digital Control Input
7	V ₋	Negative Supply Voltage Input
8	NO	Normally Open Switch Terminal. NO is connected to COM when IN is high.

Detailed Description

The MAX4649 is a high-voltage, single-pole/double-throw (SPDT) analog switch that operates from dual ±4.5V to ±20V supplies or from a single +9V to +36V supply. The MAX4649 has one normally closed (NC) switch and one normally open (NO) switch. CMOS switch construction allows bidirectional processing of rail-to-rail analog signals.

The MAX4649 has break-before-make switching. The transition time for switching from one input to the other is typically 90ns. The off-leakage is typically less than 10pA, and on-leakage is typically less than 20pA.

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V₊ on first, then V₋, followed by the logic inputs, NO₋, or COM. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with supply pins (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V₊ and one diode drop above V₋, but does not affect the device's low switch resistance and low

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leakage characteristics. Device operation is unchanged, and the difference between V_+ and V_- should not exceed 44V. These protection diodes are not recommended when using a single supply.

Off-Isolation at High Frequencies

In 50Ω systems, the high-frequency on-response of these parts extends from DC to above 300MHz, with a typical loss of -3.6dB. When the switch is turned off,

however, it behaves like a capacitor, and off-isolation decreases with increasing frequency. This effect is more pronounced with higher source and load impedances. Above 5MHz, circuit board layout becomes critical. The graphs shown in the *Typical Operating Characteristics* were taken using a 50Ω source and load connected with BNC connectors.

Test Circuits/Timing Diagrams

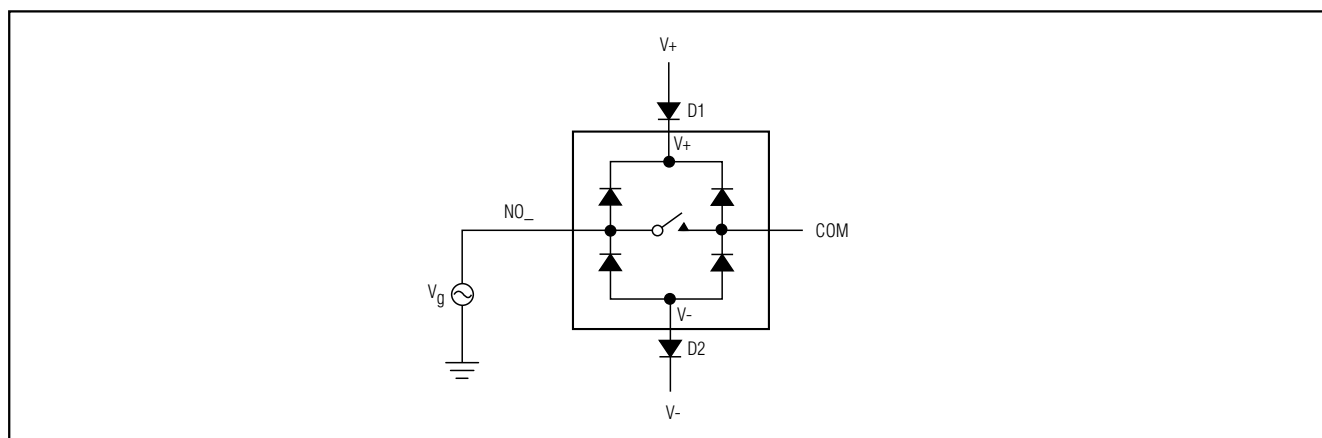


Figure 1. Overvoltage Protection

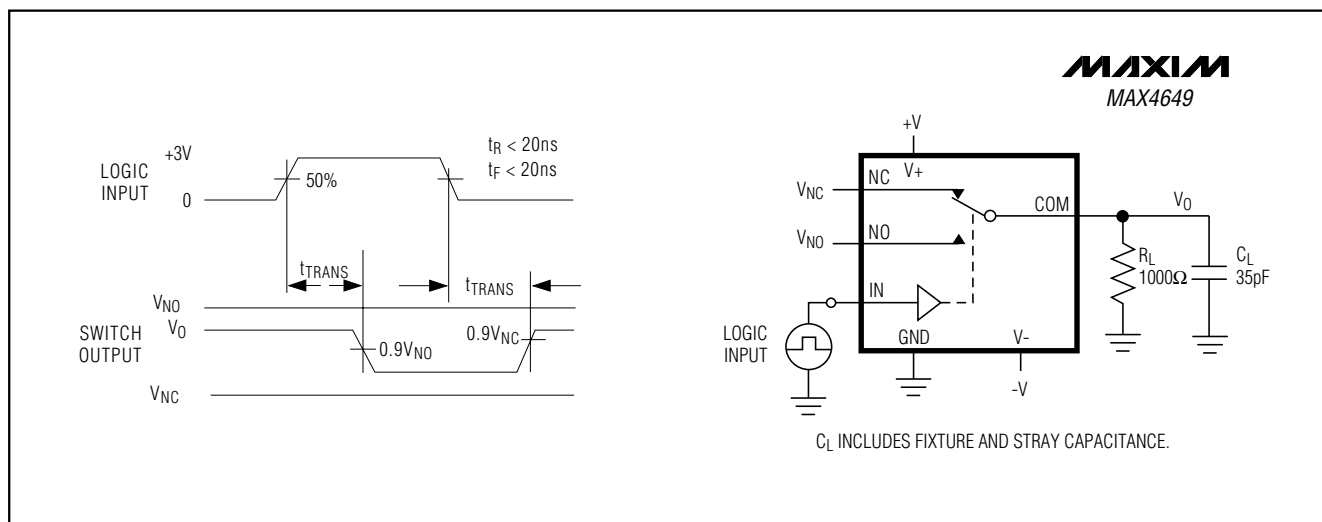


Figure 2. MAX4649 Transition Time

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Test Circuits/Timing Diagrams (continued)

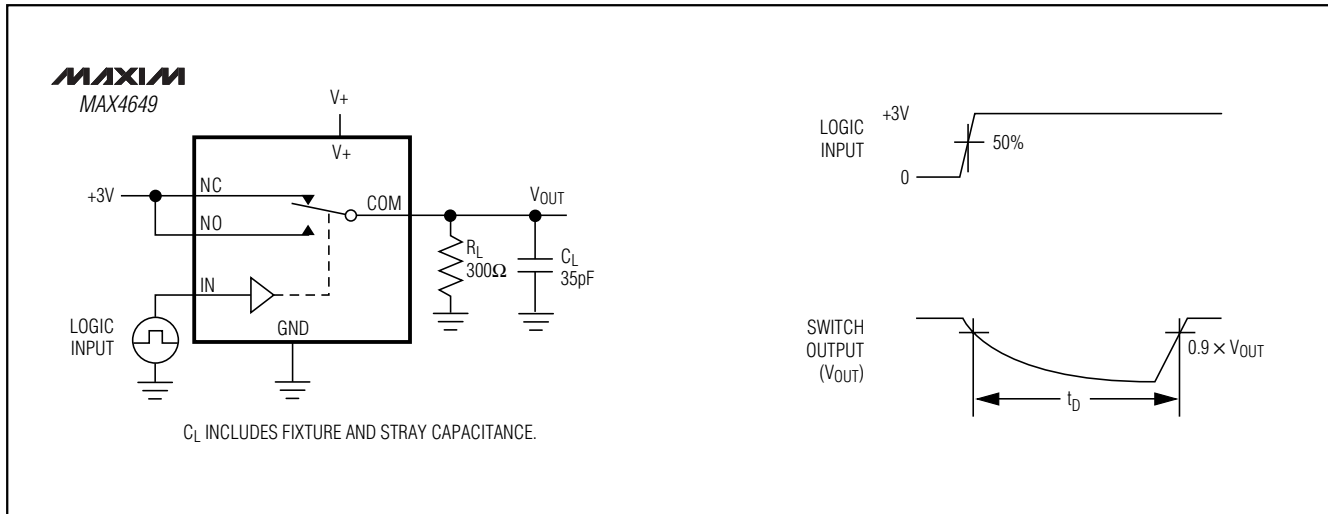


Figure 3. MAX4649 Break-Before-Make Test Circuit

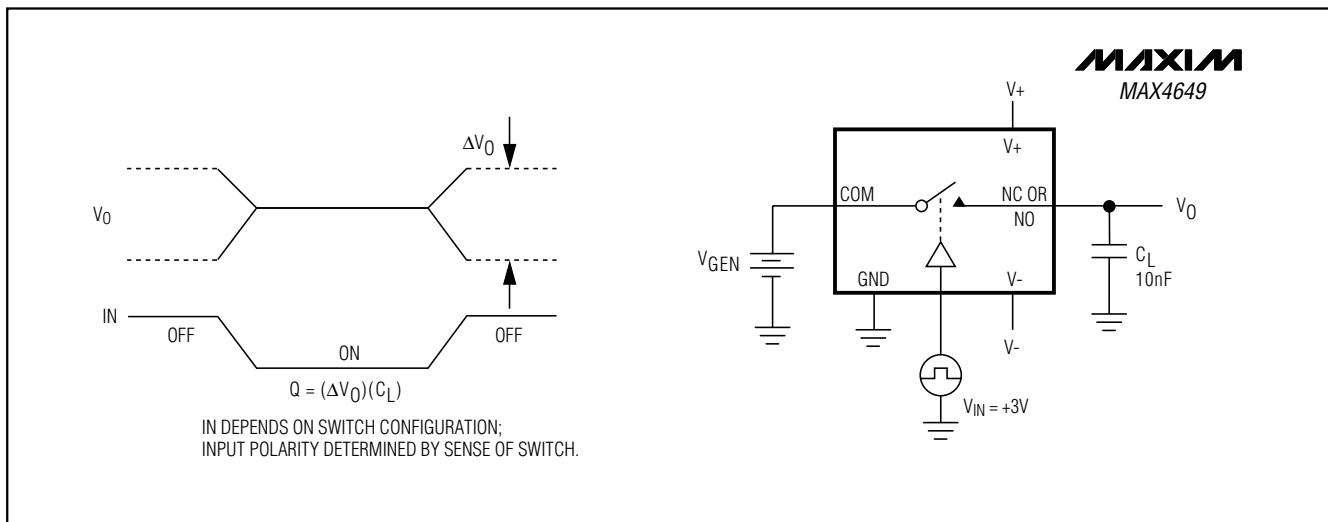


Figure 4. Charge Injection

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Test Circuits/Timing Diagrams (continued)

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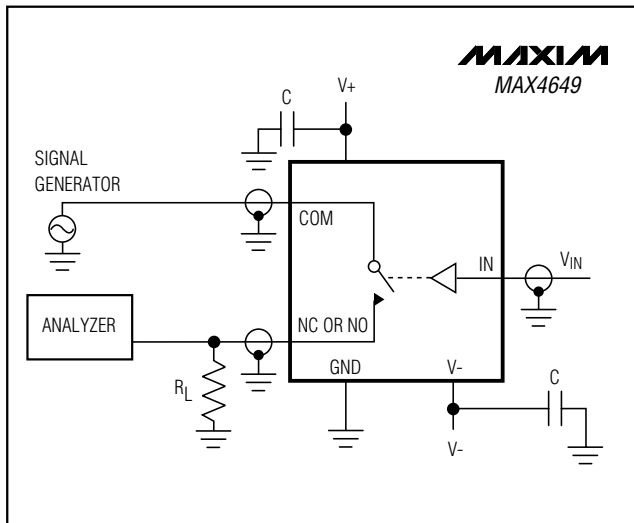


Figure 5. Off-Isolation

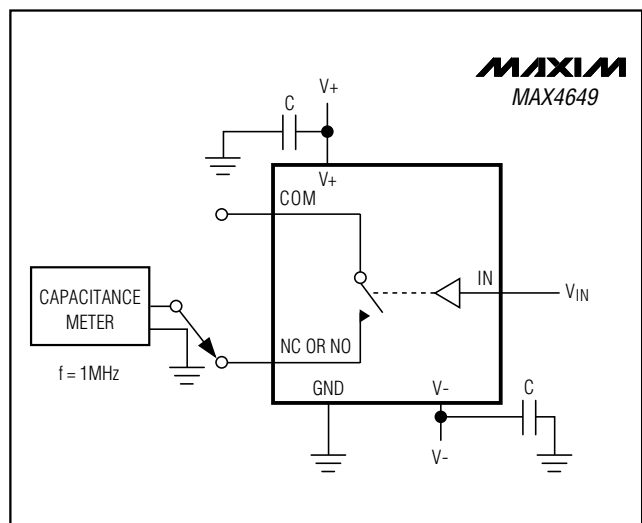


Figure 7. Channel-Off Capacitance

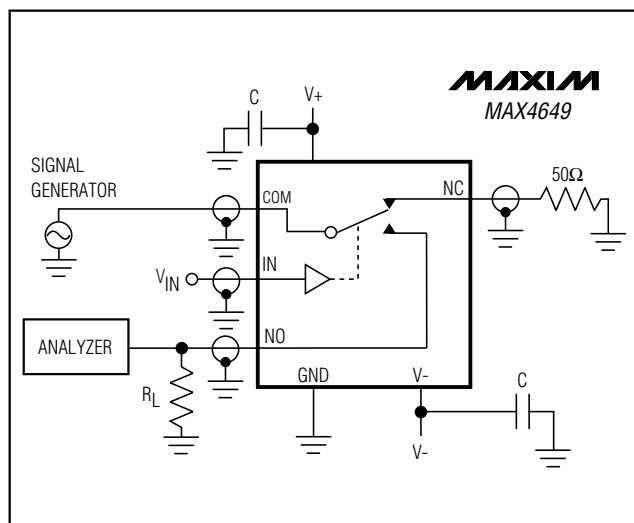


Figure 6. Crosstalk Between Switches

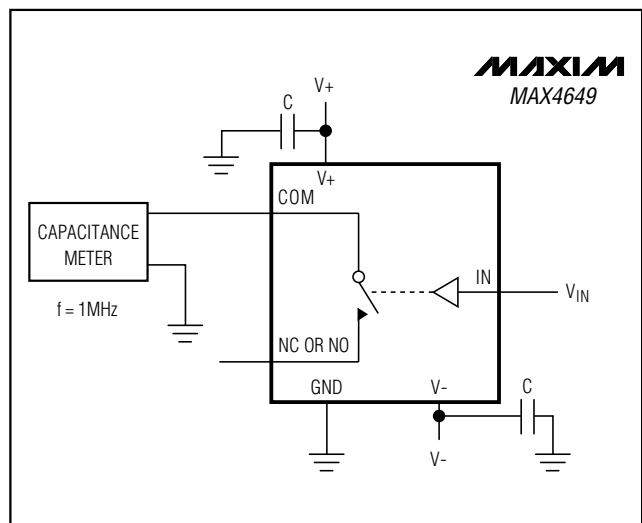


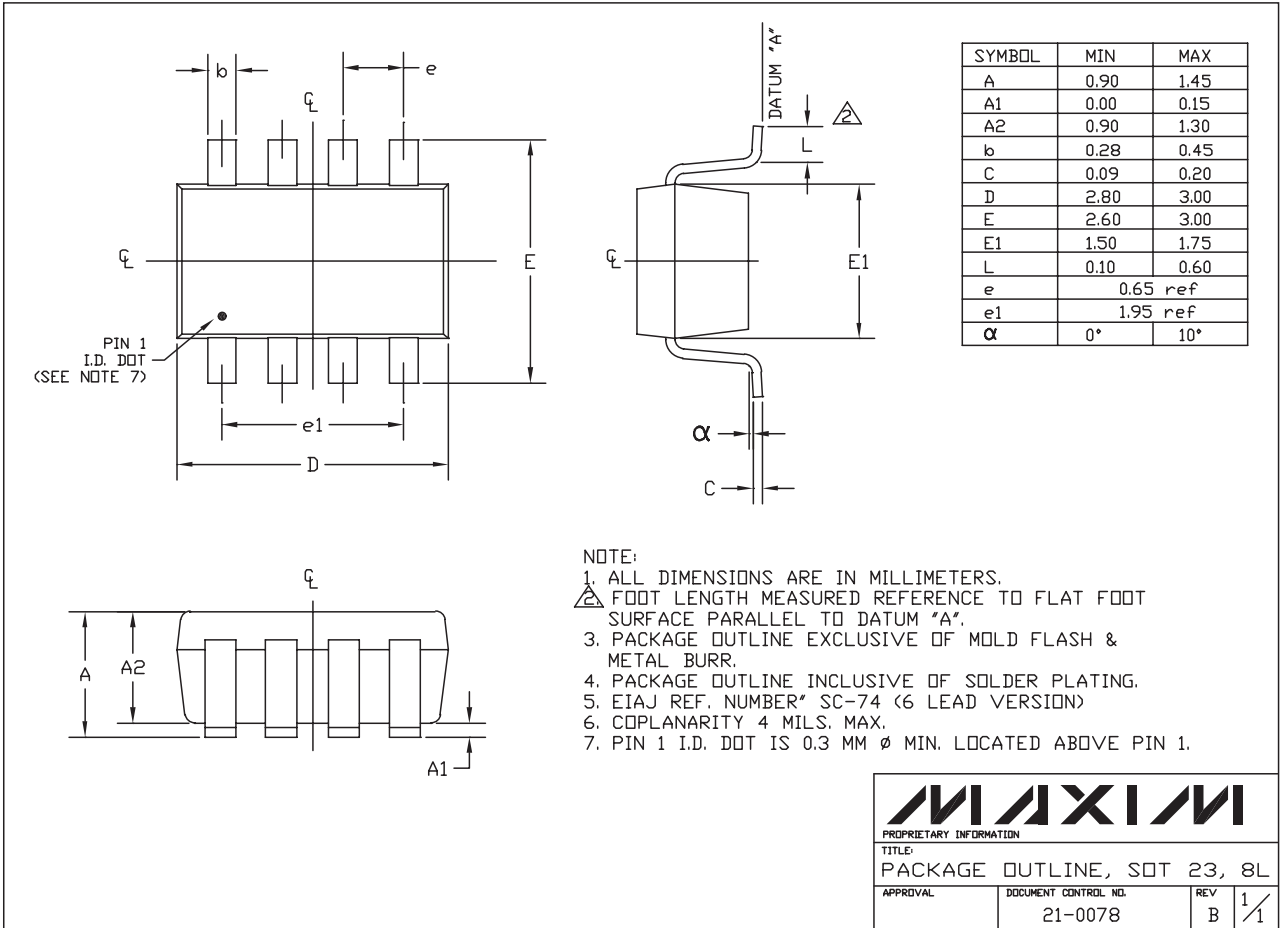
Figure 8. COM On-Capacitance

Chip Information

TRANSISTOR COUNT: 33
PROCESS TECHNOLOGY: CMOS

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Package Information



SOT23, 8LEPS

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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