ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, V_L ....-0.3V to +6V
I/O $V_{CC\_}$..-0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$ ....-0.3V to (V_L + 0.3V)
EN...-0.3V to +6V
Short-Circuit Duration I/O $V_{L\_}$, I/O $V_{CC\_}$ to GND ....Continuous

Continuous Power Dissipation (T_A = +70°C)
8-Pin µDFN (derate 4.8mW/°C above +70°C) 381mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to 5.5V, I/O $V_{L\_}$, and I/O $V_{CC\_}$ are unconnected, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		1.2		5.5	V
V_{CC} Supply Range	V_{CC}		1.65		5.50	V
Supply Current from V_{CC}	I_{QVCC}			130	300	µA
Supply Current from V_L	I_{QVL}			1	10	µA
V_{CC} Shutdown-Mode Supply Current	$I_{SHUTDOWN-VCC}$	T_A = +25°C, EN = GND		0.03	1	µA
V_L Shutdown-Mode Supply Current	$I_{SHUTDOWN-VL}$	T_A = +25°C, EN = GND		0.03	1	µA
I/O $V_{L\_}$ and I/O $V_{CC\_}$ Shutdown-Mode Leakage Current	$I_{SHUTDOWN-LKG}$	T_A = +25°C, EN = GND		0.02	1	µA
EN Input Leakage		T_A = +25°C		0.02	1	µA
Tri-State Threshold Low	V_{TH_L}	V_{CC} falling (Note 3)			1.5	V
Tri-State Threshold High	V_{TH_H}	V_{CC} rising (Note 3)			1	V
ESD PROTECTION						
I/O V_{CC}		Human Body Model (Note 4)		±15		kV
LOGIC-LEVEL THRESHOLDS						
I/O $V_{L\_}$ Input-Voltage High	V_{IHL}		V_L - 0.2			V
I/O $V_{L\_}$ Input-Voltage Low	V_{ILL}				0.15	V
I/O $V_{CC\_}$ Input-Voltage High	V_{IHC}		V_{CC} - 0.4			V
I/O $V_{CC\_}$ Input-Voltage Low	V_{ILC}				0.15	V
I/O $V_{L\_}$ Output-Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA, I/O $V_{CC\_}$ > V_{CC} - 0.4V	0.67 x V_L			V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 1mA, I/O $V_{CC\_}$ < 0.15V			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to 5.5V, I/O $V_{L\_}$, and I/O $V_{CC\_}$ are unconnected, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Output-Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA, I/O $V_{L\_}$ > V_L - 0.2V	0.67 x V_{CC}			V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 1mA, I/O $V_{L\_}$ < 0.15V			0.4	V
EN Input-Voltage High	V_{IH-EN}		V_L - 0.2			V
EN Input-Voltage Low	V_{IL-EN}				0.15	V
RISE/FALL-TIME ACCELERATOR STAGE						
Transition-Detect Threshold		I/O V_{CC} side		0.8		V
		I/O V_L side		0.8		
Accelerator Pulse Duration		V_L = 1.2V, V_{CC} = 1.65V		27		ns
I/O $V_{L\_}$ Output-Accelerator Source Impedance		V_L = 1.2V, V_{CC} = 1.65V		40		Ω
		V_L = 5V, V_{CC} = 5V		9		
I/O $V_{CC\_}$ Output-Accelerator Source Impedance		V_L = 1.2V, V_{CC} = 1.65V		30		Ω
		V_L = 5V, V_{CC} = 5V		12		

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to +5.5V, R_{LOAD} = 1MΩ, C_{LOAD} = 15pF, driver output impedance ≤ 50Ω, I/O test signal of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
+1.2V ≤ V_L ≤ V_{CC} ≤ +5.5V							
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Push-pull driving (Figure 1a)			7	25	ns
		Open-drain driving (Figure 1c)			170	400	
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Push-pull driving (Figure 1a)			6	37	ns
		Open-drain driving (Figure 1c)			6	37	
I/O $V_{L\_}$ Rise Time	t_{RVL}	Push-pull driving (Figure 1b)			8	30	ns
		Open-drain driving (Figure 1d)			180	400	
I/O $V_{L\_}$ Fall Time	t_{FVL}	Push-pull driving (Figure 1b)			3	30	ns
		Open-drain driving (Figure 1d)			3	30	
Propagation Delay	$t_{PD-VL-VCC}$	Driving I/O $V_{L\_}$	Push-pull driving (Figure 1a)		5	30	ns
			Open-drain driving (Figure 1c)		170	800	
	$t_{PD-VCC-VL}$	Driving I/O $V_{CC\_}$	Push-pull driving (Figure 1b)		4	30	
			Open-drain driving (Figure 1d)		190	1000	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded	Push-pull driving			20	ns
			Open-drain driving			50	
Maximum Data Rate		Push-pull driving		8			Mbps
		Open-drain driving		500			kbps

Dual Bidirectional Low-Level Translator in µDFN

TIMING CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to +5.5V, R_{LOAD} = 1MΩ, C_{LOAD} = 15pF, driver output impedance ≤ 50Ω, I/O test signal of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+1.8V ≤ V_L ≤ V_{CC} ≤ +3.3V						
I/O V_{CC}_ Rise Time	t_{RVCC}	Figure 1a (Note 5)			15	ns
I/O V_{CC}_ Fall Time	t_{FVCC}	Figure 1a (Note 6)			15	ns
I/O V_L_ Rise Time	t_{RVL}	Figure 1b (Note 5)			15	ns
I/O V_L_ Fall Time	t_{FVL}	Figure 1b (Note 6)			15	ns
Propagation Delay	$t_{PD-VL-VCC}$	Driving I/O V_L_			15	ns
	$t_{PD-VCC-VL}$	Driving I/O V_{CC}_			15	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			10	ns
Maximum Data Rate			16			Mbps

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: For normal operation, ensure V_L < (V_{CC} + 0.3V).

Note 3: When V_{CC} is below V_L by more than the tri-state threshold, the device turns off its pullup resistors and I/O_ enters tri-state. The device is not in shutdown.

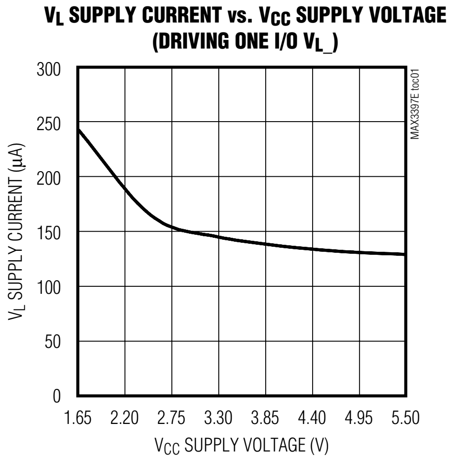
Note 4: To ensure maximum ESD protection, place a 1µF capacitor between V_{CC} and GND. See the *Typical Application Circuit*.

Note 5: 10% of input to 90% of output.

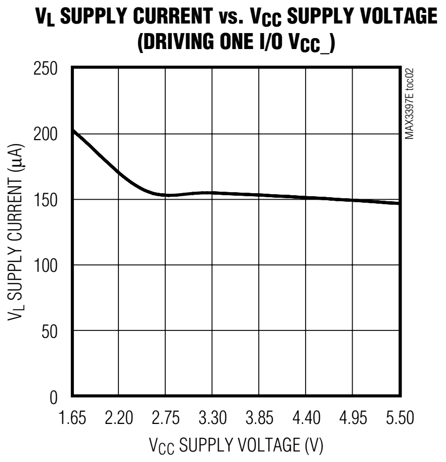
Note 6: 90% of input to 10% of output.

Typical Operating Characteristics

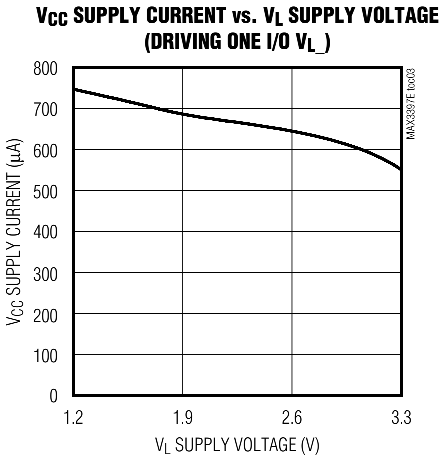
(V_{CC} = +3.3V, V_L = +1.8V, R_{LOAD} = 1MΩ, C_{LOAD} = 15pF, T_A = +25°C, data rate = 8Mbps, unless otherwise noted.)



V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O V_L_)



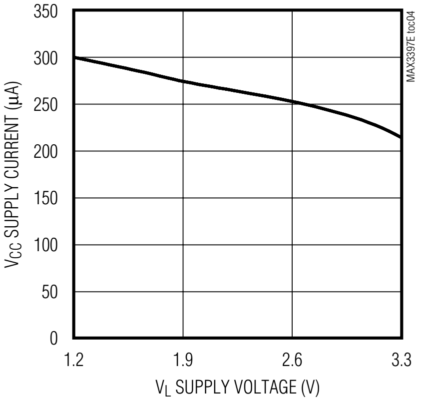
V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING ONE I/O V_{CC}_)

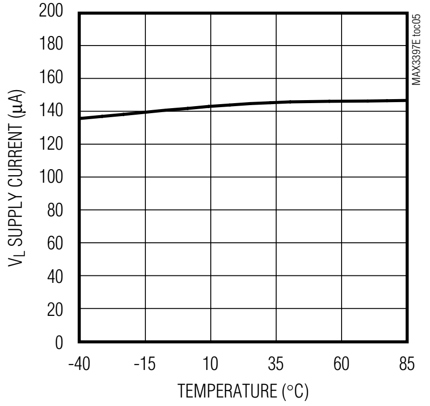


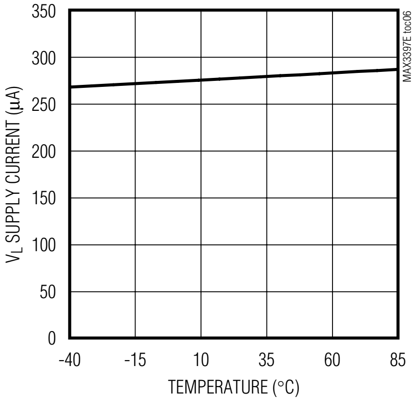
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O V_L_)

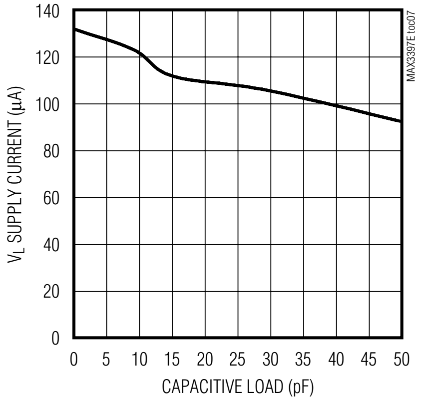
Typical Operating Characteristics (continued)

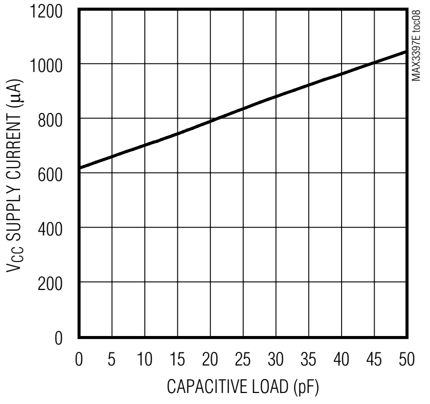
(V_{CC} = +3.3V, V_L = +1.8V, R_{LOAD} = 1MΩ, C_{LOAD} = 15pF, T_A = +25°C, data rate = 8Mbps, unless otherwise noted.)

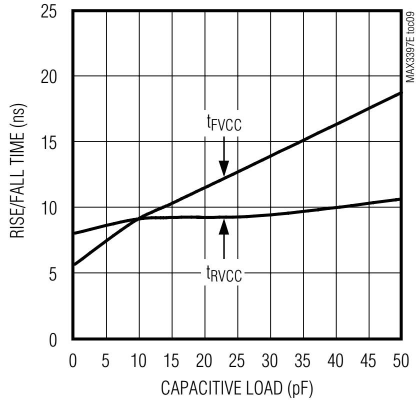

V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING ONE I/O V_{CC}_)

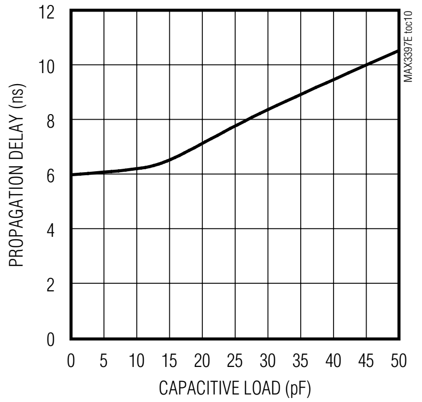

V_L SUPPLY CURRENT vs. TEMPERATURE (DRIVING ONE I/O V_L_)

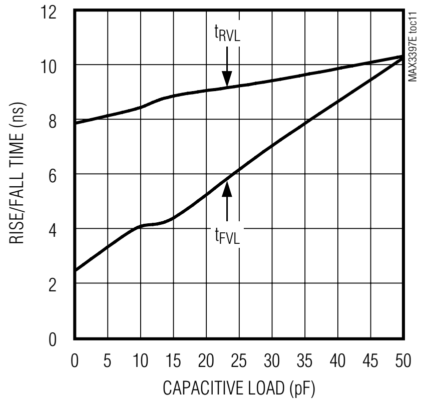

V_L SUPPLY CURRENT vs. TEMPERATURE (DRIVING ONE I/O V_{CC}_)

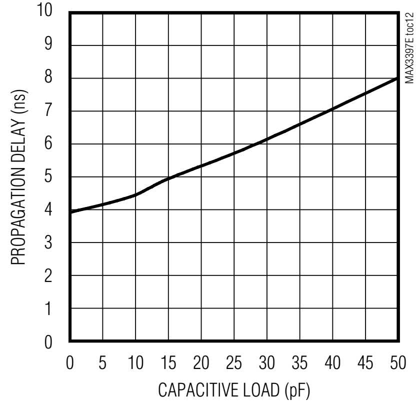

V_L SUPPLY CURRENT vs. CAPACITIVE LOAD (DRIVING ONE I/O V_L_)


V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD (DRIVING ONE I/O V_L_)


RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING ONE I/O V_L_)


PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING ONE I/O V_L_)

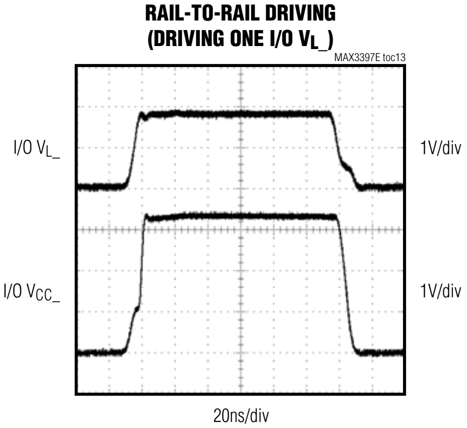

RISE/FALL TIME vs. CAPACITIVE LOAD (DRIVING ONE I/O V_{CC}_)

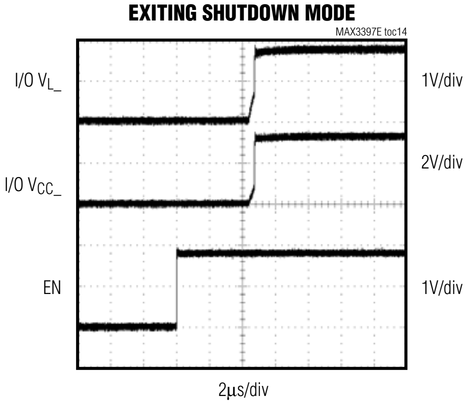

PROPAGATION DELAY vs. CAPACITIVE LOAD (DRIVING ONE I/O V_{CC}_)

Dual Bidirectional Low-Level Translator in µDFN

Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_L = +1.8V, R_{LOAD} = 1MΩ, C_{LOAD} = 15pF, T_A = +25°C, data rate = 8Mbps, unless otherwise noted.)





Pin Description

PIN	NAME	FUNCTION
1	I/O V_{CC2}	Input/Output 2. Referenced to V_{CC}.
2	GND	Ground
3	V_L	Logic-Input Voltage. The supply voltage range is +1.2V ≤ V_L ≤ +5.5V. Bypass this supply with a 0.1µF capacitor located as close as possible to the input.
4	I/O V_{L2}	Input/Output 2. Referenced to V_L.
5	I/O V_{L1}	Input/Output 1. Referenced to V_L.
6	EN	Enable Input. Drive EN high to enable the device. Drive EN low to put the device in shutdown mode.
7	V_{CC}	V_{CC} Input Voltage. The supply voltage range is +1.65V ≤ V_{CC} ≤ +5.5V. Bypass this supply with a 0.1µF capacitor located as close as possible to the input. A 1µF ceramic capacitor is recommended for full ESD protection.
8	I/O V_{CC1}	Input/Output 1. Referenced to V_{CC}.

Detailed Description

The MAX3397E bidirectional, ESD-protected level translator provides the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. A logic-low signal present on the V_L side of the device appears as a logic-low signal on the V_{CC} side of the device, and vice versa. The device uses a transmission-gate-based design (see the *Functional Diagram*) to allow data translation in either direction (V_L ↔ V_{CC}) on any single data line. The MAX3397E accepts V_L from +1.2V to +5.5V and V_{CC} from +1.65V to +5.5V, making the device ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX3397E features a shutdown mode that reduces the supply current to less than 1µA, thermal short-circuit protection, and ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally. The device operates at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. See the *Timing Characteristics* table.

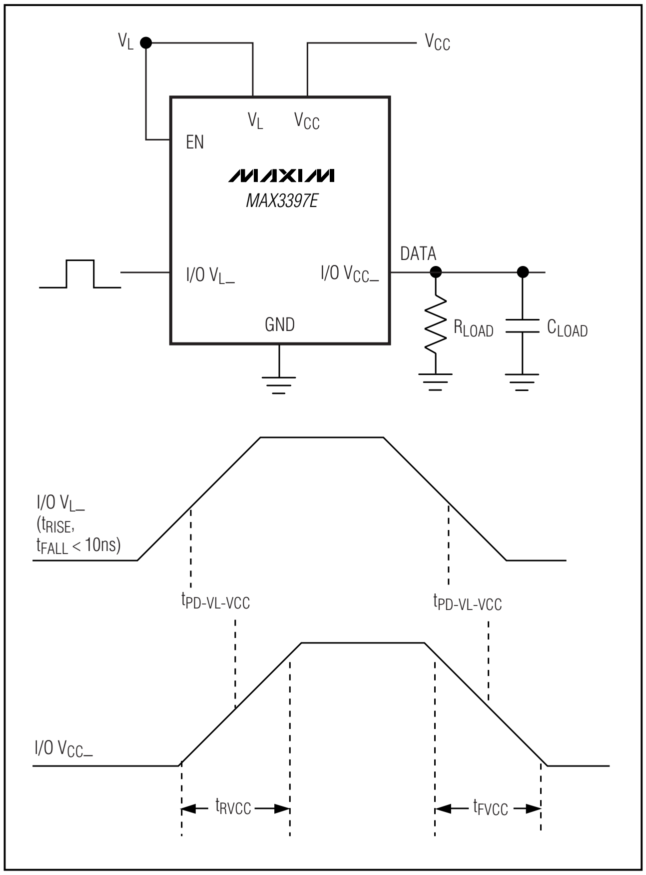


Figure 1a. Rail-to-Rail Driving I/O V_L

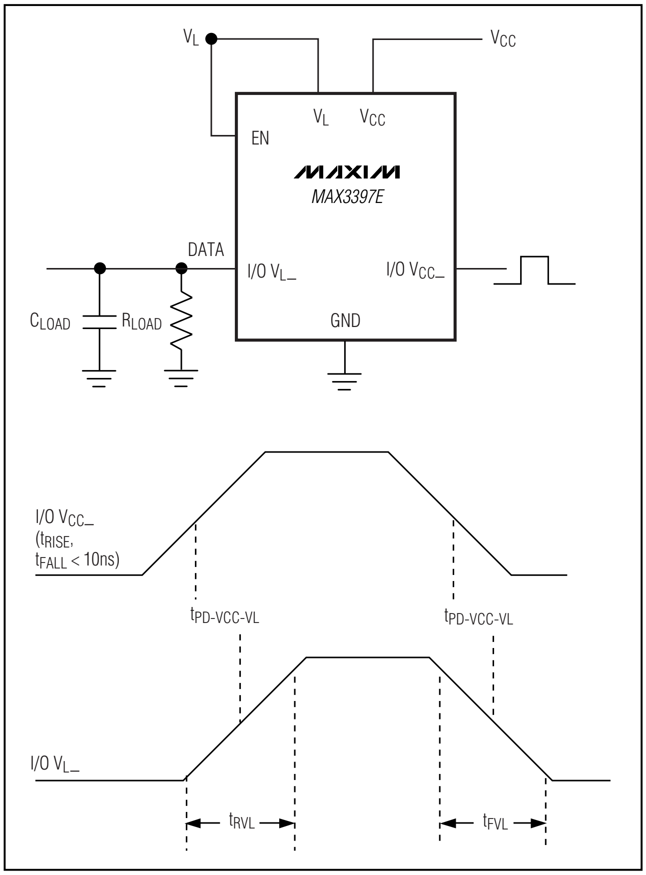


Figure 1b. Rail-to-Rail Driving I/O V_{CC}

Level Translation

For proper operation, ensure that $+1.65V \le V_{CC} \le +5.5V$ and $+1.2V \le V_L \le +5.5V$. During power-up sequencing, $V_L \ge (V_{CC} + 0.3V)$ does not damage the device. The speed-up circuitry limits the maximum data rate for the MAX3397E to 16Mbps. The maximum data rate also depends heavily on the load capacitance (see the *Typical Operating Characteristics*), output impedance of the driver, and the operational voltage range (see the *Timing Characteristics* table).

Rise-Time Accelerators

The MAX3397E has an internal rise-time accelerator, allowing operation up to 16Mbps. The rise-time accelerators are present on both sides of the device and act to speed up the rise time of the input and output of the device, regardless of the direction of the data. The triggering mechanism for these accelerators is both level and edge sensitive. To prevent false triggering of the rise-time accelerators, signal fall times of less than 20ns/V are recommended for both the inputs and outputs of the device. Under less noisy conditions, longer signal fall times are acceptable. **Note:** To guarantee operation of the rise time, accelerators the maximum parasitic capacitance should be less than 200pF on the I/O lines.

Shutdown Mode

Drive EN low to place the MAX3397E in shutdown mode. Connect EN to V_L or V_{CC} (logic-high) for normal operation. Activating the shutdown mode disconnects the internal 10kΩ pullup resistors on the I/O V_{CC} and I/O V_L lines. This forces the I/O lines to a high-impedance state, and decreases the supply current to less than 1µA. The high-impedance I/O lines in shutdown mode allow for use in a multidrop network. The MAX3397E effectively has a diode from each I/O to the corresponding supply rail and GND. Therefore, when in shutdown mode, do not allow the voltage at I/O $V_{L\_}$ to exceed (V_L + 0.3V), or the voltage at I/O $V_{CC\_}$ to exceed (V_{CC} + 0.3V).

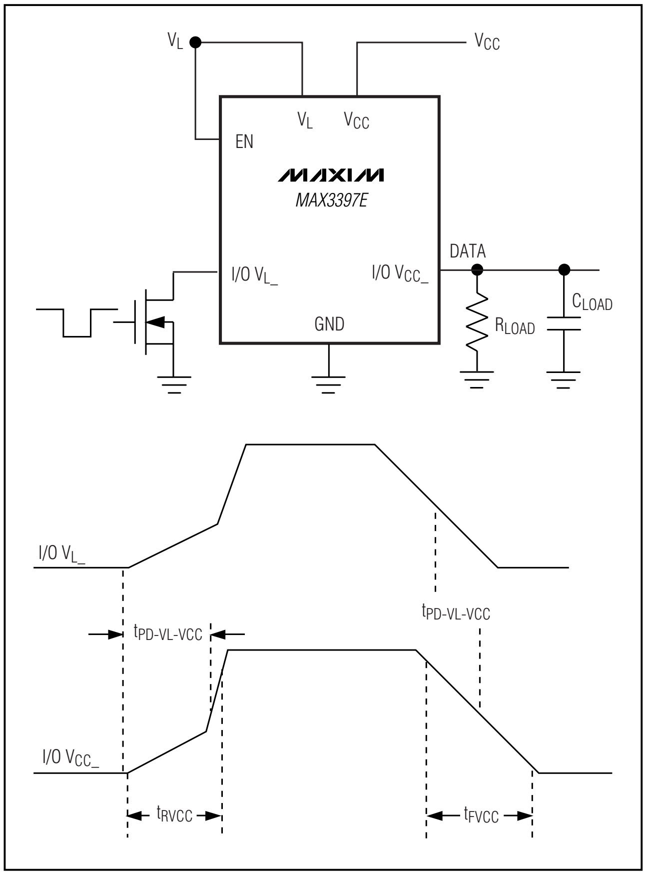


Figure 1c. Open-Drain Driving I/O V_L

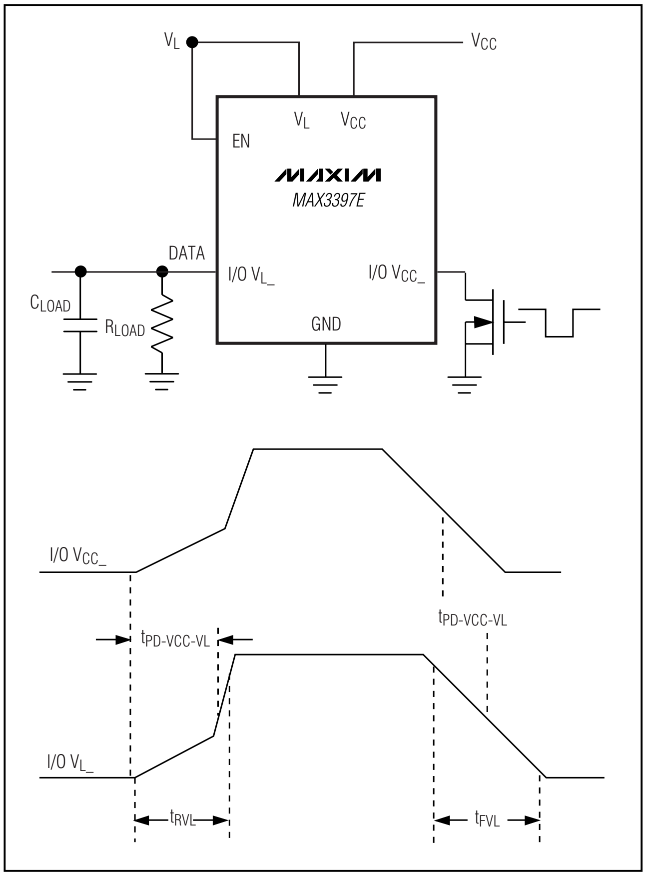


Figure 1d. Open-Drain Driving I/O V_{CC}

Operation with One Supply Disconnected

Certain applications require sections of circuitry to be disconnected to save power. When V_L is connected and V_{CC} is disconnected or connected to ground, the device enters shutdown mode. In this mode, I/O V_L can still be driven without damage to the device; however, data does not translate from I/O V_L to I/O V_{CC}. If V_{CC} falls more than 0.8V (typ) below V_L, the device disconnects the pullup resistors at I/O V_L and I/O V_{CC}. To achieve the lowest possible supply current from V_L when V_{CC} is disconnected, it is recommended that the voltage at the V_{CC} supply input be approximately equal to GND. **Note:** When V_{CC} is disconnected or connected to ground, I/O V_{CC} must not be driven more than V_{CC} + 0.3V.

When V_{CC} is connected and V_L is less than 0.7V (typ), the device enters shutdown mode. In this mode, I/O V_{CC} can still be driven without damage to the device; however, data does not translate from I/O V_{CC} to I/O V_L. **Note:** When V_L is disconnected or connected to ground, I/O V_L must not be driven more than V_L + 0.3V.

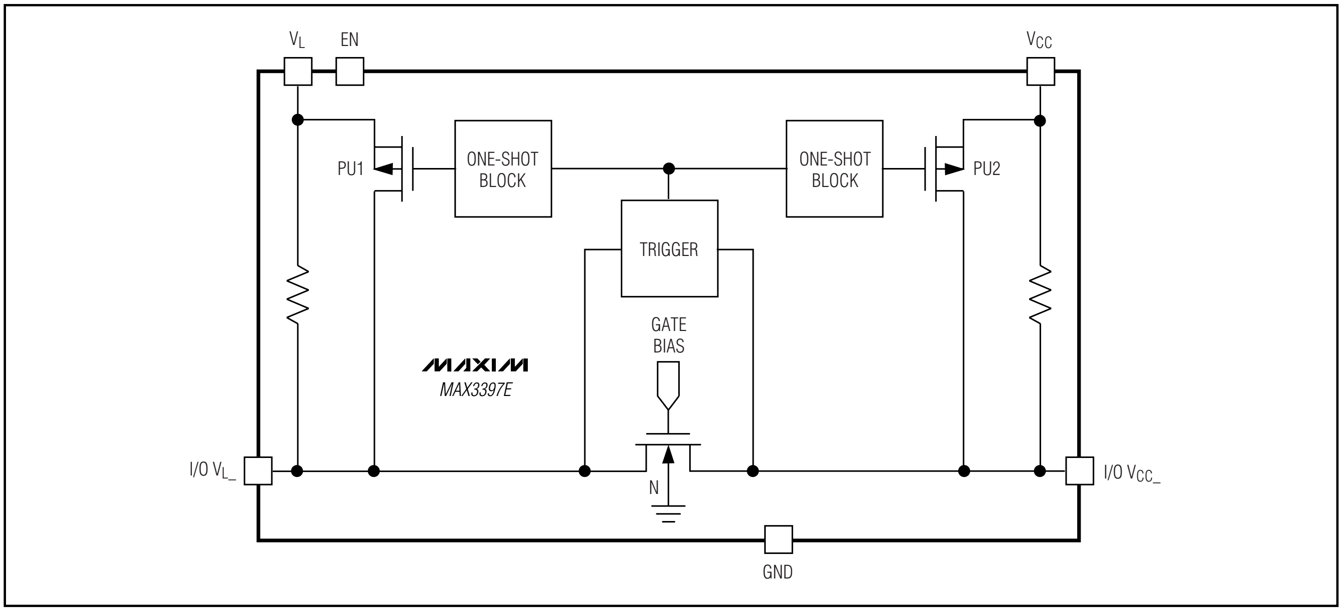
Thermal Short-Circuit Protection

Thermal-overload detection protects the MAX3397E from short-circuit fault conditions. In the event of a short-circuit fault, when the junction temperature (T_J) reaches +150°C, a thermal sensor signals the shutdown mode logic to force the device into shutdown mode. When the T_J has cooled to +140°C, normal operation resumes.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O V_{CC} lines have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown mode, and powered down. After an ESD event, Maxim's E versions keep working without

Functional Diagram



latchup, whereas competing products can latch and must be powered down to remove latchup. ESD protection can be tested in various ways. The I/O V_{CC} lines of the MAX3397E are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ± 8kV using the Contact Discharge method specified by IEC 61000-4-2
3) ±15kV using the Air-Gap Discharge method specified by IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3397E helps

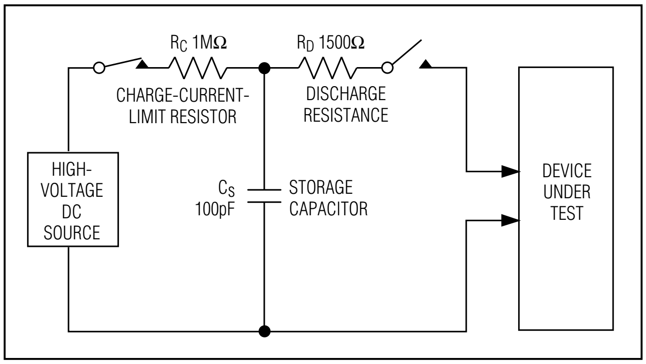


Figure 2a. Human Body ESD Test Model

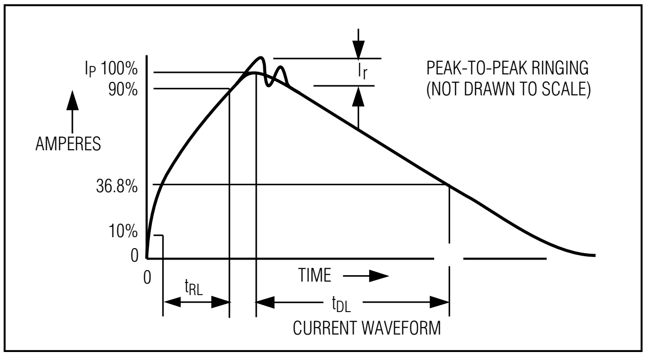


Figure 2b. Human Body Current Waveform

to design equipment that meets Level 4 of IEC 61000-4-2 without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 3a shows the IEC 61000-4-2 model, and Figure 3b shows the current waveform for the ±8kV, IEC 61000-4-2, Level 4, ESD contact-discharge test.

The Air-Gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

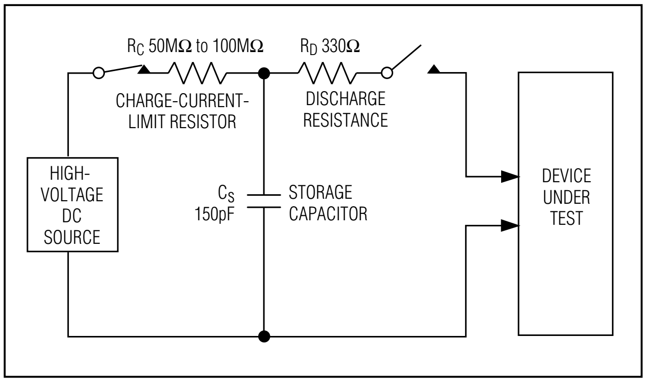


Figure 3a. IEC 61000-4-2 ESD Test Model

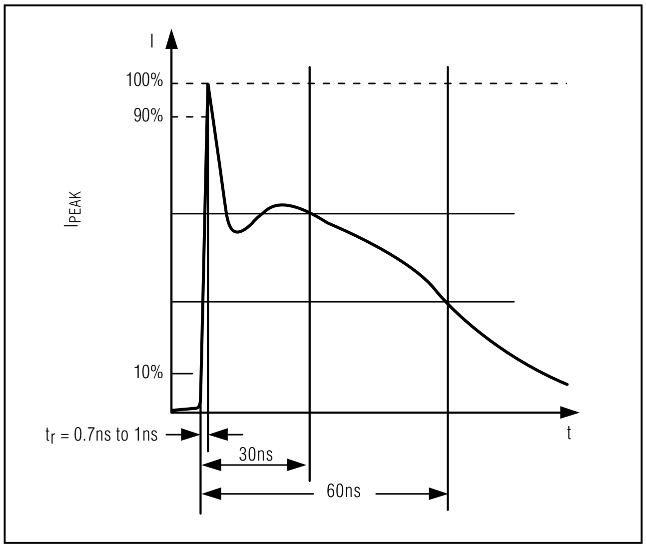


Figure 3b. IEC 61000-4-2 ESD Generator Current Waveform

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PCB assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with a 0.1µF capacitor (see the *Typical Application Circuit*). To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF capacitor. Place all capacitors as close as possible to the power-supply inputs.

I^{2}C Level Translation

The MAX3397E level-shifts the data present on the I/O lines between +1.2V and +5.5V, making them ideal for level translation between a low-voltage ASIC and an I^{2}C device. A typical application involves interfacing a low-voltage microprocessor to a 3V or 5V D/A converter, such as the MAX517.

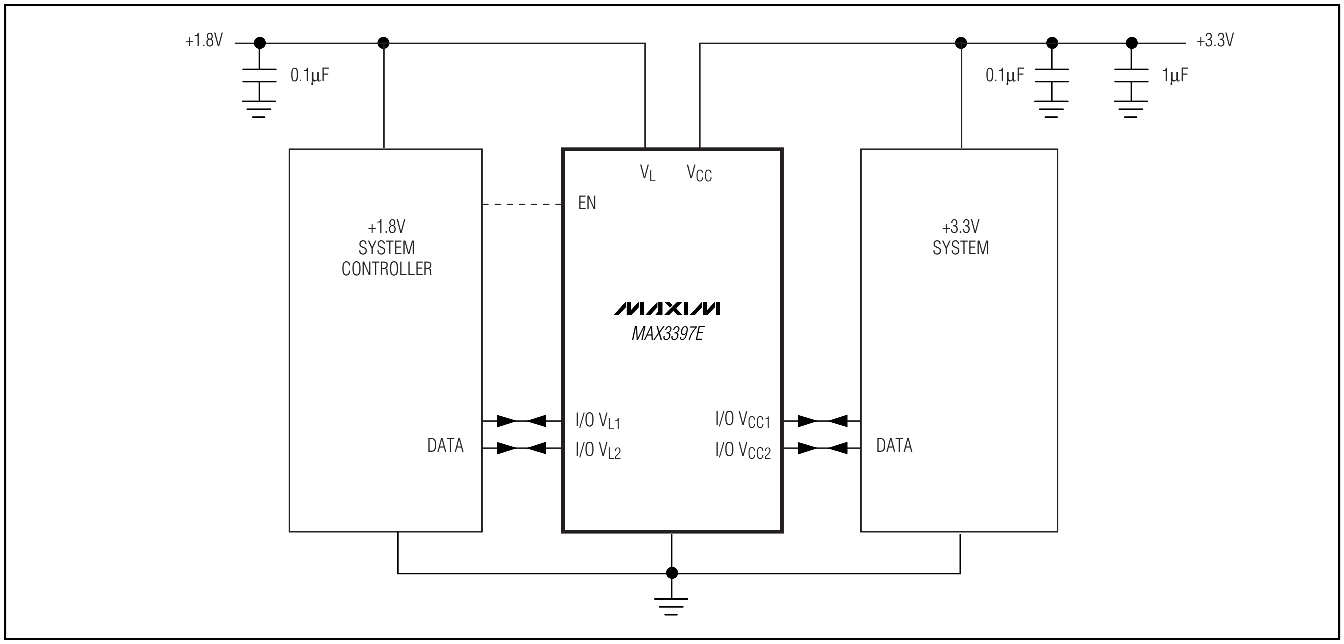
Push-Pull vs. Open-Drain Driving

The MAX3397E can be driven in a push-pull configuration and include internal 10kΩ resistors that pull up I/O V_{L}_ and I/O V_{CC}_ to their respective power supplies, allowing operation of the I/O lines with open-drain devices. See the *Timing Characteristics* table for maximum data rates when using open-drain drivers.

Chip Information

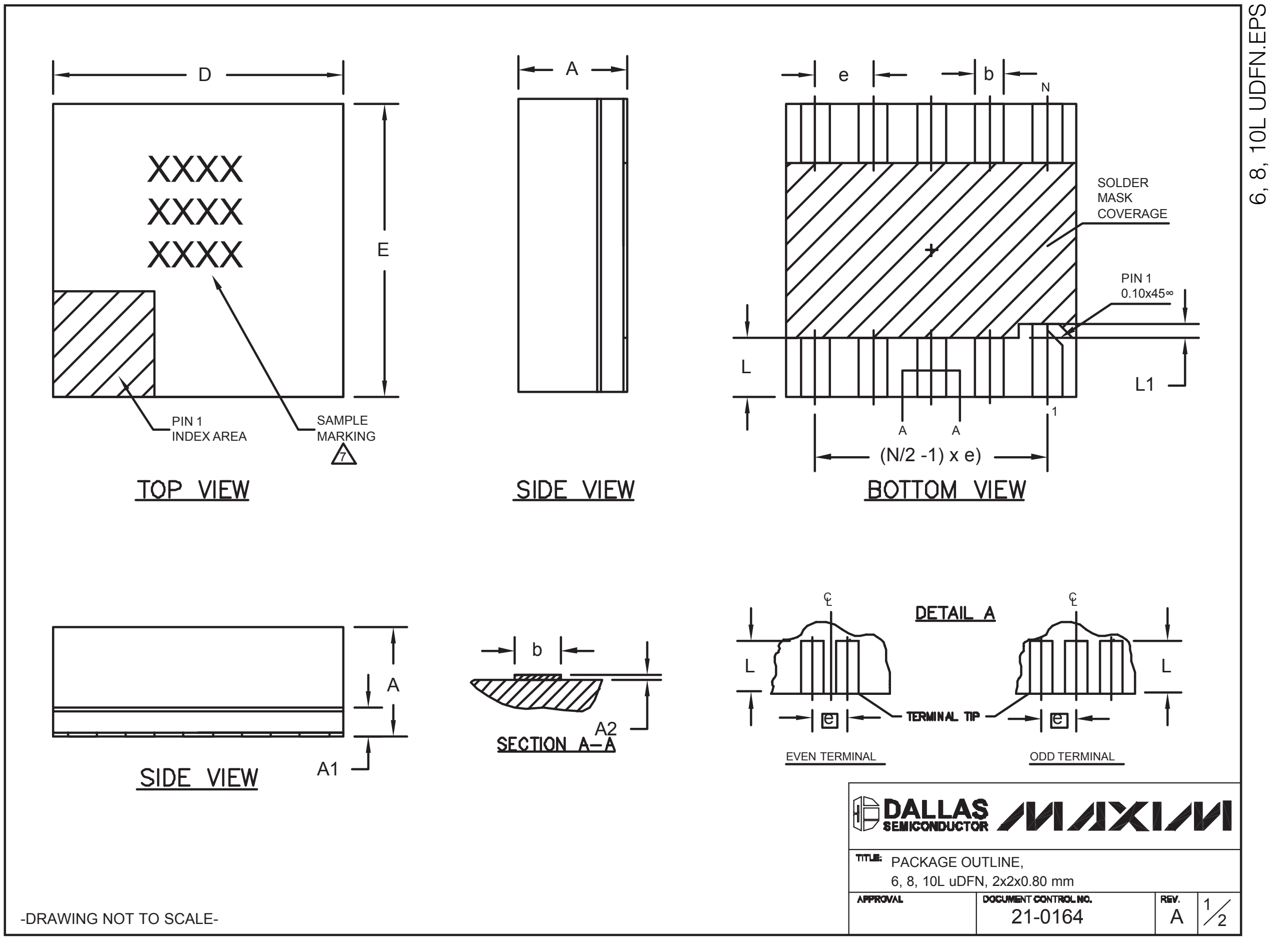
PROCESS: BiCMOS

Typical Application Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 -1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
△7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0164	REV. A	2/2