

Absolute Maximum Ratings

IN, CSN, DIM to GND -0.3V to +30V
V_{CC}, DRV to GND -0.3V to +6V
CSN to IN -0.3V to +0.3V
Maximum Current into Any Pin
(except IN, V_{CC}, and DRV) ±20mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 18.17mW/°C* above +70°C) 1454mW

Operating Temperature Range -40°C to +125°C
Junction Temperature +150°C
Storage Temperature Range -65°C to +150°C
Lead Temperature (soldering, 10s) +300°C
Pin-to-Pin ESD Ratings (HB Model) 2.5kV

*As per JEDEC51 Standard (Single-Layer Board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 12V, V_{DIM} = V_{IN}, C_{VCC} = 1μF, R_{SENSE} = 0.5Ω, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V _{IN}		4.5		28.0	V
Maximum Current Regulator Switching Frequency	f _{SW}				2	MHz
Ground Current	I _{GND}	DRV open			1.5	mA
Supply Current	I _{IN}	V _{DIM} < 0.6V			425	μA
Undervoltage Lockout	UVLO	V _{IN} = V _{CSN} = V _{DIM} , V _{IN} rising from 4V until V _{DRV} > V _{CC} - 0.5V		4.7	5.0	V
		V _{IN} = V _{CSN} = V _{DIM} , V _{IN} falling from 6V, V _{DRV} < 0.5V			4.5	
Undervoltage Lockout Hysteresis				0.5		V
SENSE COMPARATOR						
Sense Voltage Threshold High	V _{SNSHI}	(V _{IN} - V _{CSN}) rising from 0V until V _{DRV} < 0.5V (MAX16820)	195	210	225	mV
		(V _{IN} - V _{CSN}) rising from 0V until V _{DRV} < 0.5V (MAX16819)	213	230	246	
Sense Voltage Threshold Low	V _{SNSLO}	(V _{IN} - V _{CSN}) falling from 0.26V until V _{DRV} > (V _{CC} - 0.5V) (MAX16820)	176	190	204	mV
		(V _{IN} - V _{CSN}) falling from 0.26V until V _{DRV} > (V _{CC} - 0.5V) (MAX16819)	158	170	182	
Propagation Delay to Output High	t _{DPDH}	Falling edge of (V _{IN} - V _{CSN}) from 0.26V to 0V to DRV high, C _{DRV} = 1nF		82		ns
Propagation Delay to Output Low	t _{DPDL}	Rising edge of (V _{IN} - V _{CSN}) from 0V to 0.26V to DRV low, C _{DRV} = 1nF		82		ns
Current-Sense Input Current	I _{CSN}	(V _{IN} - V _{CSN}) = 200mV			1	μA
Current-Sense Threshold Hysteresis	C _{SHYS}	MAX16819		56	70	mV
		MAX16820		17	35	mV

Electrical Characteristics (continued)

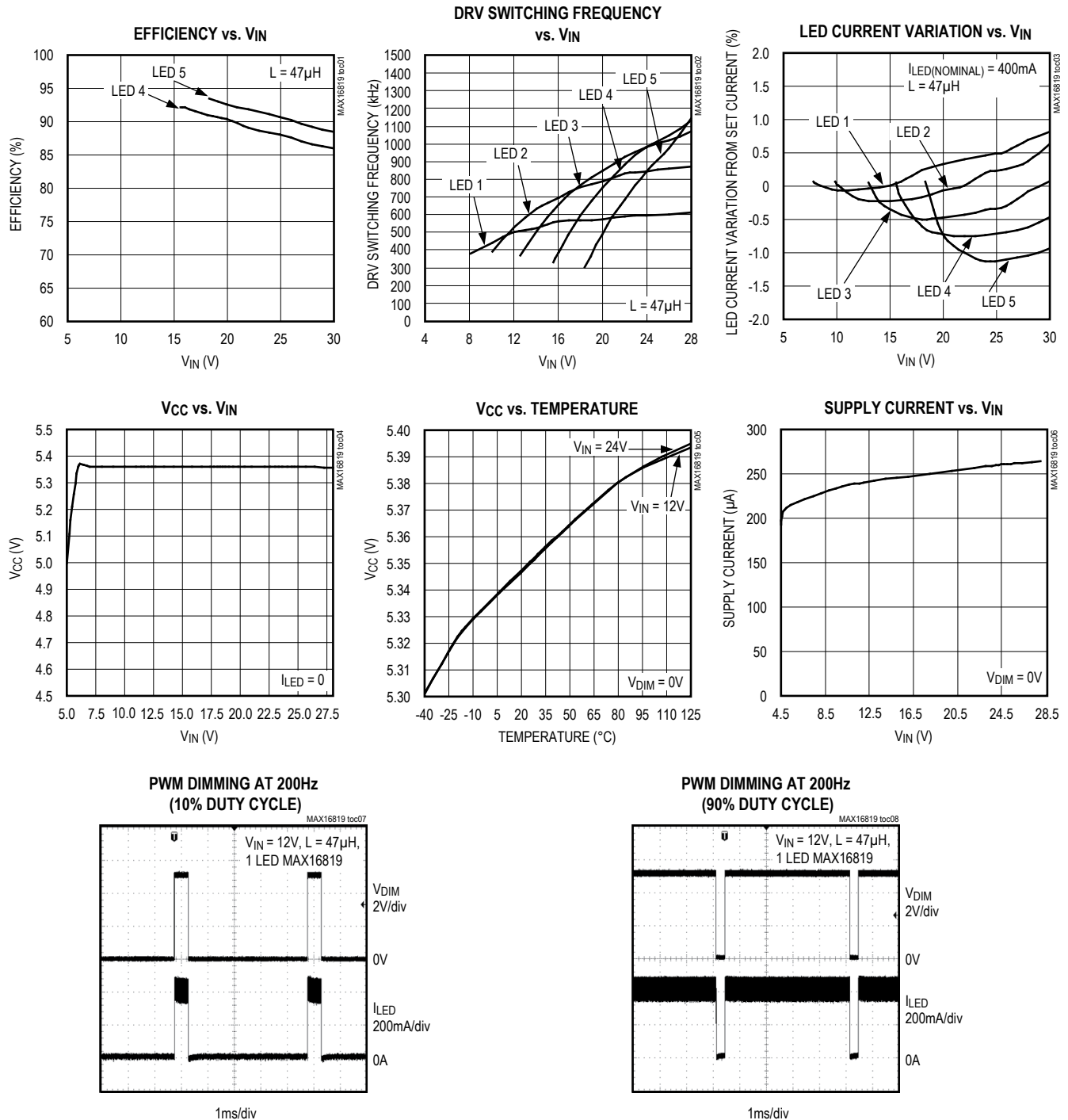
($V_{IN} = 12V$, $V_{DIM} = V_{IN}$, $C_{VCC} = 1\mu F$, $R_{SENSE} = 0.5\Omega$, $T_A = T_J = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER						
Gate Driver Source Current		$V_{CSN} = V_{IN}$, $V_{DRV} = 0.5 \times V_{CC}$		0.5		A
Gate Driver Sink Current		$V_{CSN} = V_{IN} - 250mV$, $V_{DRV} = 0.5 \times V_{CC}$		1		A
Gate Driver Output-Voltage High	V_{OH}	$I_{DRV} = 10mA$	$V_{CC} - 0.5$			V
Gate Driver Output-Voltage Low	V_{OL}	$I_{DRV} = -10mA$			0.5	V
DIM INPUT						
Maximum DIM Frequency	f_{DIM}			20		kHz
DIM Input-Voltage High	V_{IH}	$V_{CSN} = V_{IN}$, increase DIM until $V_{DRV} > (V_{CC} - 0.5V)$	2.8			V
DIM Input-Voltage Low	V_{IL}	$V_{CSN} = V_{IN}$, decrease DIM until $V_{DRV} < 0.5V$			0.6	V
DIM Hysteresis	DIM_{HYS}			200		mV
DIM Turn-On Time	t_{DIMON}	DIM rising edge to $V_{DRV} = 0.5 \times V_{CC}$, $C_{DRV} = 1nF$		100		ns
DIM Turn-Off Time	t_{DIMOFF}	DIM falling edge to $V_{DRV} = 0.5 \times V_{CC}$, $C_{DRV} = 1nF$		100		ns
DIM Input Leakage High		$V_{DIM} = V_{IN}$			10	μA
DIM Input Leakage Low		$V_{DIM} = 0V$	-1		+1	μA
VCC REGULATOR						
Regulator Output Voltage	V_{CC}	$I_{VCC} = 0.1mA$ to $10mA$, $V_{IN} = 5.5V$ to $28V$	4.5		5.5	V
		$I_{VCC} = 0.1mA$ to $10mA$, $V_{IN} = 4.5V$ to $28V$	4.0		5.5	V
Load Regulation		$I_{VCC} = 0.1mA$ to $10mA$, $V_{IN} = 12V$		4		Ω
Line Regulation		$V_{IN} = 6V$ to $28V$, $I_{VCC} = 10mA$		11		mV
Power-Supply Rejection Ratio	PSRR	$V_{IN} = 12V$, $I_{VCC} = 5mA$, $f_{IN} = 10kHz$		-35		dB
Current Limit	I_{LIM}	$V_{IN} = 4.5V$, $V_{CC} = 0V$		45		mA
		$V_{IN} = 4.5V$, $V_{CC} = 4V$		18		
Regulator Startup Time	t_{START}	$V_{CC} = 0$ to $4.5V$		350		μs

Note 1: All devices are 100% production tested at $T_J = +25^\circ C$ and $+125^\circ C$. Limits to $-40^\circ C$ are guaranteed by design.

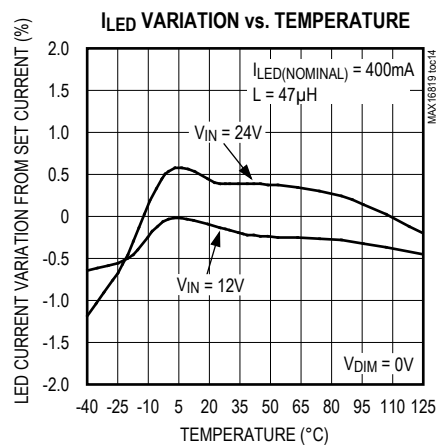
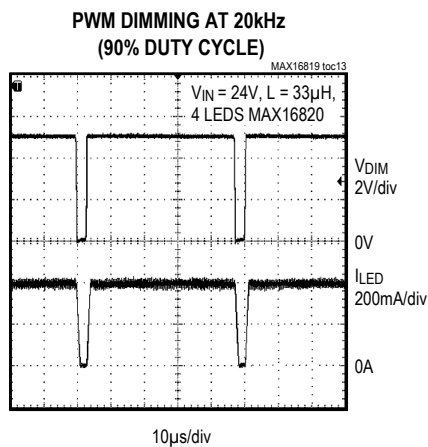
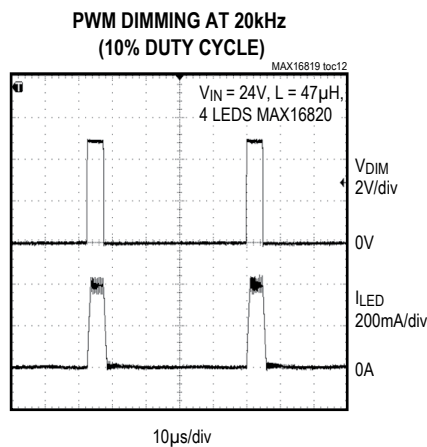
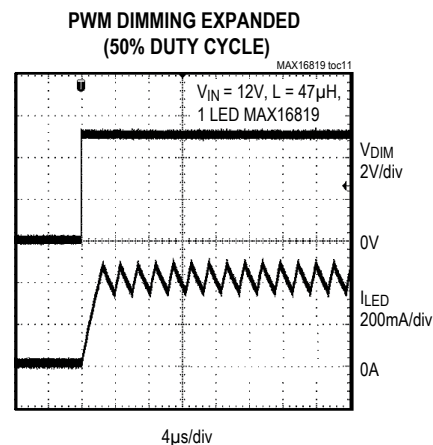
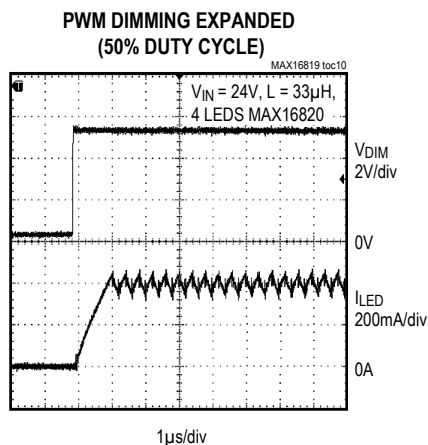
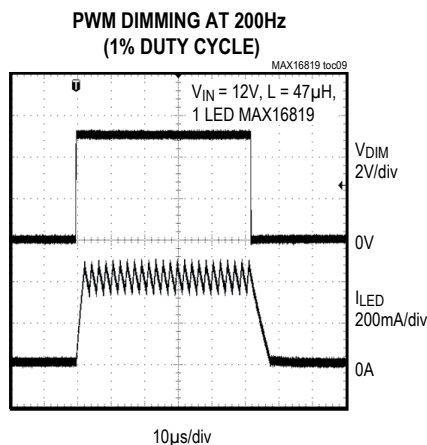
Typical Operating Characteristics

($V_{IN} = V_{DIM} = 12V$, $C_{VCC} = 1\mu F$, $R_{SENSE} = 0.5\Omega$ connected between IN and CSN. Typical values at $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

($V_{IN} = V_{DIM} = 12V$, $C_{VCC} = 1\mu F$, $R_{SENSE} = 0.5\Omega$ connected between IN and CSN. Typical values at $T_A = +25^\circ C$, unless otherwise noted.)



PIN	NAME	FUNCTION
1	IN	Positive Supply Voltage Input. Bypass with a 1μF or higher value capacitor to GND.
2	CSN	Current-Sense Input
3	DIM	Logic-Level Dimming Input. Drive DIM low to turn off the current regulator. Drive DIM high to enable the current regulator.
4	GND	Ground
5	DRV	Gate Drive Output. Connect to the gate of an external n-channel MOSFET.
6	V _{CC}	Voltage Regulator Output. Connect a 1μF capacitor from V _{CC} to GND.
EP	—	Exposed Paddle. Connect to a large-area ground plane for improved power dissipation. Do not use as the only ground connection for the device.

The block diagram illustrates the internal architecture of the MAX16819 and MAX16820 LED driver IC. The circuit is powered by an input voltage (IN) which is regulated to V_{CC} by a REGULATOR block. A current sense (CS) signal is fed into a CS COMPARATOR, which compares it with a reference voltage from a BANDGAP REF block. The output of the CS COMPARATOR is connected to the CS pin of the GATE DRIVER. A UVLO COMPARATOR monitors the V_{CC} rail, with its non-inverting input set to a 1.23V reference from the BANDGAP REF block. The output of the UVLO COMPARATOR is connected to the UVLO pin of the GATE DRIVER. The GATE DRIVER block receives V_{CC} and GND inputs and produces the DRV output. A DIM signal is processed by a DIM BUFFER, whose output is connected to the DIM pin of the GATE DRIVER. The IC is identified as MAX16819 and MAX16820.

The MAX16819/MAX16820 are step-down, constant-current, high-brightness LED (HB LED) drivers. These devices operate from a 4.5V to 28V input voltage range and provide up to 0.5A of source and 1A of sink drive capability to the gate of an external MOSFET. A high-side current-sense resistor sets the output current and a

The high-side current-sensing scheme and on-board current-setting circuitry minimize the number of external components while delivering LED current with a $\pm 5\%$ accuracy, using a 1% sense resistor. See the *Functional Diagram*.

Undervoltage Lockout (UVLO)

The MAX16819/MAX16820 include a 4.5V undervoltage lockout (UVLO) with 500mV hysteresis. When V_{IN} falls below 4.5V, DRV goes low, turning off the external n-channel MOSFET. DRV goes high once V_{IN} is 5V or higher.

5V Regulator

V_{CC} is the output of a 5V regulator capable of sourcing 10mA. Bypass V_{CC} to GND with a 1 μ F capacitor.

DIM Input

The MAX16819/MAX16820 allow dimming with a PWM signal at the DIM input. A logic level below 0.6V at DIM forces the MAX16819/MAX16820's DRV output low, turning off the LED current. To turn the LED current on, the logic level at DIM must be at least 2.8V.

Applications Information**Selecting R_{SENSE} to Set the LED Current**

The MAX16819/MAX16820 feature a programmable LED current using a resistor connected between IN and CSN. Use the following equation to calculate the sense resistor:

$$R_{SENSE}(\Omega) = \frac{1(V_{SNSHI} + V_{SNSLO})(V)}{2 I_{LEAD}(A)}$$

For the values of V_{SNSHI} and V_{SNSLO} , see the *Electrical Characteristics*.

Current Regulator Operation

The MAX16819/MAX16820 regulate the LED output current using an input comparator with hysteresis (Figure 1). As the current through the inductor ramps up and the voltage across the sense resistor reaches the upper threshold, the voltage at DRV goes low, turning off the external MOSFET. The MOSFET turns on again when the inductor current ramps down through the freewheeling diode until the voltage across the sense resistor equals the lower threshold. Use the following equation to determine the operating frequency:

$$f_{SW} = \frac{(V_{IN} - n \times V_{LED}) \times n \times V_{LED} \times R_{SENSE}}{V_{IN} \times \Delta V \times L}$$

where n = number of LEDs, V_{LED} = forward voltage drop of one LED, and $\Delta V = (V_{SNSHI} - V_{SNSLO})$.

For proper component selection, please use the design tool available at: www.maximintegrated.com/MAX16819-20-Tool.

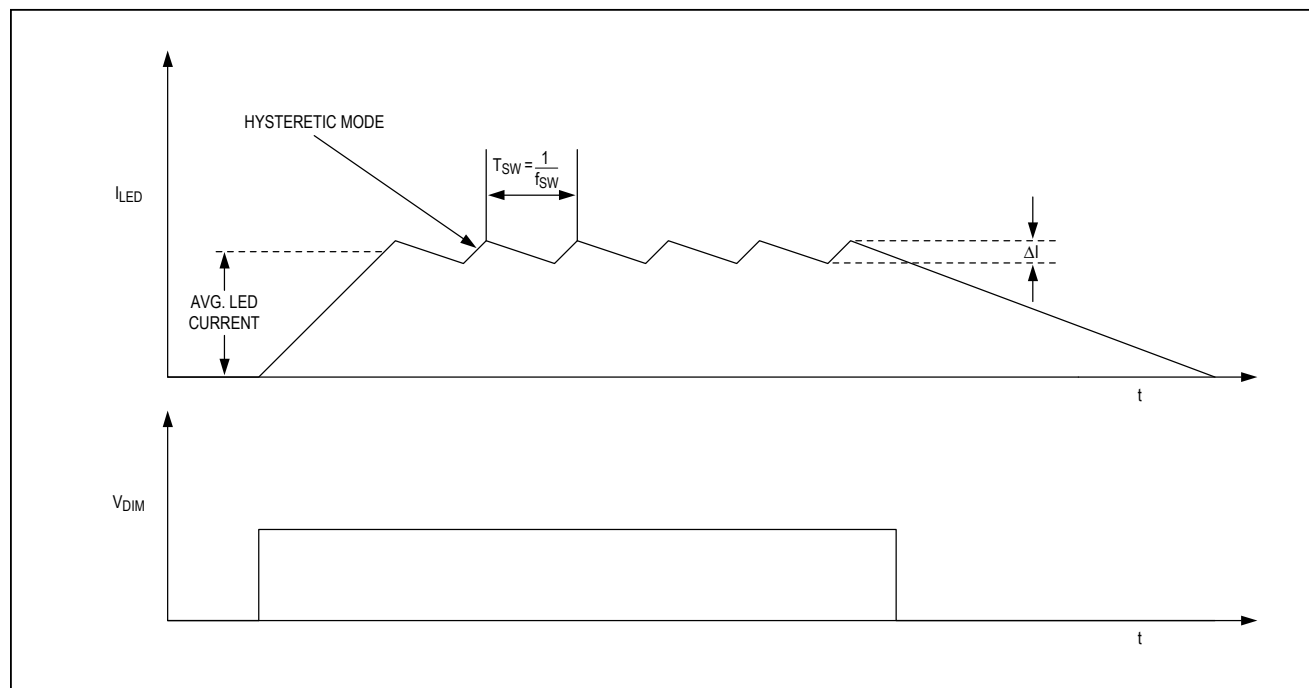


Figure 1. Current Regulator Operation

MOSFET Selection

The MAX16819/MAX16820's gate driver is capable of sourcing 0.5A and sinking 1A of current. MOSFET selection is based on the maximum input operating voltage V_{IN} , output current I_{LED} , and operating switching frequency. Choose a MOSFET that has a higher breakdown voltage than the maximum operation voltage, low $R_{DS(ON)}$, and low total charge for better efficiency. MOSFET threshold voltage must be adequate if operated at the low end of the input-voltage operating range.

Freewheeling Diode Selection

The forward voltage of the freewheeling diode should be as low as possible for better efficiency. A Schottky diode is a good choice as long as the breakdown voltage is high enough to withstand the maximum operating voltage.

The forward current rating of the diode must be at least equal to the maximum LED current.

LED Current Ripple

The LED current ripple is equal to the inductor current ripple. In cases when a lower LED current ripple is needed, a capacitor can be placed across the LED terminals.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and stable operation. Use a multilayer board whenever possible for better noise immunity. Minimize ground noise by connecting high-current ground returns, the input bypass-capacitor ground lead, and the output-filter ground lead to a single point (star ground configuration). In normal operation, there are two power loops. One is formed when the MOSFET is on and the high current flows through IN — R_{SENSE} —LEDs—Inductor—MOSFET—GND. The other loop is formed when the MOSFET is off when the high current circulates through R_{SENSE} —LEDs—Inductor—freewheeling diode. To minimize noise interaction, each loop area should be as small as possible.

Place R_{SENSE} as close as possible to the input filter and IN . For better noise immunity, a Kelvin connection is strongly recommended between CSN and R_{SENSE} . Connect the exposed paddle to a large-area ground plane for improved power dissipation.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 TDFN-EP	T633+2	21-0137	90-0058

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/06	Initial release	—
1	3/07	Revision	1, 4, 10
2	8/14	No /V OPNs; removed automotive reference from <i>Applications</i> and third line in <i>General Description</i> sections	1
3	2/15	Updated the <i>Benefits and Features</i> section	1
4	2/17	Corrected temp range for MAX16820ATT+T (from 40°C to +125°C to -40°C to +125°C) in <i>Ordering Information</i>	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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