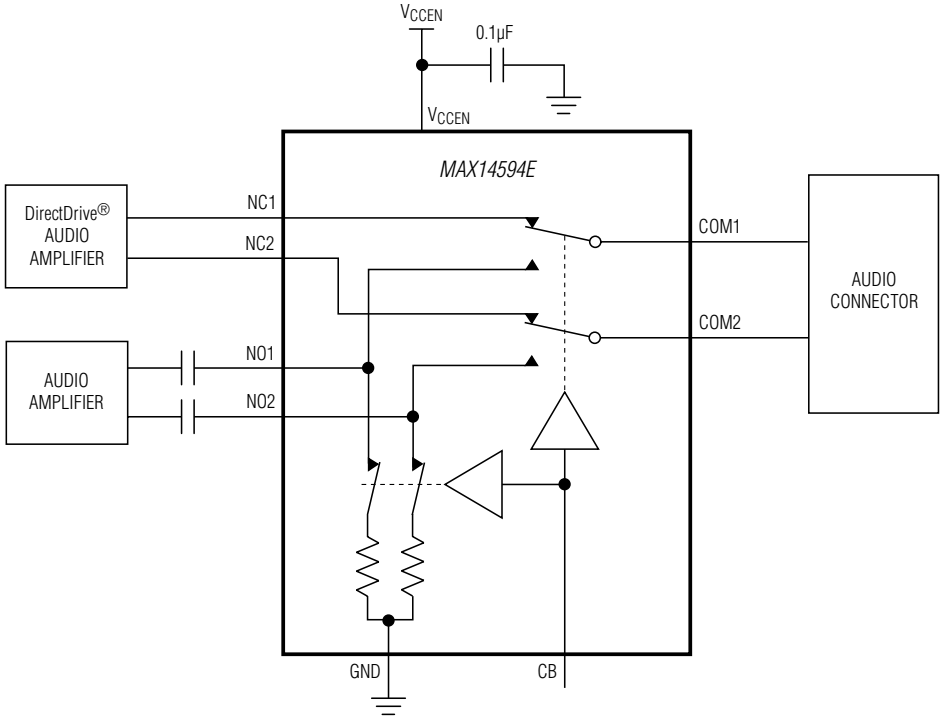
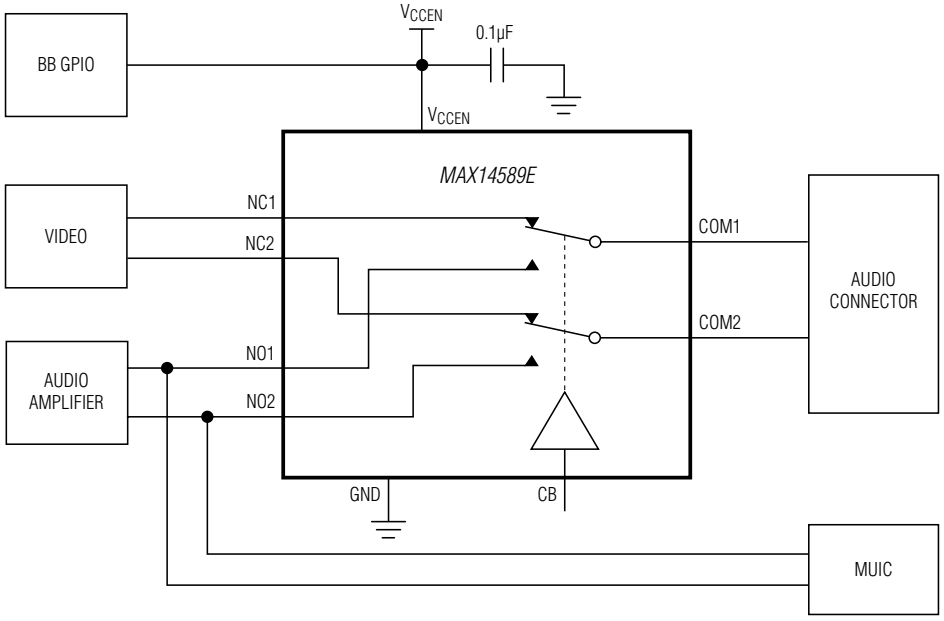
High-Density, ±5V Capable DPDT Analog Switches

Typical Application Circuits/Functional Diagrams



DirectDrive IS A REGISTERED TRADEMARK OF MAXIM INTEGRATED PRODUCTS, INC.



ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND.)

V_{CCEN}, CB .....-0.3V to +6V
NC_, NO_, COM_.....-6V to +6V
Continuous Current NC_, NO_, COM_..... ±500mA
Peak Current NC_, NO_, COM_ (50% duty cycle) ..... ±850mA

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 12mW/°C above +70°C).....963.8mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... ..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....83°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CCEN} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CCEN} = +2.5V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V_{CCEN}			1.6		5.5	V
PSRR		$R_{COM\_}$ = 32Ω, f = 20kHz			80		dB
V_{CCEN} Supply Current	I_{CC}	V_{CCEN} = +1.60V, V_{CB} = 0V or V_{CCEN}			30	50	µA
		V_{CCEN} = +4.2V, V_{CB} = 0V or V_{CCEN}			35	60	
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{NC\_}$, $V_{NO\_}$, $V_{COM\_}$	V_{CCEN} > 1.6V		-5.5		+5.5	V
		V_{CCEN} < 1.6V, R_S = 50Ω		-5.5		+5.5	
On-Resistance	R_{ON}	$V_{COM\_}$ = 0V, $I_{COM\_}$ = 100mA (Note 4)	V_{CCEN} = 2.5V		0.2	0.38	Ω
			V_{CCEN} = 1.8V		0.25	0.43	
On-Resistance Match Between Channels	$\Delta R_{ON(NC)}$	V_{CCEN} = 2.5V, $V_{NC\_}$ = 0V, $I_{COM\_}$ = 100mA, between same NC_ and NO_ channel (Note 5)			0.005	0.05	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CCEN} = 2.5V, $I_{COM\_}$ = 100mA, $V_{COM\_}$ = -5.5V to +5.5V (Notes 6, 7)			0.001	0.01	Ω
Shunt Switch Resistance	R_{SHUNT}	$I_{COM\_}$ = 1mA, MAX14594E			500	1000	Ω
NC_ or NO_ Off-Leakage Current	$I_{NC\_(OFF)}$, $I_{NO\_(OFF)}$	V_{CCEN} = 2.5V; open switch; $V_{NO\_}$ or $V_{NC\_}$ = -5.5V, +5.5V; $V_{COM\_}$ = +5.5V, -5.5V, unconnected		-400		+400	nA
		V_{CCEN} = 0V; $V_{NO\_}$ or $V_{NC\_}$ = 0V, +5.5V; $V_{COM\_}$ = +5.5V, 0V, unconnected		-400		+400	
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V_{CCEN} = 0V; $V_{COM\_}$ = +5.5V, 0V; $V_{NO\_}$ or $V_{NC\_}$ = 0V, +5.5V, unconnected		-400		+400	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.5V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V_{CCEN} = 2.5V; switch closed; $V_{COM\_}$ = +5.5V, -5.5V; $V_{NO\_}$ or $V_{NC\_}$ = +5.5V, -5.5V, unconnected	-400		+400	nA
DYNAMIC TIMING						
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 0V, R_L = 50Ω, Figure 1a (Note 6)		5	10	ms
Turn-Off Time	t_{OFF}	$V_{NO\_}$ or $V_{NC\_}$ = 0V, R_L = 50Ω, Figure 1a (Note 6)		1	2.25	ms
Break-Before-Make Time	t_{BBM}	R_L = 50Ω, V_{CCEN} = 3.3V, time for both NC_/NO_ switches are open during transition, Figure 1b (Note 6)	0	5	10	ms
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	f = 20Hz to 20kHz, $V_{COM\_}$ = 0.5V_{P-P}, R_S = R_L = 50Ω, DC bias = 0V		0.001		%
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω, $V_{COM\_}$ = 0.5V_{P-P}, f = 100kHz, V_{CCEN} = 0V, DC bias = 0.25V, Figure 2		-60		dB
Crosstalk	V_{CT}	R_S = R_L = 50Ω, $V_{COM\_}$ = 0.5V_{P-P}, f = 100kHz, Figure 2 (Note 8)		-80		dB
-3dB Bandwidth (Note 9)	BW	R_S = R_L = 50Ω, $V_{NO\_/NC}$, $V_{COM\_}$ < 2V_{P-P}		200		MHz
NC_ or NO_ Off-Capacitance	$C_{NC\_(OFF)}$ $C_{NO\_(OFF)}$	$V_{NC\_/NO\_}$ = 0.5V_{P-P}, f = 1MHz		25		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	$V_{NC\_/NO\_}$ = 0.5V_{P-P}, f = 1MHz		50		pF
DIGITAL I/O (CB)						
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic-Low Voltage	V_{IL}				0.4	V
Input Leakage Current	I_{IN}	V_{CB} = 0V or V_{CCEN}	-1		+1	µA
ESD PROTECTION						
COM1, COM2		Human Body Model		±15		kV
		IEC 61000-4-2 Air-Gap Discharge		±10		
		IEC 61000-4-2 Contact Discharge		±8		
NO_, NC_		Human Body Model		±15		kV
All Other Pins		Human Body Model		±2		kV

Note 2: All specifications are 100% production tested at T_A = +25°C, unless otherwise noted. Specifications are over -40°C to +85°C and are guaranteed by design.
Note 3: Full analog voltage range supported for signal frequencies less than 50kHz applied to all signal pins.
Note 4: The same limits apply for $V_{COM\_}$ = -5.5V to +5.5V and are guaranteed by design.
Note 5: $\Delta R_{ON(MAX)} = |R_{ON(CH1)} - R_{ON(CH2)}|$.
Note 6: Guaranteed by design; not production tested.
Note 7: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.
Note 8: Between two switches.
Note 9: Full bandwidth supported for signal amplitudes less than 2V peak-to-peak applied to all signal pins.

High-Density, ±5V Capable DPDT Analog Switches

Timing Diagrams

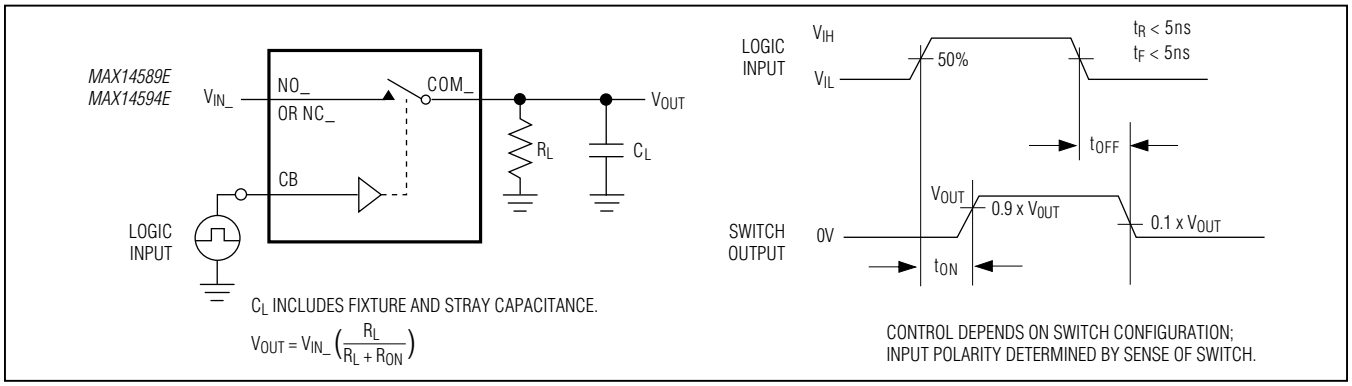


Figure 1a. Switching Time

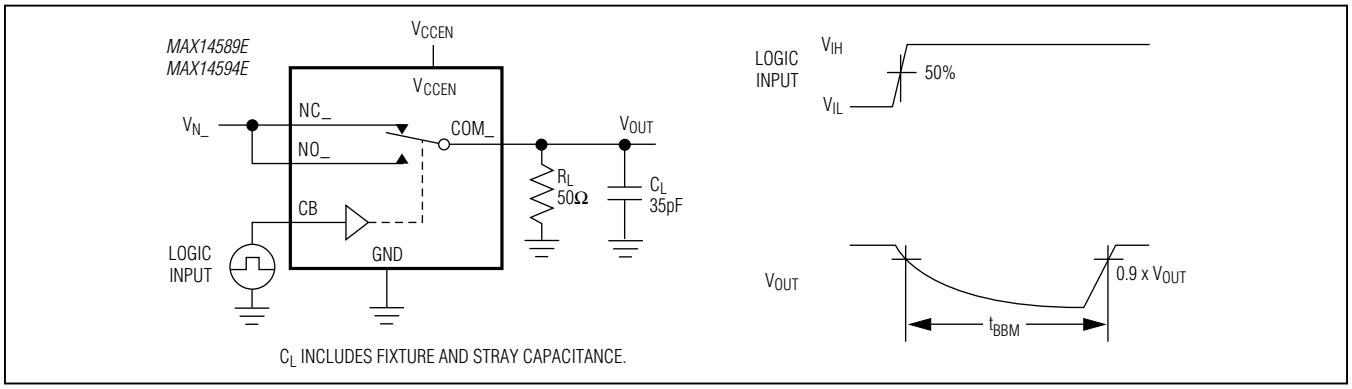


Figure 1b. Break-Before-Make Interval

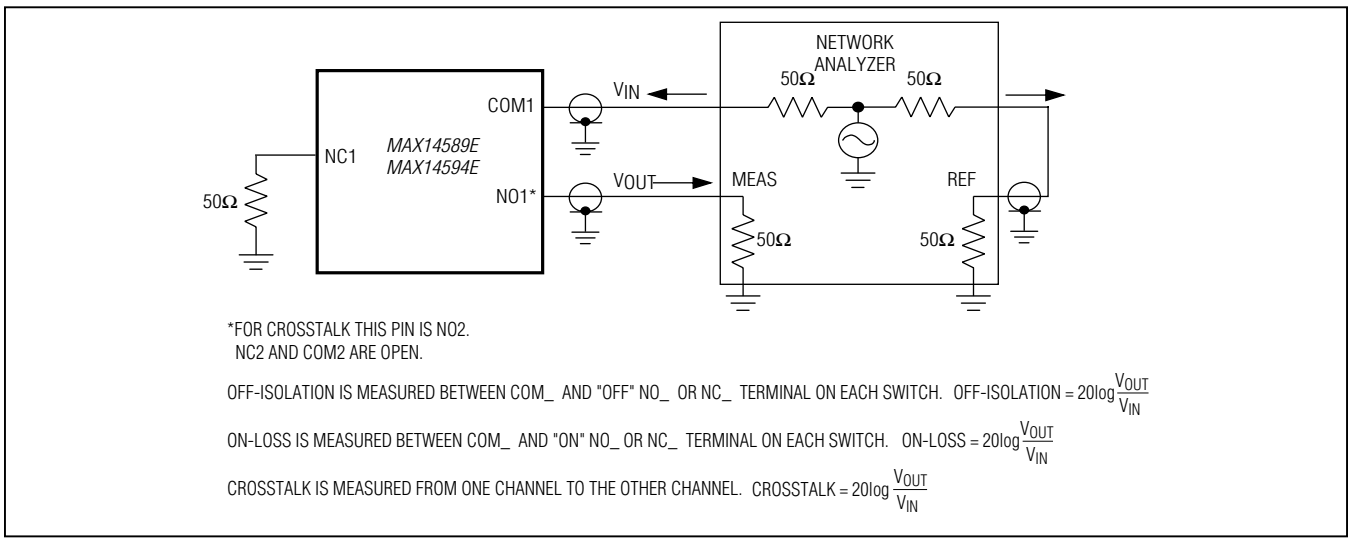


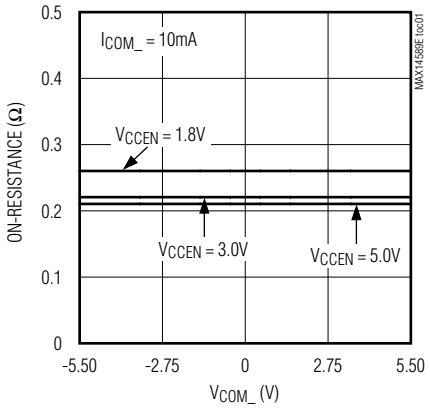
Figure 2. On-Loss, Off-Isolation, and Crosstalk

High-Density, ±5V Capable DPDT Analog Switches

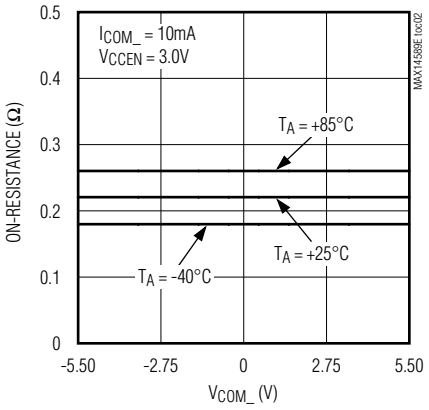
Typical Operating Characteristics

(V_{CCEN} = +2.5V, T_A = +25°C, unless otherwise noted.)

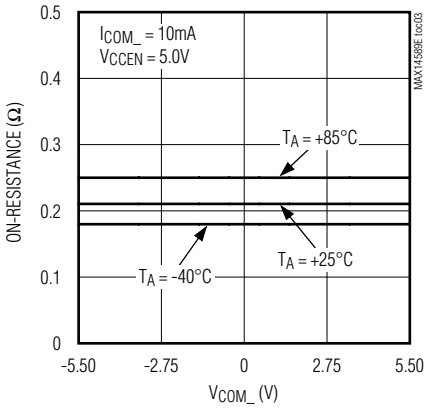
ON-RESISTANCE vs. COM_ VOLTAGE



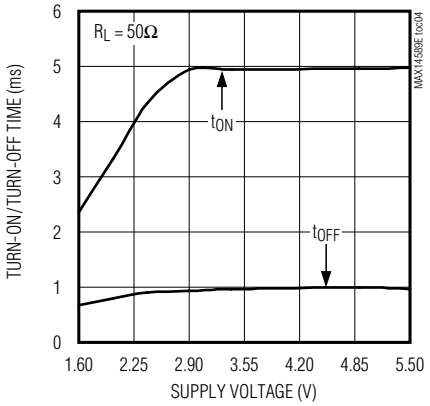
ON-RESISTANCE vs. COM_ VOLTAGE



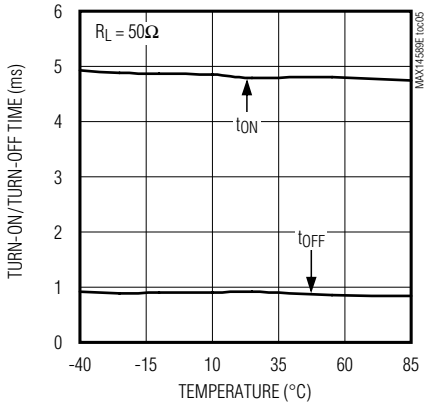
ON-RESISTANCE vs. COM_ VOLTAGE



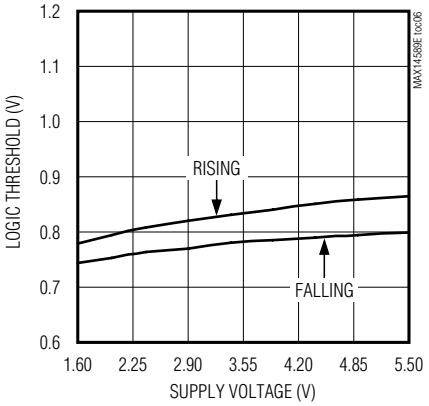
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



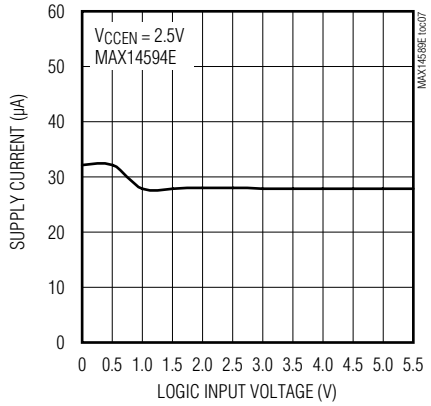
TURN-ON/TURN-OFF TIME vs. TEMPERATURE



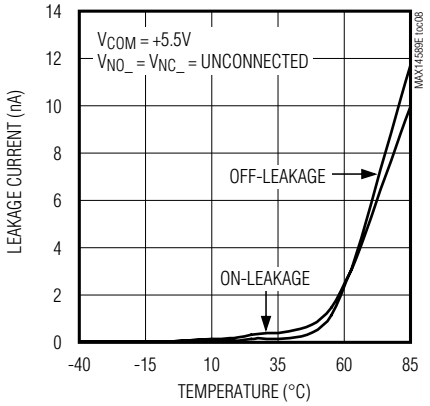
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



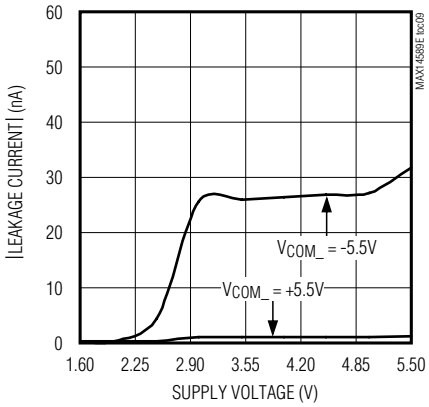
COM_ LEAKAGE CURRENT vs. TEMPERATURE



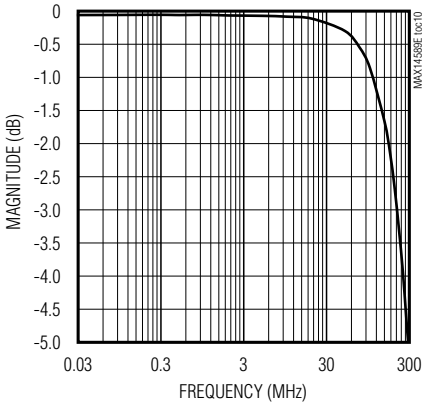
Typical Operating Characteristics (continued)

(V_{CCEN} = +2.5V, T_A = +25°C, unless otherwise noted.)

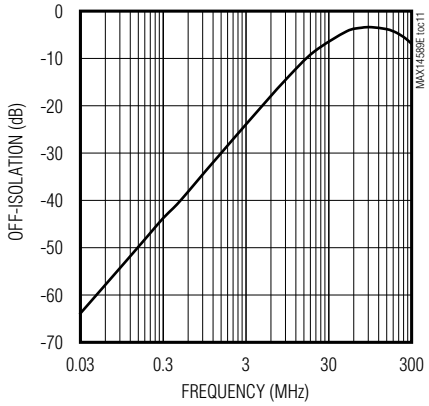
|COM_| LEAKAGE CURRENT vs. SUPPLY VOLTAGE



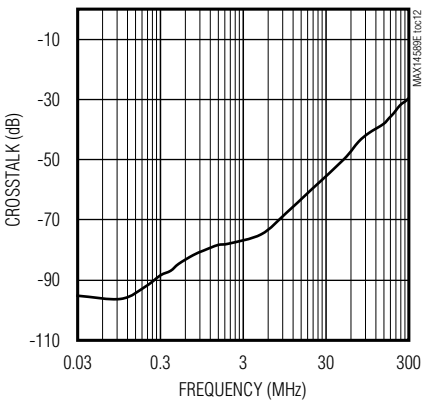
FREQUENCY RESPONSE*



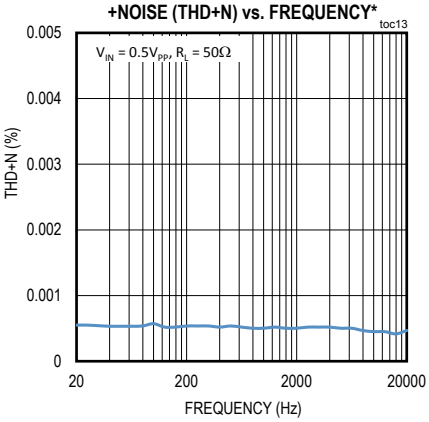
OFF-ISOLATION vs. FREQUENCY*



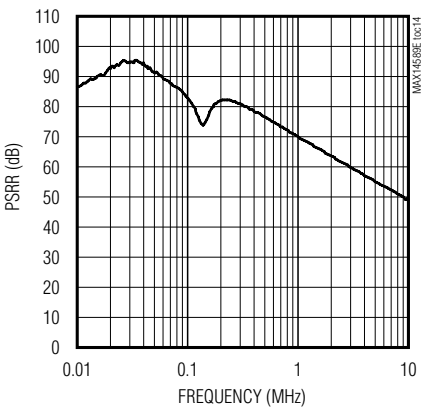
CROSSTALK vs. FREQUENCY*



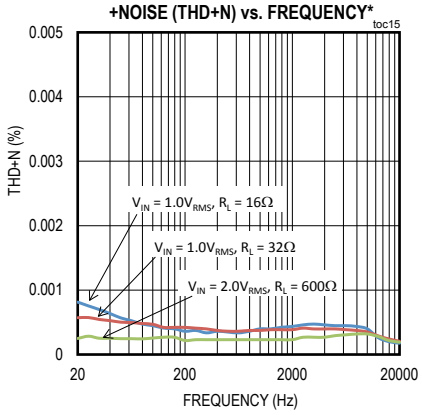
TOTAL HARMIC DISTORTION +NOISE (THD+N) vs. FREQUENCY*



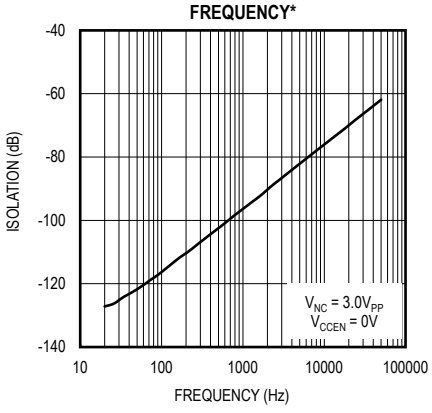
PSRR vs. FREQUENCY



TOTAL HARMONIC DISTORTION +NOISE (THD+N) vs. FREQUENCY*



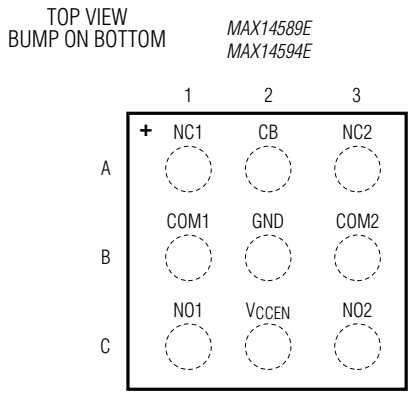
OFF-ISOLATION vs. FREQUENCY*



***Note:** Signals with frequencies greater than 50kHz are supported for amplitudes up to $2V_{P-P}$. Full analog voltage range supported for signal frequencies less than 50kHz applied to any signal pin.*

High-Density, ±5V Capable DPDT Analog Switches

Bump Configuration



WLP

Bump Description

BUMP	NAME	FUNCTION
A1	NC1	Normally Closed Terminal for Switch 1
A2	CB	Digital Control Input. Drive CB low to connect COM_ to NC_. Drive CB high to connect COM_ to NO_.
A3	NC2	Normally Closed Terminal for Switch 2
B1	COM1	Common Terminal for Switch 1
B2	GND	Ground
B3	COM2	Common Terminal for Switch 2
C1	NO1	Normally Open Terminal for Switch 1
C2	V_{CCEN}	Positive Supply Voltage Input. Bypass V_{CCEN} to GND with a 0.1µF capacitor as close as possible to the device.
C3	NO2	Normally Open Terminal for Switch 2

Detailed Description

The MAX14589E/MAX14594E are low on-resistance and high ESD-protected DPDT switches that operate from a +1.6V to +5.5V supply and are designed to multiplex AC-coupled analog signals. These switches feature the low on-resistance (R_{ON}) necessary for high-performance switching applications. The Beyond-the-Rails signal capability of the analog channel allows signals below ground, and above V_{CCEN}, to pass through without distortion.

Analog Signal Levels

The devices are bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs. The topology of the internal switches allows the signal to drop below ground without the need of an external negative voltage supply. **Note:** The devices can withstand analog signal levels of -5.5V to +5.5V when the device is not powered.

Digital Control Input

The devices provide a single-bit control logic input, CB. CB controls the switch position, as shown in the *Typical Application Circuits/Functional Diagrams*.

Click-and-Pop Suppression (MAX14594E Only)

The 500Ω shunt resistors automatically discharge any capacitance at both NO_ terminals when they are not connected to COM_. This reduces audio click-and-pop sounds that might occur when switching between capacitively coupled audio sources.

The shunt resistors are controlled by CB. When CB is low, NC_ is connected to COM_, and NO_ is connected to the shunt resistors. When CB is high, NO_ is connected to COM_ and the shunt resistors are unconnected.

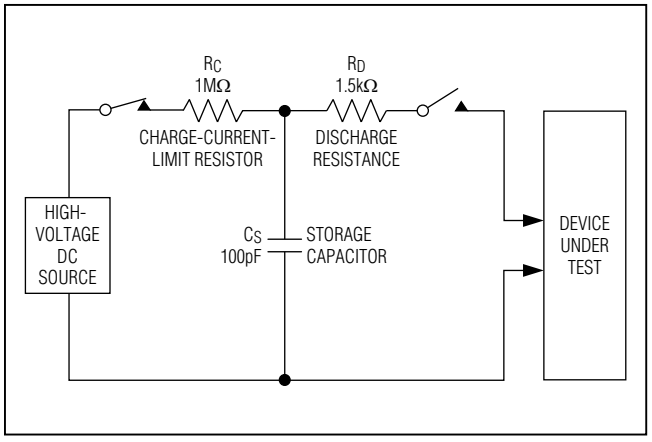


Figure 3. Human Body ESD Test Model

Applications Information

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. COM1 and COM2 are further protected against ESD up to ±15kV (HBM), ±10kV (Air-Gap Discharge), and ±8kV (Contact Discharge) without damage. NO_ and NC_ are further protected against ESD up to ±15kV (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the devices continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test methodology and test results.

Human Body Model

Figure 3 shows the Human Body Model. Figure 4 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM. Figure 4 shows the IEC 61000-4-2 model and Figure 5 shows the current waveform for the ±8kV, IEC 61000-4-2, Level 4, ESD Contact-Discharge Method.

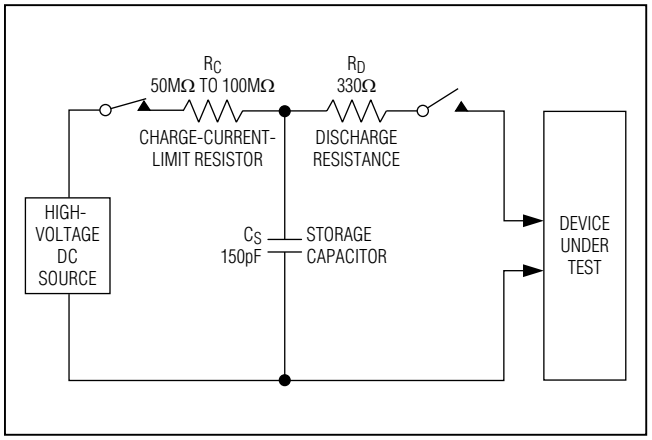


Figure 4. IEC 61000-4-2 ESD Test Model

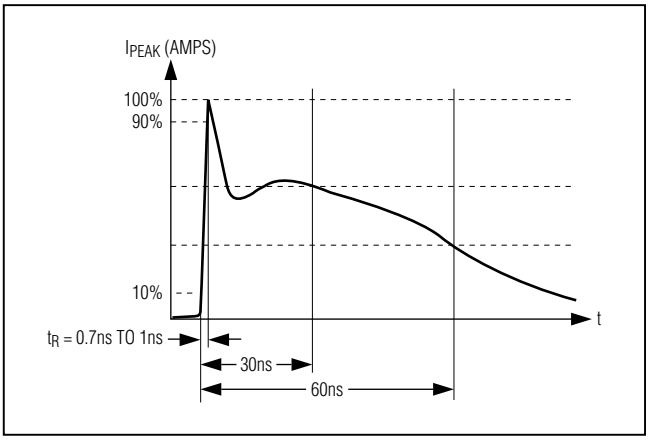


Figure 5. IEC 61000-4-2 ESD Generator Current Waveform

Chip Information

PROCESS: BiCMOS

Ordering Information/ Selector Guide

PART	PIN-PACKAGE	TOP MARK	SHUNT RESISTOR
MAX14589EEWL+T	9 WLP	AJA	No
MAX14594EEWL+T	9 WLP	AJB	Yes

Note: *All devices are specified over the -40°C to +85°C temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91B1+7	21-0459	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/12	Initial release	—
1	1/13	Updated *Electrical Characteristics* table, added note to TOCs	4, 7
2	7/14	Updated TOC 13, 15, 16	1, 7