ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
BAT, $\overline{INT}$, SDA, SCL, CE0, CE1, CE2, $\overline{EN}$ ..... -0.3V to +6.0V
LOUT ..... -0.3V to (V_B + 0.3V, 6V) (min)
V_B ..... -0.3V to +30V
Switch Disabled or CP_ENA = 1 (Note 1)
CD+, CD- ..... -2.1V to (V_{SWPOS} + 0.3V)
TD+, TD- ..... -0.3V to (V_{SWPOS} + 0.3V)
Switch Enabled or CP_ENA = 0 (Note 2)
CD+, CD-, TD+, TD- ..... -0.3V to (V_{VCCINT} + 0.3V)

Continuous Current into LOUT ..... ±150mA
Continuous Current into Any Other Terminal ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 13.7mW/°C above +70°C) 1096mW
TQFN (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: V_{SWPOS} = (V_{VCCINT} or 3.3V) (min)
Note 2: V_{VCCINT} = (V_{BAT}, [(V_B or 4.2V) (min)]) (max)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 3)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 73°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 10°C/W

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Voltage Range	V_{BAT}			2.8		5.5	V
	V_B			3.5		28	
Internal Positive Switch Regulator	V_{SWPOS}			3.25	3.4	3.6	V
Internal Negative Switch Regulator	V_{SWNEG}			-2.06	-1.90	-1.76	V
V_{BAT} UVLO	$V_{BATUVLO}$	V_{BAT} = 4.2V, V_B = 0V		0.90	1.65	2.45	V
V_{BUS} UVLO	$V_{BUSUVLO}$	V_{BAT} = 0V, V_B = 5.5V		1.0	1.33	3.30	V
BAT Supply Current	I_{BAT}	MAX14578E	V_{BAT} = +3.6V, V_B = 0V, CP_ENA = 0, USBSWC = 0		1	2.5	µA
			V_{BAT} = +4.2V, V_B = 0V, CP_ENA = 1, USBSWC = 1, V_{SDA} = V_{SCL} = 1.8V		34.5	59	

ELECTRICAL CHARACTERISTICS (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT Supply Current	I_{BAT}	MAX14578AE	V_{BAT} = +3.6V, $V_B < V_{VBRAW}$, $V_{\overline{EN}}$ = +3.6V		1	2.5	µA
			V_{BAT} = +4.2V, V_B = 0V, $V_{\overline{EN}}$ = 0V		1.3	30	
			Supply current increase when $V_{\overline{EN}}$ = 1.6V, V_{BAT} = +4.2V		1.3	3.5	
V_B Supply Current	I_{VB}	MAX14578E	V_B = +5.5V, CP_ENA = 0, USBSWC = 0		87	140	µA
		MAX14578AE	V_B = +5.5V, $V_{\overline{EN}}$ = 0V		190	295	µA
			V_B = +5.0V, $V_{\overline{EN}}$ = 0V		4.1		mA
			V_B = +5.5V, $V_{\overline{EN}}$ = +5.5V		75	125	µA
LOUT (LDO OUT) (MAX14578AE ONLY)							
LOUT Current Limit	I_{LOUT}				95		mA
LOUT Voltage	V_{LOUT}	I_{LOUT} = 10mA, V_B = 5.0V		4.87	4.94		V
		I_{LOUT} = 0mA, V_B = 6.0V		4.0	5.3	5.5	
LOUT Debounce Time	t_{LOUT_DEB}	V_B = 5.0V to V_{LOUT} = 4.5V			20		ms
LOUT Turn-On Time					100		µs
Themal Shutdown					+141		°C
Themal Shutdown Hysteresis					20		°C
CHARGER DETECTION							
V_{DP_SRC} Voltage	V_{DP_SRC}			0.5		0.7	V
V_{DAT_REF} Voltage	V_{DAT_REF}			0.25		0.4	V
V_{LGC} Voltage	V_{LGC}			0.8		2.0	V
I_{DP_SRC} Current	I_{DP_SRC}			6.6		11	µA
CD+ and CD- Sink Current	I_{CD+_SINK} I_{CD-_SINK}			50		150	µA
R_{CD} Resistance	R_{CD}			200	330	500	kΩ
TD+ Pulldown Resistor	R_{TD+_DWN}			15	20	25	kΩ
TD- Pulldown Resistor	R_{TD-_DWN}			14.25		24.8	kΩ
Charger Detection Weak Sink	I_{WEAK}					0.18	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS25 Ratio	VBUS25	Reference ratio for special charger as a percentage of V_{BUS} voltage, V_B = 5V	24	26	29	%
VBUS47 Ratio	VBUS47	Reference ratio for special charger as a percentage of V_{BUS} voltage, V_B = 5V	44	47	50	%
VBUS60 Ratio	VBUS60		57.5	60.3	63.5	%
DCD M Time	t_{MDEB}	All comparators	20	30	40	ms
DCD C Time	t_{CDEB}	All comparators			5	ms
DCD Timer				2		s
Charger-Detect Source Time	$t_{DP\_SRC\_ON}$	DCHK = 0		40		ms
		DCHK = 1		625		
Charger-Detect-Type Detection Time	$t_{DP\_RES\_ON}$		120			ms
Charger-Detect Delay Time	$t_{DP\_SRC\_HICRNT}$		40		80	ms
V_B Attach to CE1 and CE2 Output Time	t_{VBSW}	From V_B > V_{VBDET} or CHG_TYP_M = 1 (DCHK = 0) to CE1 and/or CE2 change			520	ms
		From V_B > V_{VBDET} or CHG_TYP_M = 1 (DCHK = 1) to CE1 and/or CE2 change			1450	
V_B Raw-Detect Threshold	V_{VBRAW}		1.7	2.6	3.5	V
V_B-Detect Threshold	V_{VBDET}		3.2	3.5	3.3	V
V_B-Detect Threshold Hysteresis	V_{VBDET_HYS}		38	50		mV
USB ANALOG SWITCHES (CD-, CD+)						
Analog-Signal Range	V_{DN2}, V_{DP2}	CP_ENA = 0 (MAX14578E)	0		V_{VCCINT}	V
		CP_ENA = 1	V_{SWNEG}		V_{SWPOS}	
On-Resistance	R_{ONUSB}	V_{BAT} = +3.0V, I_{CD+} = I_{CD-} = 10mA, V_{CD+}, V_{CD-} = 0 to +3.0V		3.3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	V_{BAT} = +3.0V, I_{CD+} = I_{CD-} = 10mA, V_{CD+}, V_{CD-} = +400mV			0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	V_{BAT} = +3.0V, I_{CD+} = I_{CD-} = 10mA, V_{CD+}, V_{CD-} = 0 to +3.3V		0.06	0.26	Ω
Off-Leakage Current	$I_{LUSB(OFF)}$	V_{BAT} = 4.2V, switch open, V_{CD+} = V_{CD-} = +0.3V or +2.5V; V_{TD+} or V_{TD-} = +2.5V or +0.3V	-360		+360	nA
On-Leakage Current	$I_{LUSB(ON)}$	V_{BAT} = 4.2V, switch closed, V_{CD+} or V_{CD-} = +0.3V or +2.5V	-360		+360	nA
DIGITAL SIGNALS ($\overline{INT}$, SCL, SDA, $\overline{EN}$, CE0, CE1, CE2)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current	I_{INLEAK}		-1		+1	µA
Open-Drain Low	V_{ODOL}	I_{SINK} = 1mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{BAT} = +2.8V to +5.5V, V_B = +3.5V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = +3.6V, V_B = +5.0V, T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-High	V_{OH}	I_{SOURCE} = 1mA	V_{IO} - 0.2			V
Output Logic-Low	V_{OL}	I_{SINK} = 1mA			0.2	V
DYNAMIC (Note 5)						
Charge-Pump Delay Time	t_{CP}	CP_ENA from 0 to 1 until switch on			1	ms
Analog-Switch Turn-On Time	t_{ON}	MAX14578E, I²C STOP to switch on, R_L = 50Ω		0.1	1	ms
Analog-Switch Turn-Off Time	t_{OFF}	MAX14578E, I²C STOP to switch off, R_L = 50Ω		0.1	1	ms
Break-Before-Make Delay Time	t_{BBM}	R_L = 50Ω, T_A = +25°C	> 0			µs
Off-Capacitance	C_{OFF}	TD-, TD+, applied voltage is 0.5V_{P-P}, DC bias = 0V, f = 240MHz; CD-, CD+ not connected to TD-, TD+		2		pF
On-Capacitance	C_{ON}	TD-, TD+, applied voltage is 0.5V_{P-P}, DC bias = 0V, f = 240MHz; CD-, CD+ connected to TD-, TD+; R_L = 50Ω		4.5		pF
-3dB Bandwidth	BW	$V_{CD\_}$ = 0.5V_{P-P}		1000		MHz
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 20kHz, $V_{CD\_}$ = 0.5V_{P-P}		-60		dB
I²C TIMING SPECIFICATIONS						
I²C Max Clock	f_{I2CCLK}			400		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Setup Time			0.6			µs
Repeat START Condition Setup Time	$t_{SU:STA}$	90% to 90%	0.6			µs
START Condition Hold Time	$t_{HD:STA}$	10% of SDA to 90% of SCL	0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	0.6			µs
Clock Low Period	t_{LOW}	10% to 10%	1.3			µs
Clock High Period	t_{HIGH}	90% to 90%	0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write setup time	100			ns
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write hold time			0	ns
ESD PROTECTION						
CD+, CD-		Human Body Model		±15		kV
		IEC 61000-4-2 Contact Discharge		±8		

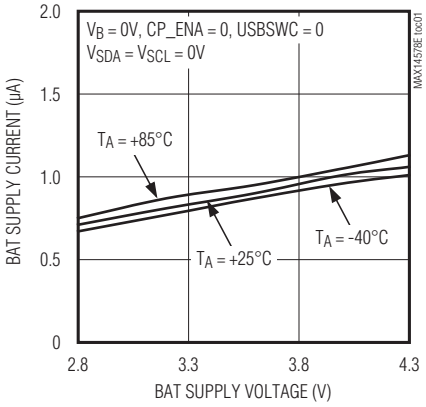
Note 4: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 5: Guaranteed by design; not production tested.

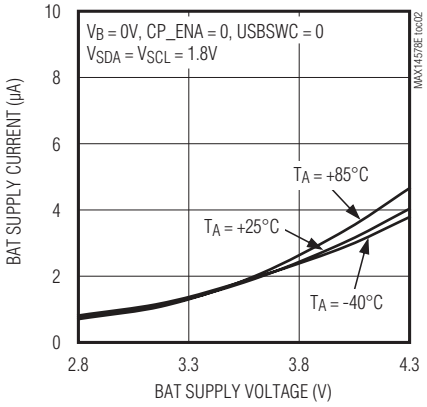
Typical Operating Characteristics

(V_{BAT} = +4.2V, V_B = +5.0V, C_{BAT} = 1µF, C_{VB} = 1µF, unless otherwise noted.)

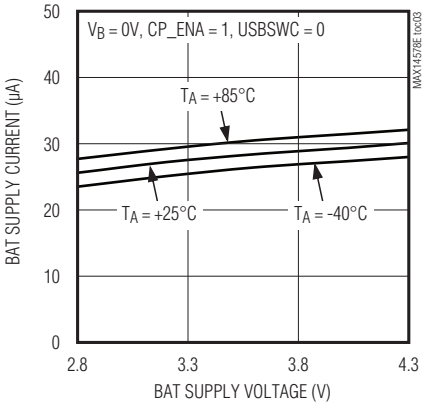
BAT SUPPLY CURRENT vs. SUPPLY VOLTAGE



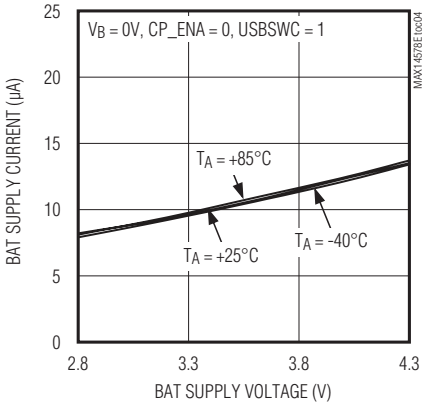
BAT SUPPLY CURRENT INCREASE vs. SUPPLY VOLTAGE



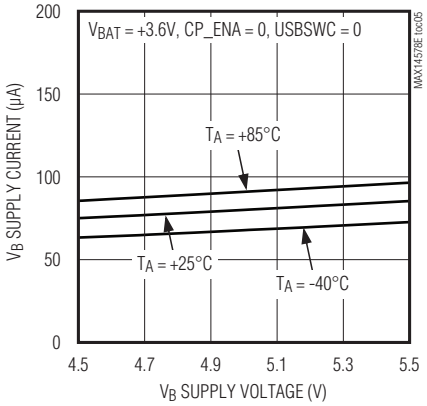
BAT SUPPLY CURRENT vs. SUPPLY VOLTAGE



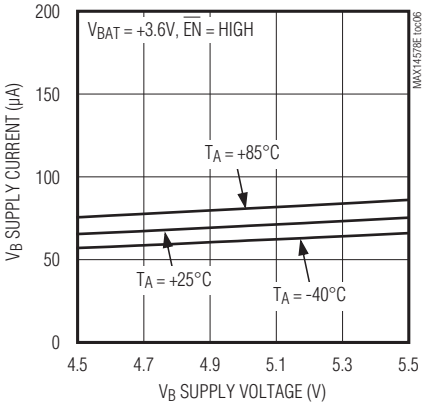
BAT SUPPLY CURRENT vs. SUPPLY VOLTAGE



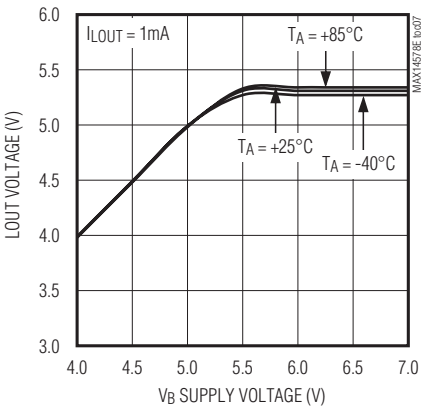
VB SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX14578E)



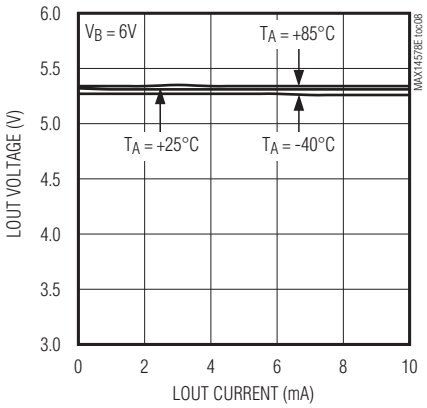
VB SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX14578AE)



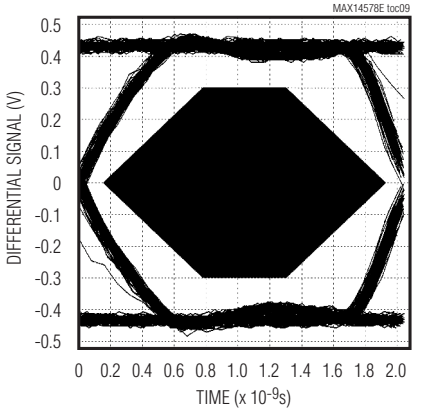
LOUT VOLTAGE REGULATION (MAX14578AE)



LOUT LOAD REGULATION (MAX14578AE)



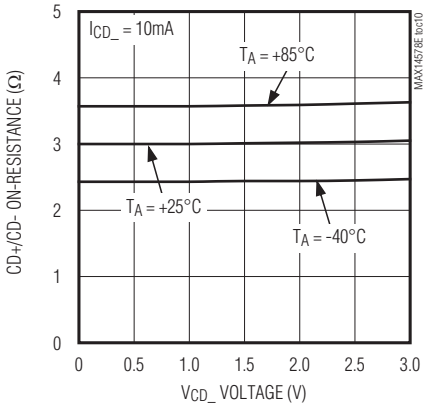
ANALOG-SWITCH EYE DIAGRAM



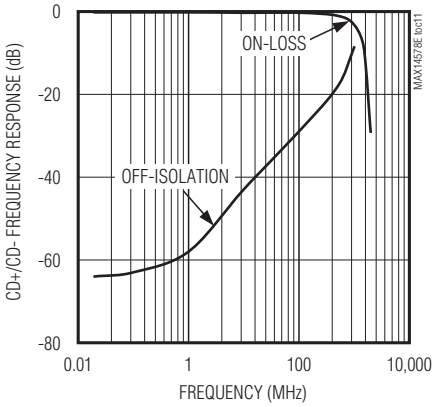
Typical Operating Characteristics (continued)

(V_{BAT} = +4.2V, V_B = +5.0V, C_{BAT} = 1µF, C_{VB} = 1µF, unless otherwise noted.)

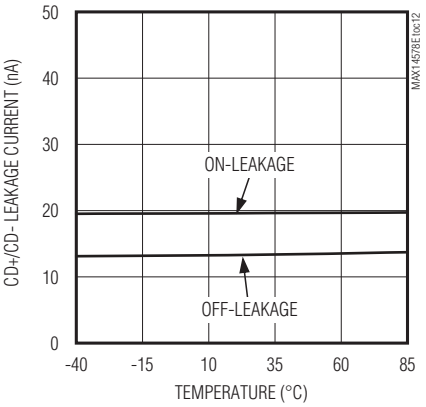
CD+/CD- ON-RESISTANCE vs. $V_{CD\_}$ VOLTAGE



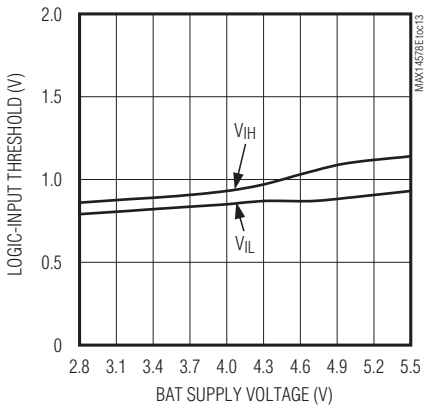
CD+/CD- FREQUENCY RESPONSE



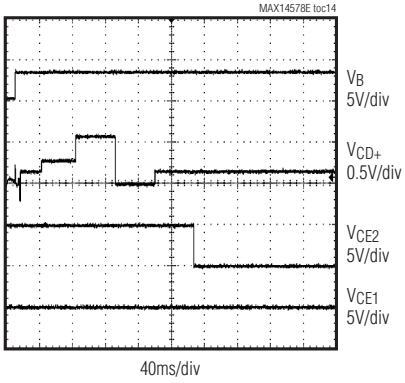
CD+/CD- LEAKAGE CURRENT vs. TEMPERATURE



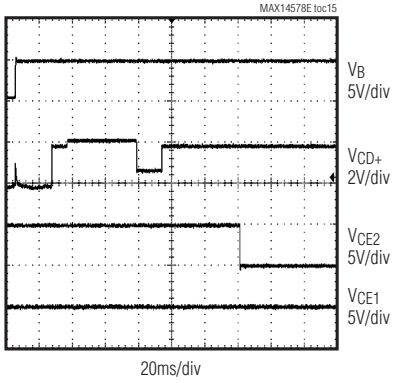
LOGIC-INPUT THRESHOLD vs. SUPPLY VOLTAGE



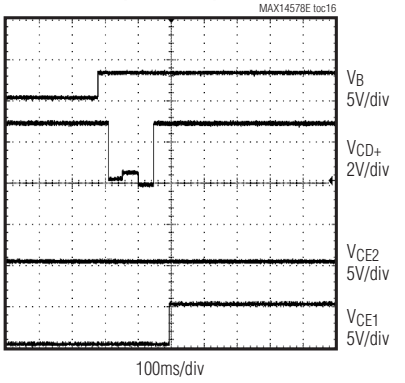
CE_ vs. V_{BUS} CONNECTION (MAX14578E) USB CHARGING DOWNSTREAM PORT, USB COMPLIANT (USB_CPL = 1, USBSWC = 0, V_{TD+} = 3V)



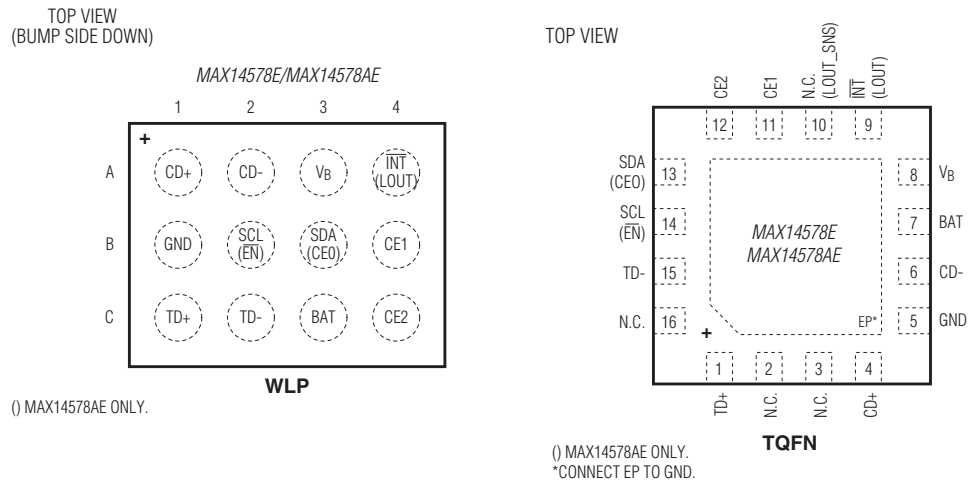
CE_ vs. V_{BUS} CONNECTION (MAX14578E) APPLE 1A CHARGER, USB COMPLIANT (USB_CPL = 1, USBSWC = 0, V_{TD+} = 3V)



CE_ vs. V_{BUS} CONNECTION (MAX14578AE) USB CHARGING DOWNSTREAM PORT (V_{TD+} = 3V)



Pin/Bump Configurations



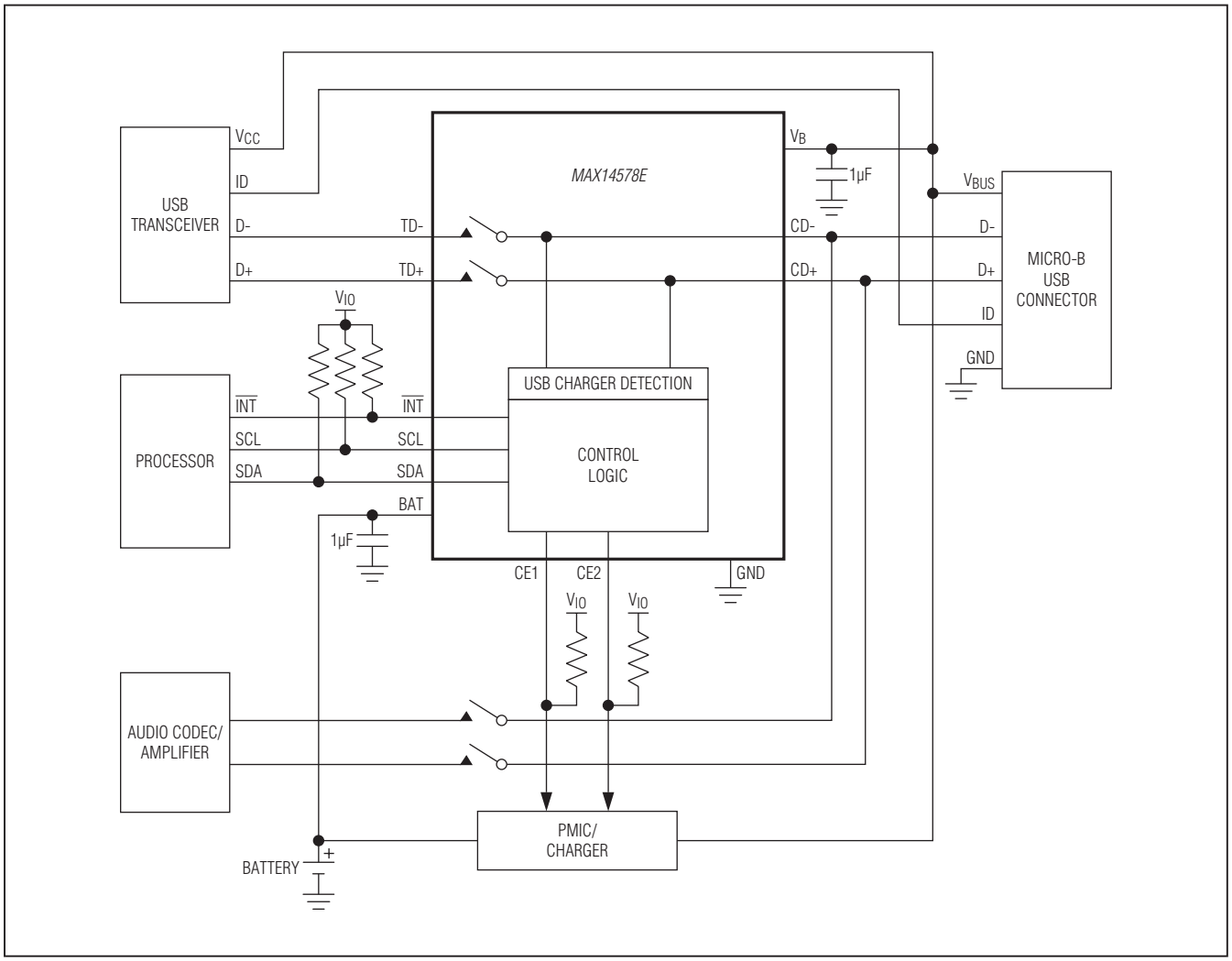
Pin/Bump Description

PIN				NAME	FUNCTION
MAX14578E		MAX14578AE			
TQFN-EP	WLP	TQFN-EP	WLP		
1	C1	1	C1	TD+	USB Transceiver D+ Connection
2, 3, 10, 16	—	2, 3, 16	—	N.C.	No Connection. Not internally connected.
4	A1	4	A1	CD+	USB Connector D+ Connection
5	B1	5	B1	GND	Ground
6	A2	6	A2	CD-	USB Connector D- Connection
7	C3	7	C3	BAT	Battery Connection Input. Connect a 1µF capacitor as close as possible between BAT and GND.
8	A3	8	A3	V_B	USB Connector V_{BUS} Connection. Connect a 1µF capacitor as close as possible between V_B and GND for ±15kV ESD protection.
9	A4	—	—	$\overline{INT}$	Active-Low Interrupt Request, Open-Drain Output
—	—	9	A4	LOUT	+5.3V USB Transceiver V_{BUS} Power Output. Connect a 1µF capacitor as close as possible between LOUT and GND.
—	—	10	—	LOUT_SNS	Connect Externally to LOUT (MAX14578AE, TQFN Only)
11	B4	11	B4	CE1	Charger-Enable Control 1, Open-Drain Output
12	C4	12	C4	CE2	Charger-Enable Control 2, Open-Drain Output
13	B3	—	—	SDA	I^2C Serial-Data Input/Output. Connect SDA to an external pullup resistor.
—	—	13	B3	CE0	Charger-Enable Control 0, Open-Drain Output
—	—	14	B2	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ low to enable the charger ID detection and close the USB switches after charger detection is complete.

Pin/Bump Description (continued)

PIN				NAME	FUNCTION
MAX14578E		MAX14578AE			
TQFN-EP	WLP	TQFN-EP	WLP		
14	B2	—	—	SCL	I²C Serial-Clock Input. Connect SCL to an external pullup resistor.
15	C2	15	C2	TD-	USB Transceiver D- Connection
—	—	—	—	EP	Exposed Pad (TQFN Only). EP is internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

MAX14578E Functional Diagram/Typical Application Circuit



MAX14578AE Functional Diagram/Typical Application Circuit

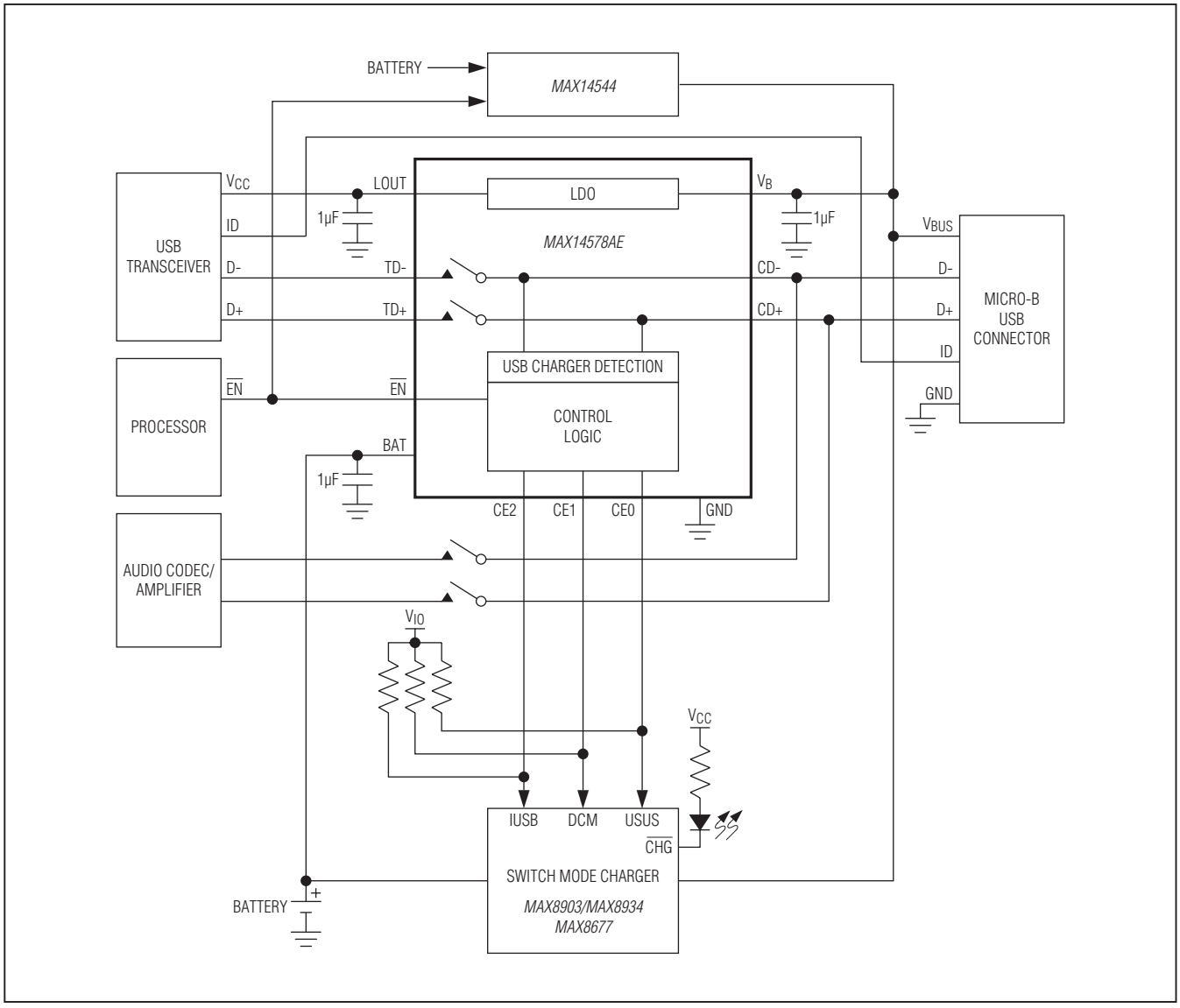


Table 1. Register Map

ADDRESS	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	DEVICE ID	VENDOR_ID				CHIP_REV			
0x01	CONTROL 1	INTPOL	INTEN	USBSWC	CP_ENA	LOW_POW	DCHK	CHG_TYP_M	USB_CHGDET
0x02	INTERRUPT	CHG_TYP			VBCOMP	DBCHG	DCD_T	CHGRUN	RFU
0x03	CONTROL 2	DCD_EN	DB_EXIT	DB_IDLE	SUS_LOW	CE_FRC	CE		
0x04	CONTROL 3	RFU	RFU	RFU	CDP_DET	USB_CPL	SFOUT_EN	SFOUTASRT	DCD_EXIT

Table 2. Detailed Register Map

FIELD NAME	READ/WRITE	BIT	DEFAULT	DESCRIPTION
DEVICE ID (I^2C ADDRESS = 0x00)				
VENDOR_ID	Read Only	[7:4]	0010	Vendor Identification
CHIP_REV	Read Only	[3:0]	0001	Chip Revision
CONTROL 1 (I^2C ADDRESS = 0x01)				
INTPOL	Read/Write	7	0	Interrupt Polarity 0 = Active low 1 = Active high
INTEN	Read/Write	6	0	Interrupt Enable. If interrupt is disabled, pending interrupts are not cleared and the $\overline{INT}$ pin deasserts. INTEN is a global setting to mask all interrupts. 0 = Interrupt disabled 1 = Interrupt enabled
USBSWC	Read/Write	5	0	Opens/Closes USB Switch 0 = Switch open 1 = Switch closed
CP_ENA	Read/Write	4	0	Charge-Pump Enable 0 = Charge pump disabled 1 = Charge pump enabled
LOW_POW	Read/Write	3	1	Low-Power Mode 0 = Low-power mode disabled; oscillator/bandgap always on 1 = Low-power mode enabled; oscillator/bandgap turned off under the following conditions: no V_{BUS}, USBSWC = 0, and CP_ENA = 0
DCHK	Read/Write	2	0	Charger-Type Source-Detection Time 0 = DCHK, $t_{DP\_SRC\_ON}$ = 40ms 1 = DCHK, $t_{DP\_SRC\_ON}$ = 625ms
CHG_TYP_M	Read/Write	1	0	Charger-Type Manual-Detection Enable. Set CHG_TYP_M to 1 to force the internal logic to open the USB switches and perform a charger-type detection. After the detection state matching completes, this bit resets to 0. 0 = Charger detection disabled 1 = Force a manual charge detection

Table 2. Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BIT	DEFAULT	DESCRIPTION
USB_CHGDET	Read/Write	0	1	Charger-Detection-Enable Start. Charger detection starts with any change in V_B. 0 = Charger detection disabled 1 = Charger detection enabled
INTERRUPT (I^2C ADDRESS = 0x02)				
CHG_TYP	Read Only	[7:5]	000	Output of USB Charger Detection 000 = Nothing attached 001 = USB cable attached 010 = Charging dowstream port: current depends on USB operating speed 011 = Dedicated charger: current up to 1.8A 100 = Special charger: 500mA max 101 = Special charger: current up to 1A 110 = RFU 111 = Dead-battery charging: 100mA max
VBCOMP	Read Only	4	0	Output of V_B Comparator. Changes in VBCOMP triggers interrupt. 0 = $V_B < V_{VBDET}$ 1 = $V_B \geq V_{VBDET}$
DBCHG	Read Only	3	0	Dead-Battery Charger Mode. If DBCHG = 1, the 45-minute timer is running. 0 = Not in dead-battery charge mode 1 = In dead-battery charge mode
DCD_T	Read Only	2	0	Data-Contact Detection (DCD) Time Wait. DCD_T generates an interrupt after a 0-to-1 transition. 0 = Data contact detection not running 1 = Data contact detection running for > 2s
CHGRUN	Read Only	1	0	Charger-Detection State Machine Running. For information only—no interrupt generated. 0 = Charger detection not running 1 = Charger detection running (DCD, dead battery, D+/D- short)
RFU	Read Only	0	0	Reserved
CONTROL 2 (I^2C ADDRESS = 0x03)				
DCD_EN	Read/Write	7	1	DCD Enable. If DCD_EN = 1, D+/D- is tested for a short after DCD passes. If DCD_EN = 0, DCD is skipped and D+/D- short detection begins when V_{BUS} is connected or CHG_TYP_M = 1. If DCD is stuck (DCD_T) = 1, setting DCD_EN = 0 bypasses DCD and D+/D- short detection begins. 0 = Disabled 1 = Enabled

Table 2. Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BIT	DEFAULT	DESCRIPTION
DB_EXIT	Read/Write	6	0	Exit Dead-Battery Charge Mode. If DBCHG = 1, setting DB_EXIT to 1 stops the 45-minute timer, sets DBCHG to 0, and leaves CHG_EN = 1. DB_EXIT is automatically reset to 0 if V_{BAT} reaches the dead-battery threshold. 0 = Do not exit dead-battery mode 1 = Exit dead-battery mode
DB_IDLE	Read/Write	5	0	Dead-Battery Idle Mode. DB_IDLE = 1 in dead-battery mode to forces the USB switch to close. DB_IDLE is automatically reset when the USB switch is closed. 0 = Dead-battery mode off or test completed 1 = Dead-battery mode on or test still needed
SUS_LOW	Read/Write	4	0 (1)*	Suspend Mode Selection 0 = When the charger is disabled, CE1 = CE2 = 1 1 = When the charger is disabled, CE1 = CE2 = 0
CE_FRC	Read/Write	3	0	CE Outputs Force Enable 0 = CE outputs follow the charger-detection finite state machine (FSM) 1 = CE outputs follow the CE[2:0] register regardless of the result from the charger-detection FSM
CE	Read/Write	[2:0]	000	CE Outputs (CE2, CE1, CE0). If CE_FRC = 0, registers are set by the result of charger FSM. If CE_FRC = 1, registers are set by I^2C command only.
CONTROL 3 (I^2C ADDRESS = 0x04)				
RFU	Read/Write	[7:5]	000	Reserved
CDP_DET	Read/Write	4	0	0 = Normal detection 1 = Resistive detection
USB_CPL	Read/Write	3	1 (0)*	USB Compliance 0 = Device is not USB compliant 1 = Device is USB compliant
SFOUT_EN	Read/Write	2	0 (1)*	LOUT Enable 0 = LOUT off 1 = LOUT on as per SFOUTASRT
SFOUTASRT	Read/Write	1	1	LOUT Assert Timing 0 = LOUT asserts when the charger-detection FSM completes 1 = LOUT asserts after valid V_{BUS} voltage detection
DCD_EXIT	Read/Write	0	1	Exit Charger-Type-Detection Routine After DCD_T is Set to 1 0 = Disabled 1 = Enabled

Note: *CP_ENA, DCHK, USB_CHGDET, DCD_EN, SUS_LOW, CE_FRC, CE, USB_CPL, SFOUT_EN, SFOUTASRT, and DCD_EXIT can be configured to have different default values. Contact the factory for more information.*

**Default value for MAX14578AE only.*

Detailed Description

The MAX14578E/MAX14578AE are USB charger detectors compliant with USB Battery Charging Revision 1.1. The USB charger-detection circuitry detects USB standard downstream ports (SDPs), USB charging downstream ports (CDPs), or dedicated charger ports (DCPs), and controls an external lithium-ion (Li+) battery charger.

The MAX14578E features I²C communication, while the MAX14578AE features an $\overline{EN}$ pin and an LDO output pin.

The internal USB switch is compliant to Hi-Speed USB, full-speed USB, and low-speed USB signals. Both devices feature low on-resistance, low on-resistance flatness, and very low capacitance.

Input Sources and Routing

The typical Micro/Mini-USB connector has five signal lines: USB power, two USB signal lines (D-, D+), ID line, and ground. The USB power on the Micro/Mini-USB connector connects to V_B on the MAX14578E/MAX14578AE. The two USB signal lines, D- and D+, connect to CD- and CD+.

USB (CD-, CD+)

The MAX14578E/MAX14578AE support Hi-Speed (480Mbps), full-speed (12Mbps), and low-speed USB (1.5Mbps) signal levels. The USB channel is bidirectional and has low 3.3Ω (typ) on-resistance and 4.5pF (typ) on-capacitance. The low on-resistance is stable as the analog input signals are swept from ground to V_{SWPOS} for low signal distortion.

LOUT LDO Output (MAX14578AE Only)

The LOUT LDO provides a 5.3V (typ) output, used to power a USB transceiver. Most USB transceivers are powered from a 3.3V or higher voltage that is difficult to derive from a Li+ battery. One solution is to power the transceivers from the USB V_{BUS} power; however, V_{BUS} can rise as high as +28V in a fault condition. The LOUT pin provides a voltage-limited supply that protects the USB transceiver from these high voltages. When V_{BUS} rises above 9.0V (typ), the MAX14578AE detects an overvoltage fault and LOUT goes to 0V. Additionally, LOUT features a 100mA (typ) current limit to protect the device in the event of a short circuit.

Interrupts

The MAX14578E generates an interrupt for any change in VBCOMP, and when DBCHG or DCD_T transitions from 0 to 1. The INTEN bit in the CONTROL 1 register (0x01) enables interrupt output. When INTEN is set to zero, all interrupts are masked but not cleared. A read to the INTERRUPT register (0x02) is required to clear interrupts.

Detection Debounce

To avoid multiple interrupts at the insertion of an accessory and for added noise/disturbance protection, a 30ms (typ) debounce timer is present that requires an inserted or removed state hold for the debounce time before it sends an interrupt.

Low-Power Modes

The MAX14578E has two I²C bits in the CONTROL 1 register (0x01) dedicated to low-power operation: LOW_POW and CP_ENA.

LOW_POW sets low-power mode. In low-power mode, the internal oscillator is turned off under the following conditions: no V_{BUS}, USBSWC = 0, and CP_ENA = 0. When enabled, all switches are high impedance (note that no negative rail voltage can be applied).

CP_ENA controls the charge pump required for proper operation of the analog switches. When set to disable, no negative rail voltage can be applied. A factory default sets CP_ENA = 0 automatically.

USB Charger Detection

The MAX14578E includes internal logic to detect if a valid USB charger is connected. When a valid V_{BUS} voltage is applied to V_B or when CHG_TYP_M in the CONTROL 1 register is set to 1, the MAX14578E/MAX14578AE begin the charger-type-detection sequence (see Figure 1). During the charger-type-detection sequence, the CD- and CD+ switches are open, and once the sequence completes, the switches return to their previous state. Figure 2 shows a timing diagram for an example charger-type-detection sequence.

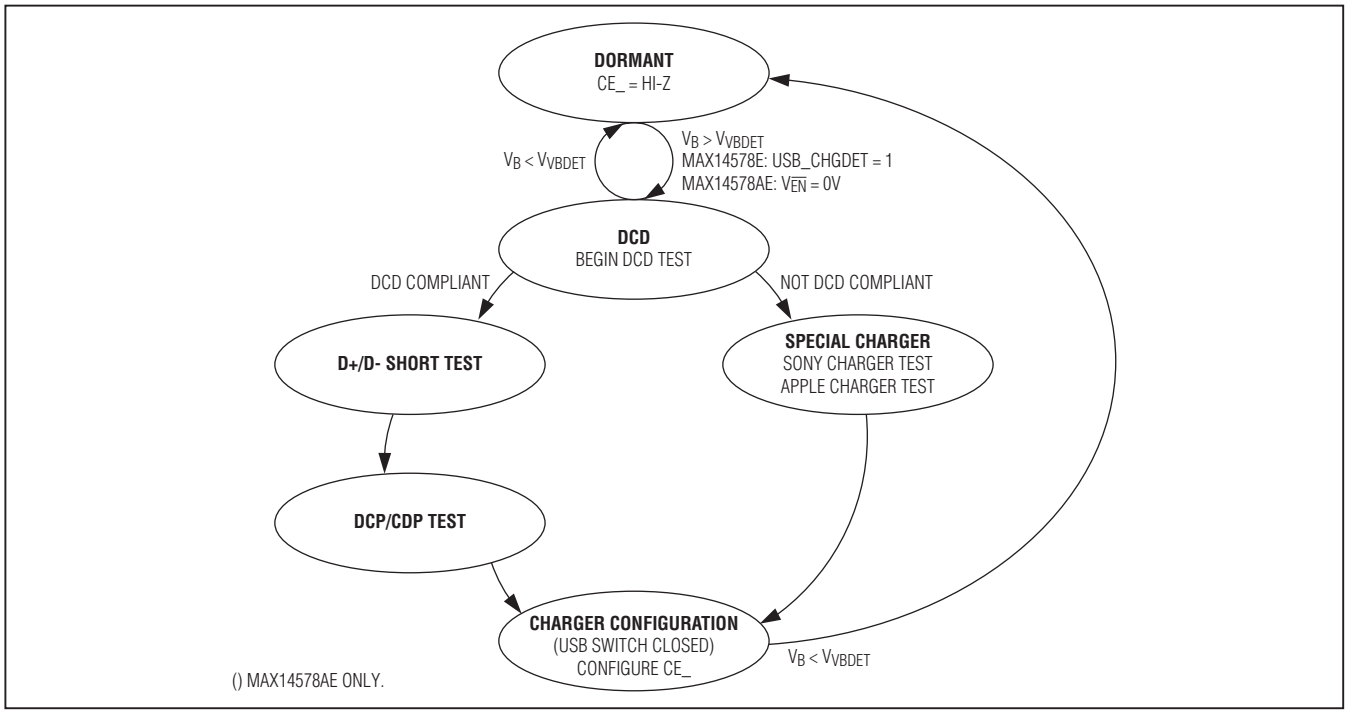


Figure 1. Charger-Type-Detection Sequence

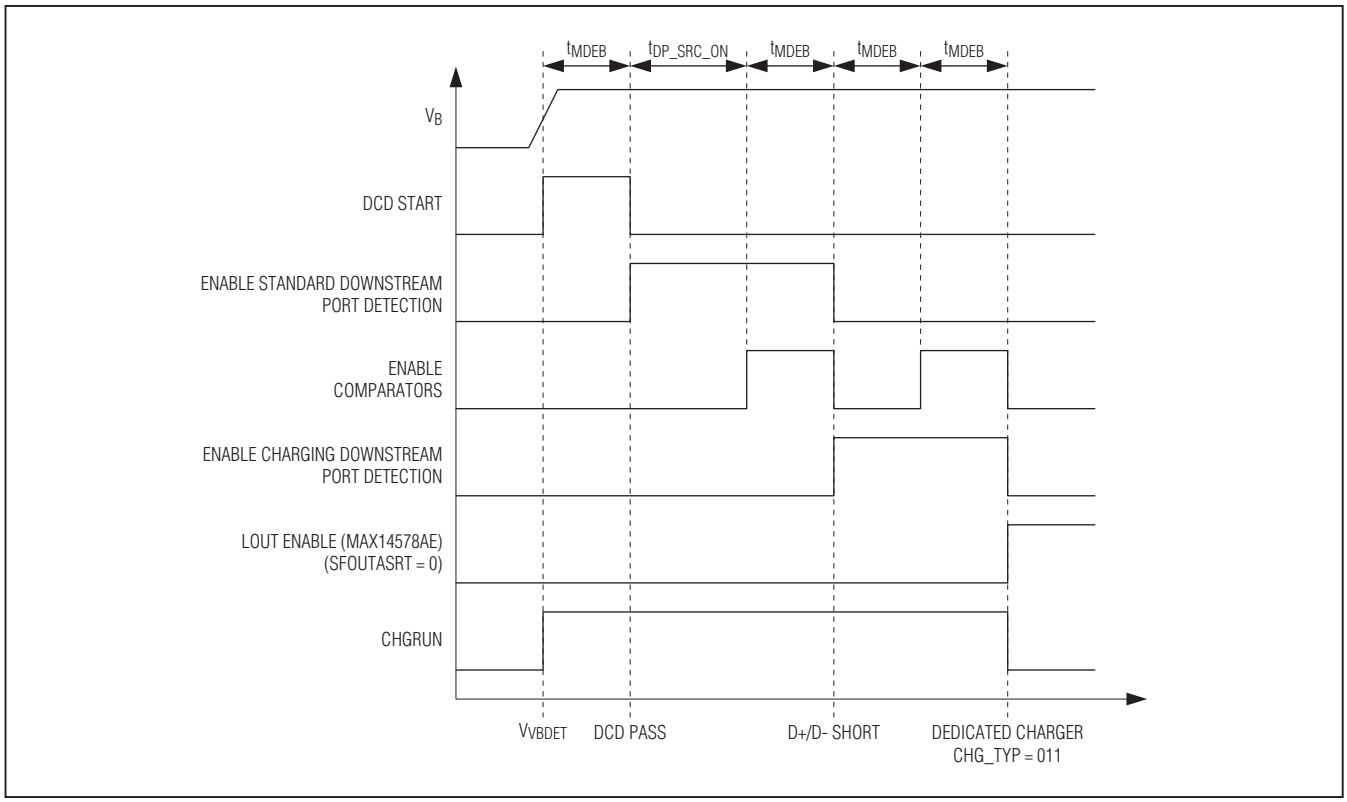


Figure 2. Charger-Detection Timing

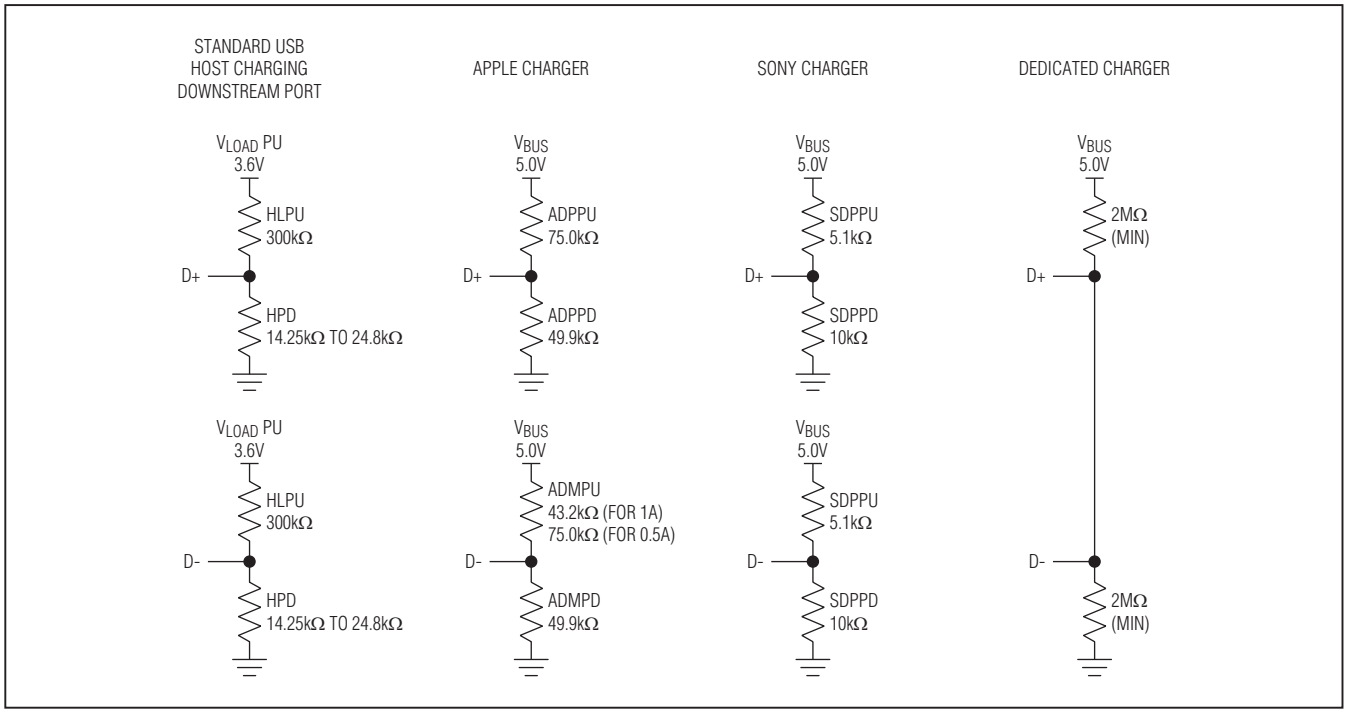


Figure 3. Standard USB Host/Charging Downstream Port, Apple Charger, Sony Charger, and Dedicated Charger

Figure 3 shows D+/D- terminations for a standard USB host/charging downstream port, an Apple charger, a Sony charger, and a dedicated charger.

Charger-Enable Control Outputs

The MAX14578E/MAX14578AE feature digital open-drain outputs—CE0 (MAX14578AE only), CE1, and CE2—to control an external charger autonomously. See Table 3.

Table 3. Charger-Enable Control Outputs

SUS_LOW	$\overline{EN}$	CHG_TYP	USB_CPL	CE2	CE1	CE0
0	1	X	X	1	1	1
1	1	X	X	0	0	1
0	0	000	X	1	1	1
1	0	000	X	0	0	1
0	0	110	X	1	1	1
1	0	110	X	0	0	1
X	0	001	0	1	0	0
0	0	001	1	1	1	1
1	0	001	1	0	0	1
X	0	010	X	0	1	0
X	0	011	X	0	1	0
X	0	100	X	1	0	0
X	0	101	X	0	1	0
X	0	111	X	0	0	0

Note: *When CE_FRC = 1, CE[2:0] are set by an I²C command.*

X = Don't care.

I²C Serial Interface (MAX14578E)

Serial Addressing

The MAX14578E operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX14578E and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition (Figure 4) sent by a master, followed by the MAX14578E 7-bit slave address plus a R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (see Figure 5). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

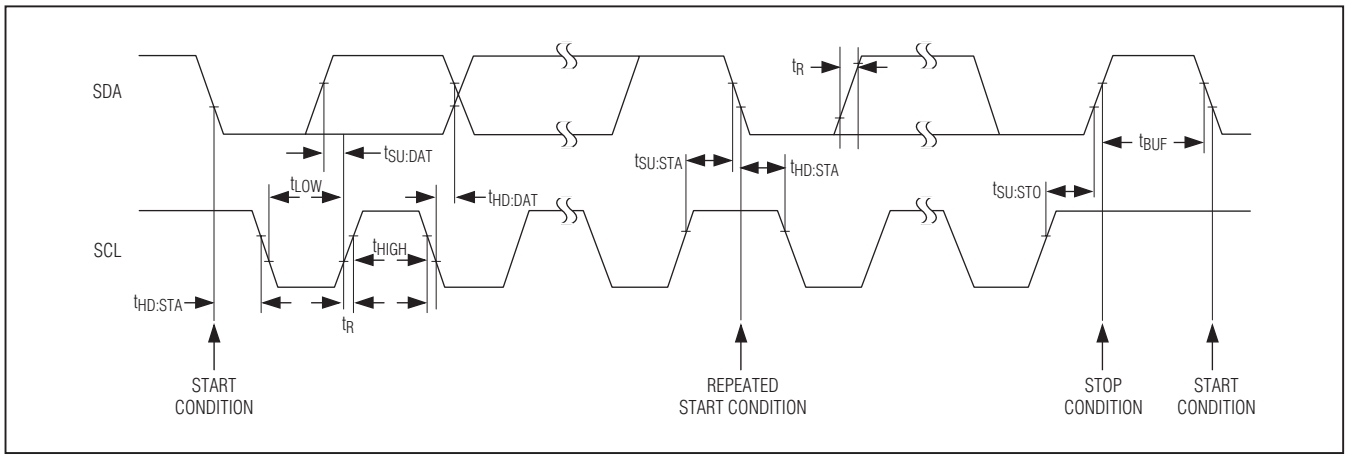


Figure 4. I²C Interface Timing Details

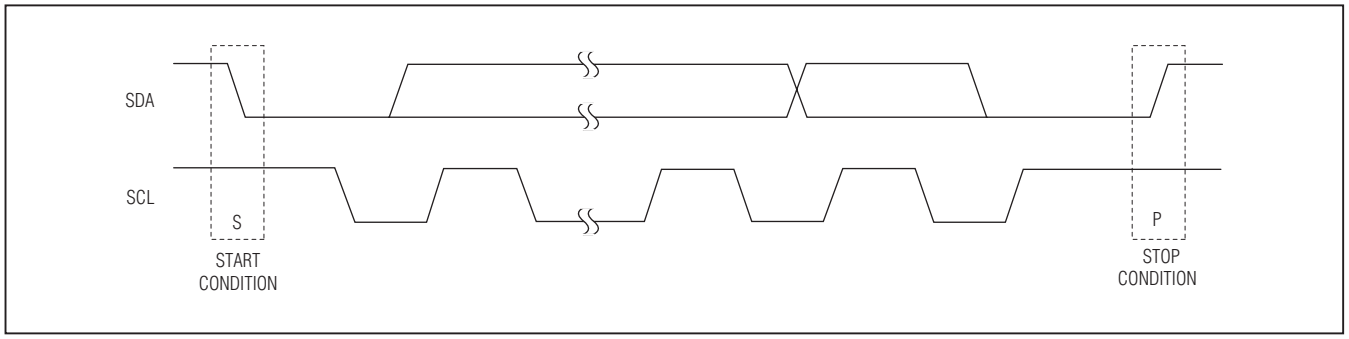


Figure 5. START and STOP Conditions

Bit Transfer

One data bit is transferred during each clock pulse (Figure 6). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 7). Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14578E, it generates the acknowledge bit because the MAX14578E is the recipient. When the MAX14578E is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX14578E has a 7-bit long slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address is 01011001 for read commands and 01011000 for write commands. See Figure 8.

Bus Reset

The MAX14578E resets the bus with the I²C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the MAX14578E transmits data to the master, thus the master is reading from the device.

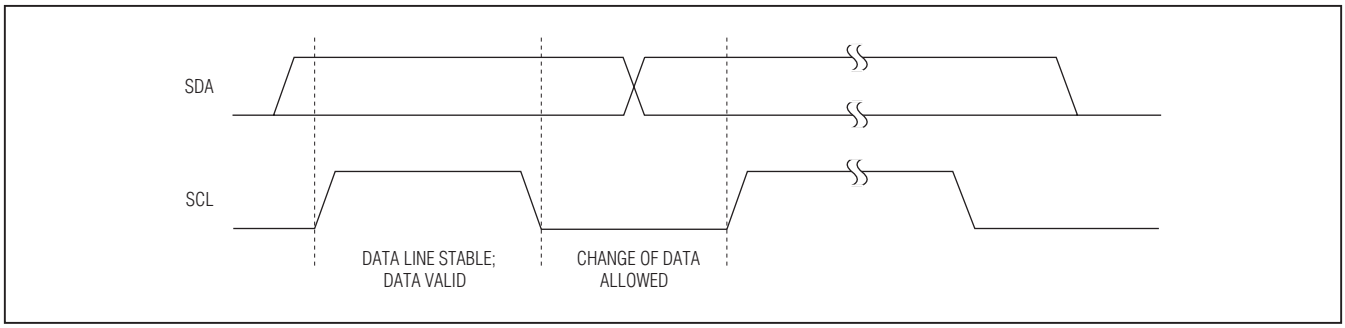


Figure 6. Bit Transfer

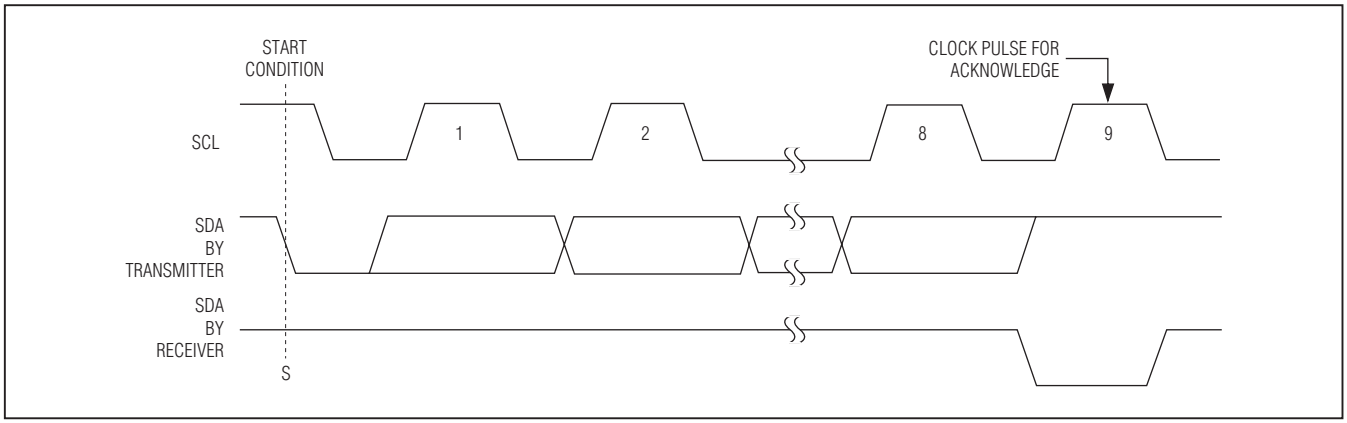


Figure 7. Acknowledge

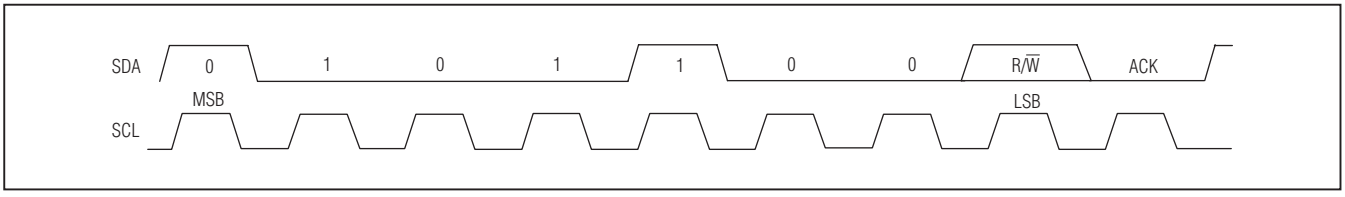


Figure 8. Slave Address

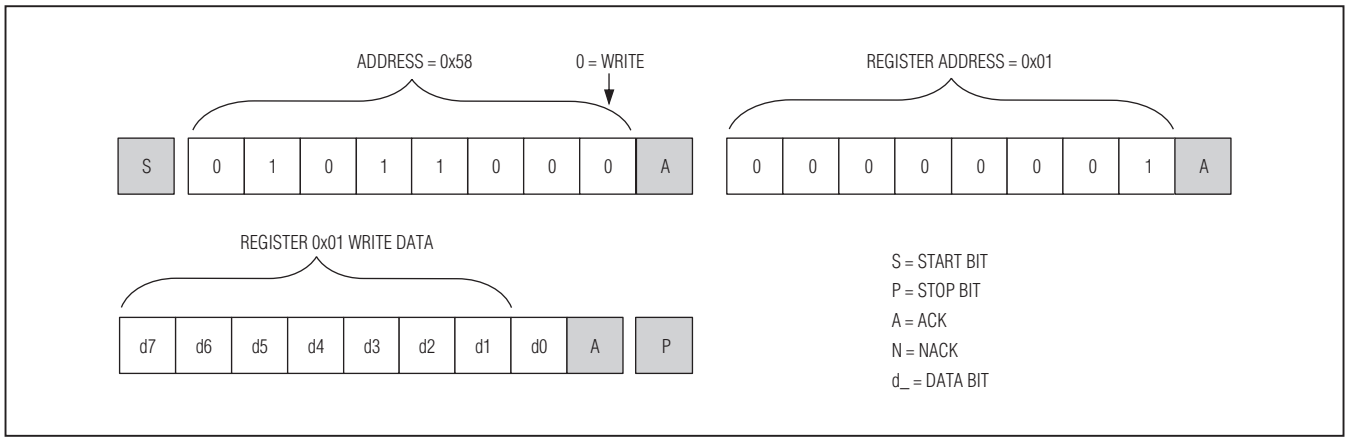


Figure 9. Format for I²C Write

Figure 10. Format for Writing to Multiple Registers

Format for Writing

A write to the MAX14578E comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the register address or command byte. The register address determines which register of the MAX14578E is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the MAX14578E takes no further action beyond storing the register address (Figure 9). Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, and subsequent data bytes go into subsequent registers (Figure 10). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrements.

Format for Reading

The MAX14578E is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 11). The master can now read consecutive bytes from the MAX14578E, with the first data byte being read from the register address pointed by the previously written register address. Once the master sends a NACK, the MAX14578E stops sending valid data.

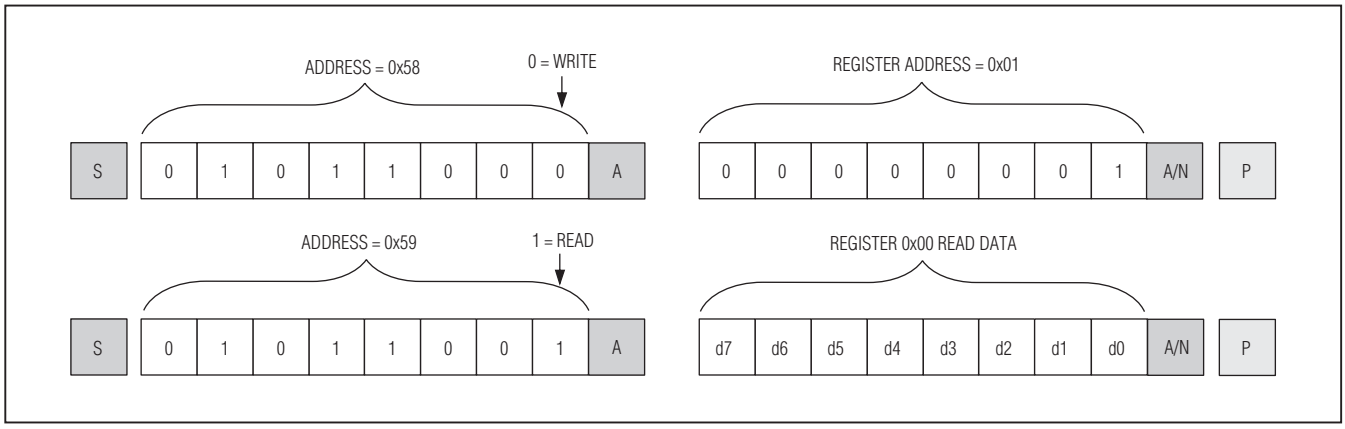


Figure 11. Format for Reads (Repeated START)

Table 4. CE_ Outputs for Different Charger Control

	CE_ OUTPUTS	OFF	100mA	500mA	ISET	MAX8606, MAX8856	MAX8814, MAX8845
SUS_LOW = 0	(CE0)	1	0	0	0	—	$\overline{EN}$
	CE1	1	0	0	1	$\overline{EN1}$	—
	CE2	1	0	1	0	$\overline{EN2}$	—
	CE_ OUTPUTS	**OFF**	**100mA**	**500mA**	**ISET**	**MAX8934, MAX8677**	**MAX8903**
SUS_LOW = 1	(CE0)	1	0	0	0	USUS	USUS
	CE1	0	0	0	1	PEN1	DCM
	CE2	0	0	1	0	PEN2	IUSB

() MAX14578AE only.

Applications Information

Charger Control

The MAX14578E charger-enable control outputs are ideal for autonomous external charger control. Table 4 shows example connections for various Maxim chargers.

Hi-Speed USB

Hi-Speed USB requires careful PCB layout with 45Ω single-ended/90Ω differential controlled-impedance matched traces of equal lengths.

Power-Supply Bypassing

Bypass V_B and BAT with 1µF ceramic capacitors to GND as close as possible to the device.

Choosing I²C Pullup Resistors

I²C requires pullup resistors to provide a logic-high level to data and clock lines. There are trade-offs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast-mode, which is defined for a clock frequency up to 400kHz (see the *I²C Serial Interface (MAX14578E)* section for details).

To meet the rise time requirement, choose pullup resistors so that $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. If the transition time becomes too slow, the setup and hold times may not be met and waveforms may not be recognized.

Extended ESD Protection

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. The CD- and CD+ pins are further protected against ESD up to ±15kV (Human Body Model) and ±8kV IEC 61000-4-2 Contact Discharge without damage.

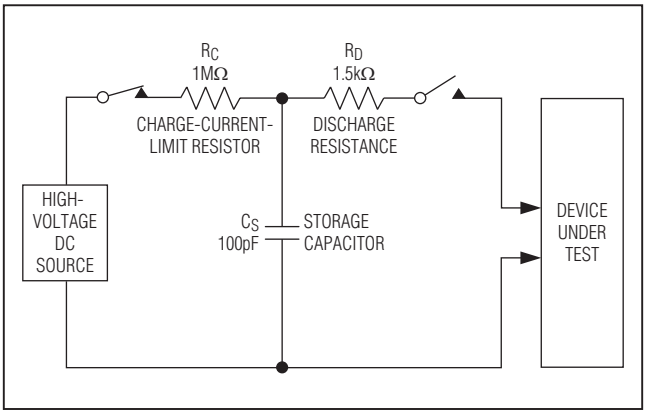


Figure 12. Human Body ESD Test Model

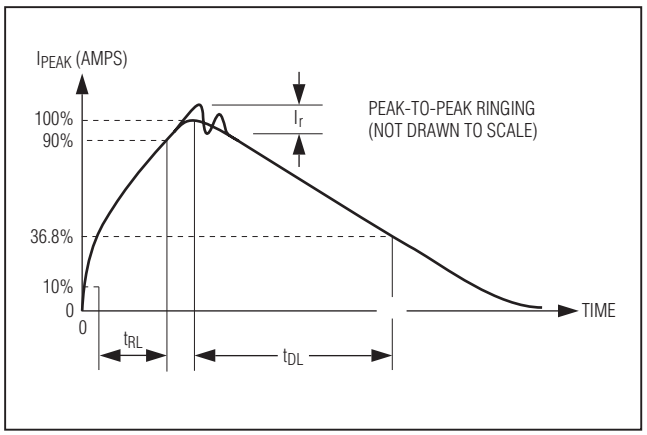


Figure 13. Human Body Current Waveform

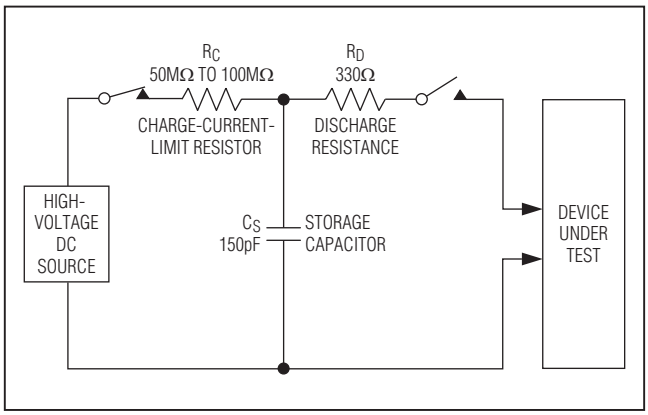


Figure 14. IEC 61000-4-2 ESD Test Model

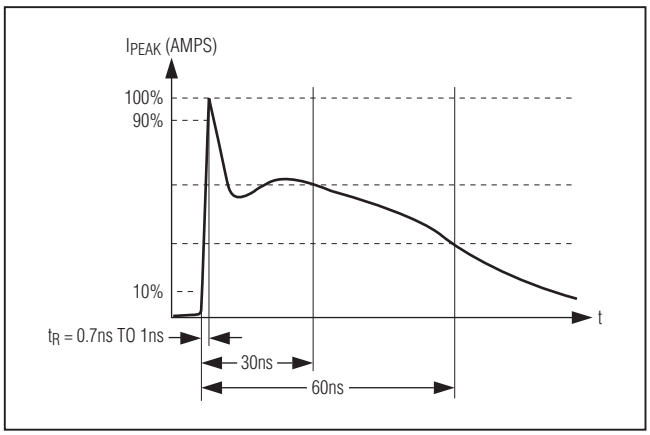


Figure 15. IEC 61000-4-2 ESD Generator Current Waveform

The V_B input withstands up to ±15kV (HBM) if bypassed with a 1µF ceramic capacitor close to the pin. The ESD structures withstand high ESD both in normal operation and when the devices are powered down. After an ESD event, the MAX14578E/MAX14578AE continue to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 12 shows the Human Body Model, and Figure 13 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14578E/MAX14578AE assist in designing equipment to meet IEC 61000-4-2 without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2, because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 14 shows the IEC 61000-4-2 model, and Figure 15 shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 WLP	W121A1+1	21-0449	Refer to Application Note 1891
16 TQFN	T1633+5	21-0136	90-0032

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/11	Initial release	—
1	2/12	Added TQFN package, corrected *MAX14578E Functional Diagram/Typical Operating Circuit*, and corrected default values for MAX14578AE in Table 2	1, 2, 8, 9, 13, 22
2	9/12	Updated *Package Thermal Characteristics* section and VB supply current parameter for the MAX14578A	2, 3