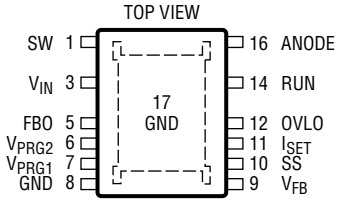
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Supply Voltage ..... –0.3V to 140V
RUN Voltage ..... –0.3V to 140V
SS, FBO, OVLO, I_{SET} Voltages ..... –0.3V to 6V
V_{FB}, V_{PRG1}, V_{PRG2} Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3, 4)
LTC7138E, LTC7138I ..... –40°C to 125°C
LTC7138H ..... –40°C to 150°C
LTC7138MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
VARIATION: MSE16 (12)
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7138EMSE#PBF	LTC7138EMSE#TRPBF	7138	16-Lead Plastic MSOP	–40°C to 125°C
LTC7138IMSE#PBF	LTC7138IMSE#TRPBF	7138	16-Lead Plastic MSOP	–40°C to 125°C
LTC7138HMSE#PBF	LTC7138HMSE#TRPBF	7138	16-Lead Plastic MSOP	–40°C to 150°C
LTC7138MPMSE#PBF	LTC7138MPMSE#TRPBF	7138	16-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (V_{IN})							
V_{IN}	Input Voltage Operating Range			4		140	V
V_{OUT}	Output Voltage Operating Range			0.8		V_{IN}	V
UVLO	V_{IN} Undervoltage Lockout	V_{IN} Rising V_{IN} Falling Hysteresis	● ●	3.5 3.3	3.75 3.5 250	4.0 3.8	V V mV
I_Q	DC Supply Current (Note 5) Active Mode Sleep Mode Shutdown Mode	 No Load V_{RUN} = 0V			 200 12 1.4	 400 22 6	 µA µA µA
V_{RUN}	RUN Pin Threshold	RUN Rising RUN Falling Hysteresis		1.17 1.06	1.21 1.10 110	1.25 1.14	V V mV
I_{RUN}	RUN Pin Leakage Current	RUN = 1.3V		–10	0	10	nA
V_{OVLO}	OVLO Pin Threshold	OVLO Rising OVLO Falling Hysteresis		1.17 1.06	1.21 1.10 110	1.25 1.14	V V mV

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Supply (V_{FB})							
$V_{FB(ADJ)}$	Feedback Comparator Threshold (Adjustable Output)	V_{FB} Rising, V_{PRG1} = V_{PRG2} = 0V					
		LTC7138E, LTC7138I	●	0.792	0.800	0.808	V
		LTC7138H, LTC7138MP	●	0.788	0.800	0.812	V
V_{FBH}	Feedback Comparator Hysteresis (Adjustable Output)	V_{FB} Falling, V_{PRG1} = V_{PRG2} = 0V	●	3	5	9	mV
I_{FB}	Feedback Pin Current	V_{FB} = 1V, V_{PRG1} = V_{PRG2} = 0V		–10	0	10	nA
$V_{FB(FIXED)}$	Feedback Comparator Thresholds (Fixed Output)	V_{FB} Rising, V_{PRG1} = SS, V_{PRG2} = 0V	●	4.94	5.015	5.09	V
		V_{FB} Falling, V_{PRG1} = SS, V_{PRG2} = 0V	●	4.91	4.985	5.06	V
		V_{FB} Rising, V_{PRG1} = 0V, V_{PRG2} = SS	●	3.25	3.31	3.37	V
		V_{FB} Falling, V_{PRG1} = 0V, V_{PRG2} = SS	●	3.23	3.29	3.35	V
		V_{FB} Rising, V_{PRG1} = V_{PRG2} = SS	●	1.78	1.81	1.84	V
		V_{FB} Falling, V_{PRG1} = V_{PRG2} = SS	●	1.77	1.80	1.83	V
Operation							
I_{PEAK}	Peak Current Comparator Threshold	I_{SET} Floating	●	540	610	680	mA
		100k Resistor from I_{SET} to GND	●	270	310	350	mA
		I_{SET} Shorted to GND	●	140	170	200	mA
I_{VAL}	Valley Current Comparator Threshold Relative to I_{PEAK}	I_{SET} Floating	●	50	60	70	%
		100k Resistor from I_{SET} to GND	●	45	60	70	%
		I_{SET} Shorted to GND	●	45	60	75	%
R_{ON}	Power Switch On-Resistance	I_{SW} = –100mA			1.8		Ω
I_{LSW}	Switch Pin Leakage Current	V_{IN} = 140V, SW = 0V			0.1	1	µA
I_{SS}	Soft-Start Pin Pull-Up Current	V_{SS} < 2.5V		4	5	6	µA
$t_{INT(SS)}$	Internal Soft-Start Time	SS Pin Floating			1		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7138 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7138E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7138I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC7138H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC7138MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range.

High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} is 40°C/W for the MSOP package.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device. The overtemperature protection level is not production tested.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

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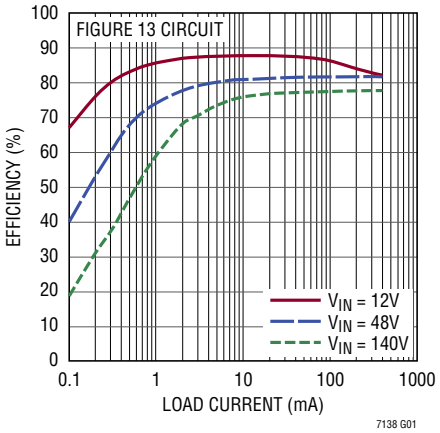
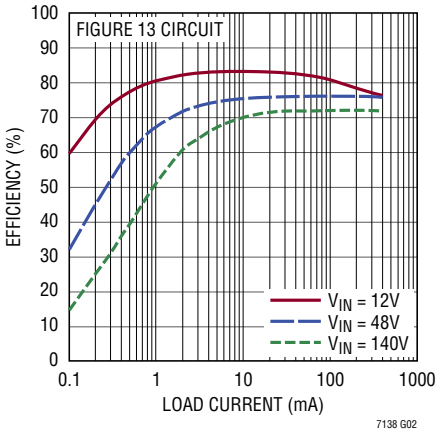
TYPICAL PERFORMANCE CHARACTERISTICS

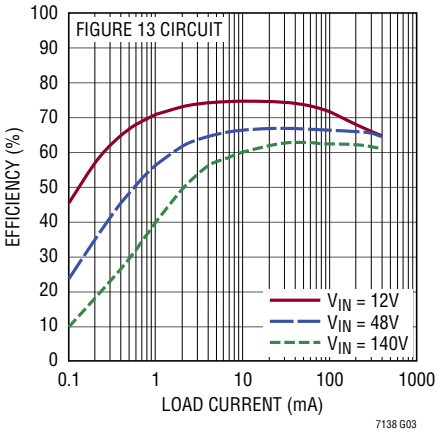
Efficiency vs Load Current, V_{OUT} = 5V



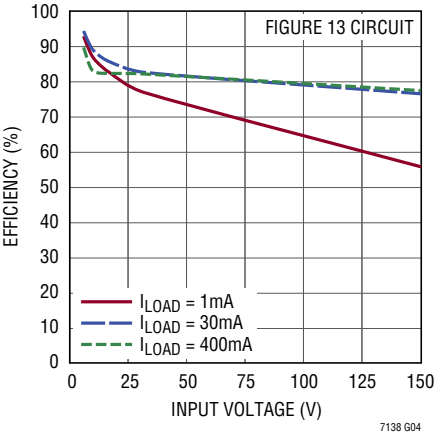
Efficiency vs Load Current, V_{OUT} = 3.3V



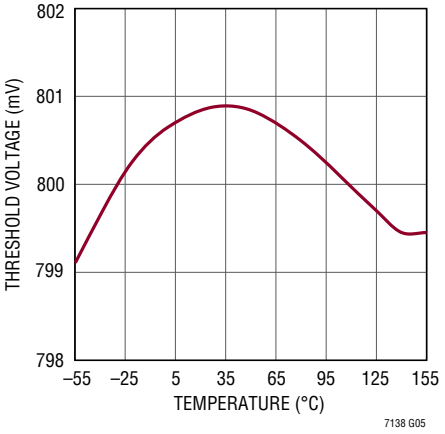
Efficiency vs Load Current, V_{OUT} = 1.8V



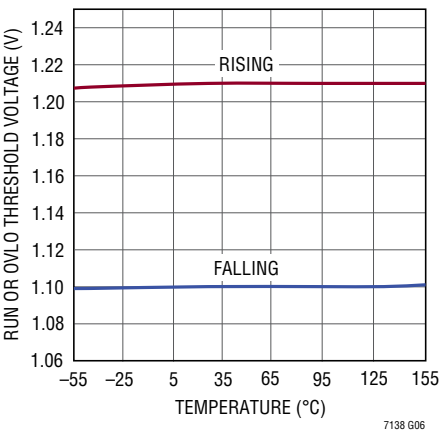
Efficiency vs Input Voltage, V_{OUT} = 5V



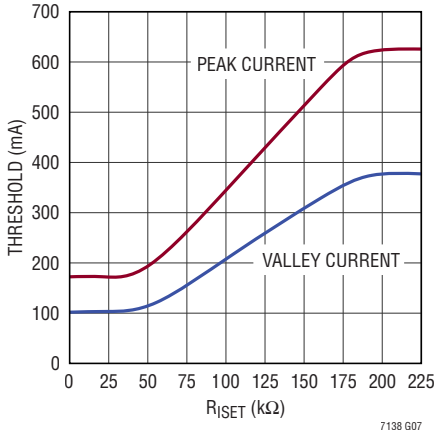
Feedback Comparator Trip Threshold vs Temperature



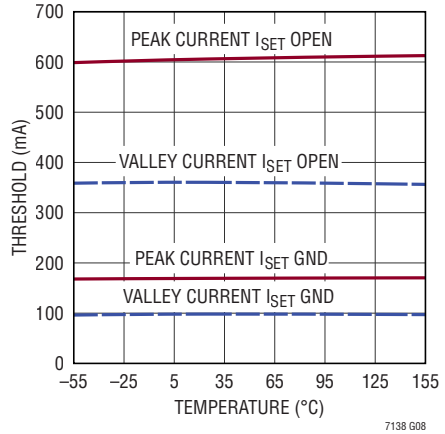
RUN and OVLO Thresholds vs Temperature



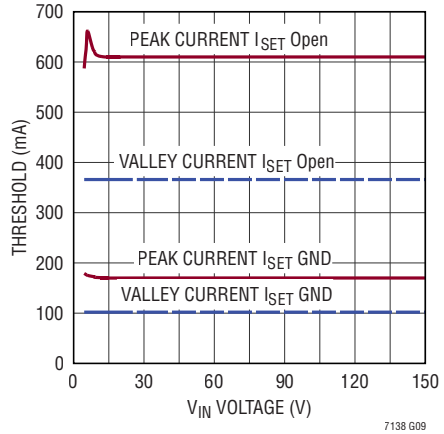
Peak Current and Valley Current Trip Thresholds vs R_{ISET}



Peak Current and Valley Current Trip Thresholds vs Temperature and I_{SET}



Peak Current and Valley Current Trip Thresholds vs Input Voltage



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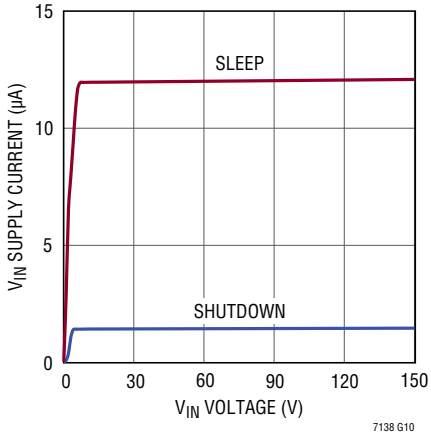
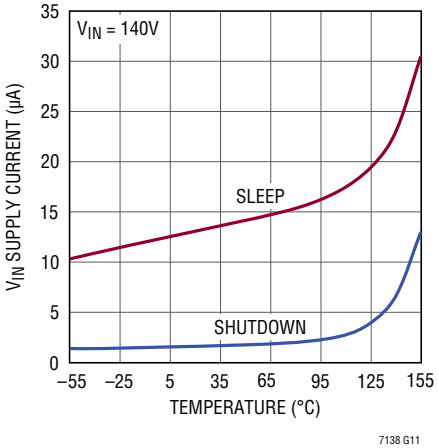
TYPICAL PERFORMANCE CHARACTERISTICS

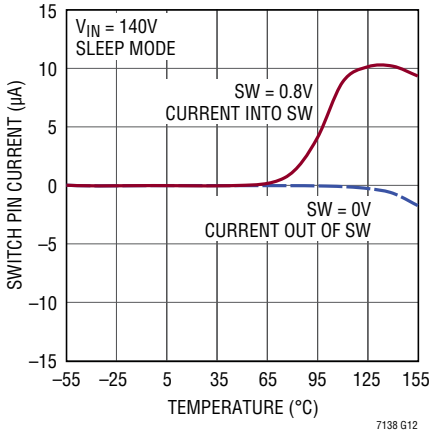
Quiescent Supply Current vs Input Voltage



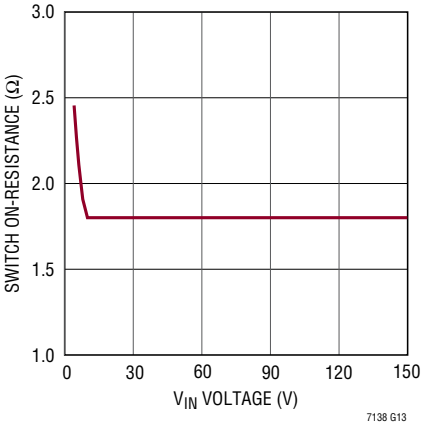
Quiescent Supply Current vs Temperature



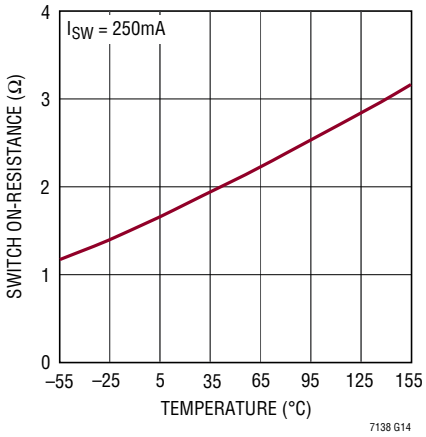
Switch Pin Current vs Temperature



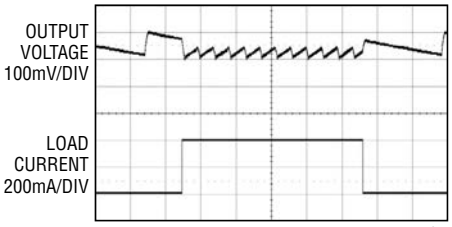
Switch On-Resistance vs Input Voltage



Switch On-Resistance vs Temperature

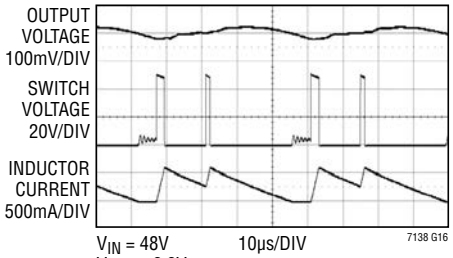


Load Step Transient Response



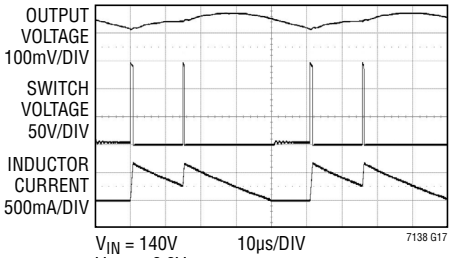
V_{IN} = 48V 200µs/DIV
V_{OUT} = 3.3V
10mA TO 400mA LOAD STEP
FIGURE 14 CIRCUIT

Operating Waveforms, V_{IN} = 48V



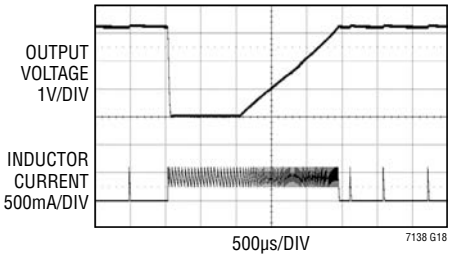
V_{IN} = 48V 10µs/DIV
V_{OUT} = 3.3V
I_{OUT} = 300mA
FIGURE 14 CIRCUIT

Operating Waveforms, V_{IN} = 140V



V_{IN} = 140V 10µs/DIV
V_{OUT} = 3.3V
I_{OUT} = 300mA
FIGURE 14 CIRCUIT

Short-Circuit and Recovery



500µs/DIV
FIGURE 14 CIRCUIT

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PIN FUNCTIONS

SW (Pin 1): Switch Node Connection to Inductor and Catch Diode Cathode. This pin connects to the drain of the internal power MOSFET switch.

V_{IN} (Pin 3): Main Supply Pin. A ceramic bypass capacitor should be tied between this pin and GND.

FBO (Pin 5): Feedback Comparator Output. Connect to the V_{FB} pins of additional LTC7138s to combine the output current. The typical pull-up current is 20µA. The typical pull-down impedance is 70Ω. See Applications Information.

V_{PRG2}, V_{PRG1} (Pins 6, 7): Output Voltage Selection. Short both pins to ground for a resistive divider programmable output voltage. Short V_{PRG1} to SS and short V_{PRG2} to ground for a 5V output voltage. Short V_{PRG1} to ground and short V_{PRG2} to SS for a 3.3V output voltage. Short both pins to SS for a 1.8V output voltage.

GND (Pin 8, Exposed Pad Pin 17): Ground. The exposed pad must be soldered to the PCB ground plane for rated electrical and thermal performance.

V_{FB} (Pin 9): Output Voltage Feedback. When configured for an adjustable output voltage, connect to an external resistive divider to divide the output voltage down for comparison to the 0.8V reference. For the fixed output configuration, directly connect this pin to the output.

SS (Pin 10): Soft-Start Control Input. A capacitor to ground at this pin sets the output voltage ramp time. A 50µA current initially charges the soft-start capacitor until switching begins, at which time the current is reduced to its nominal value of 5µA. The output voltage ramp time from zero to its regulated value is 1ms for every 6.25nF of capacitance from SS to GND. If left floating, the ramp time defaults to an internal 1ms soft-start.

I_{SET} (Pin 11): Peak Current Set Input. A resistor from this pin to ground sets the peak current comparator threshold. Leave floating for the maximum peak current (610mA typical) or short to ground for minimum peak current (170mA typical). The valley current is typically 60% of the peak current set by this pin. The maximum output current is 75% of the peak current. The 5µA current that is sourced out of this pin when switching is reduced to 1µA in sleep. Optionally, a capacitor can be placed from this pin to GND to trade off efficiency for light load output voltage ripple. See Applications Information.

OVLO (Pin 12): Overvoltage Lockout Input. Connect to the input supply through a resistor divider to set the overvoltage lockout level. A voltage on this pin above 1.21V disables the internal MOSFET switch. Normal operation resumes when the voltage on this pin decreases below 1.10V. Exceeding the OVLO lockout threshold triggers a soft-start reset, resulting in a graceful recovery from an input supply transient. This pin must be grounded if the OVLO is not used.

RUN (Pin 14): Run Control Input. A voltage on this pin above 1.21V enables normal operation. Forcing this pin below 0.7V shuts down the LTC7138, reducing quiescent current to approximately 1.4µA. Optionally, connect to the input supply through a resistor divider to set the undervoltage lockout.

ANODE (Pin 16): Catch Diode Anode Sense. This pin is the anode connection for the catch diode. An internal sense resistor is connected between this pin and the exposed pad ground.

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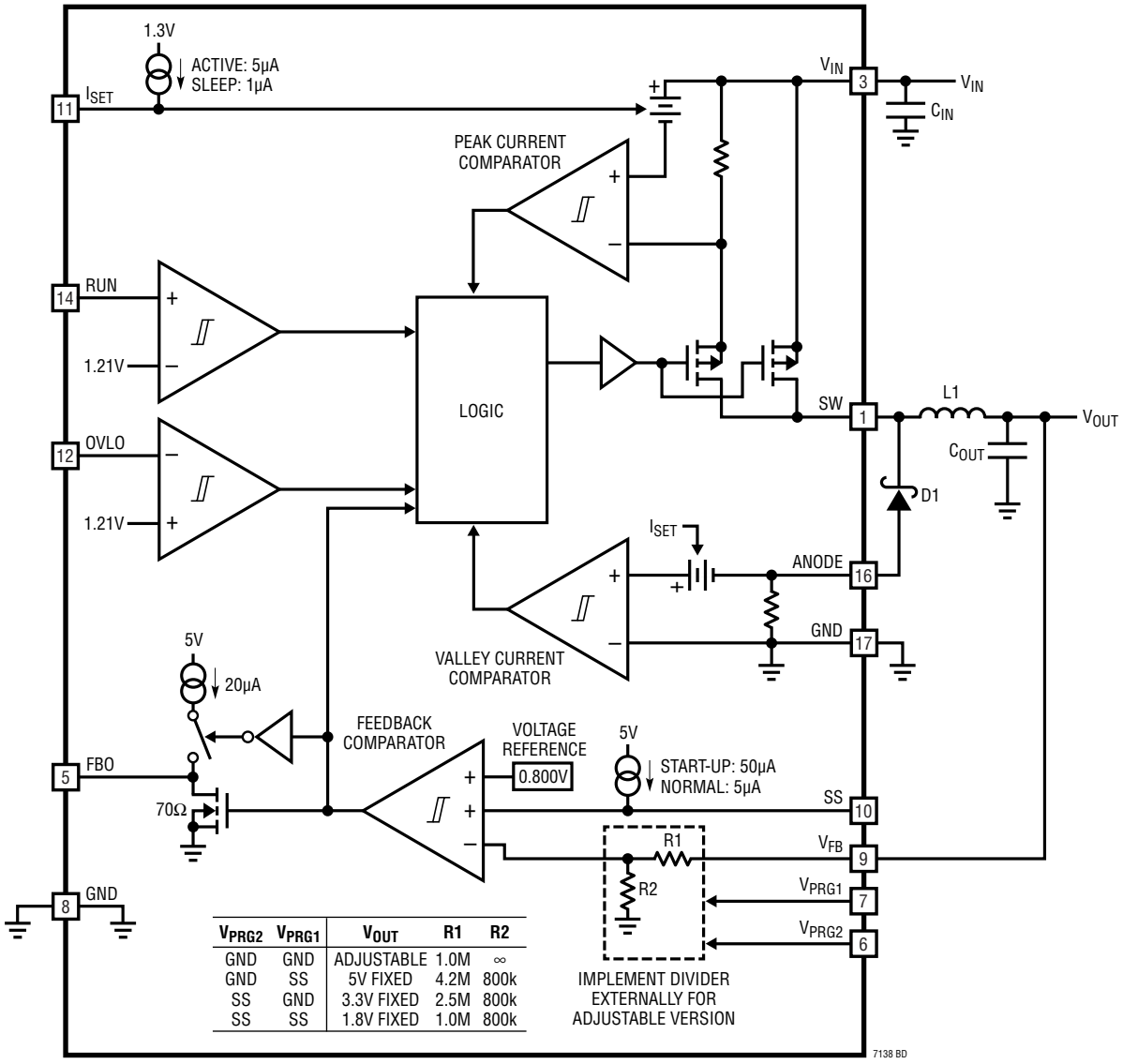
BLOCK DIAGRAM



V_{PRG2}	V_{PRG1}	V_{OUT}	R1	R2
GND	GND	ADJUSTABLE	1.0M	∞
GND	SS	5V FIXED	4.2M	800k
SS	GND	3.3V FIXED	2.5M	800k
SS	SS	1.8V FIXED	1.0M	800k

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OPERATION (Refer to Block Diagram)

The LTC7138 is a step-down DC/DC regulator with internal power switch that uses Burst Mode control, combining low quiescent current with high switching frequency, which results in high efficiency across a wide range of load currents. Burst Mode operation functions by using short "burst" cycles to switch the inductor current through the internal power MOSFET, followed by a sleep cycle where the power switch is off and the load current is supplied by the output capacitor. During the sleep cycle, the LTC7138 draws only 12µA of supply current. At light loads, the burst cycles are a small percentage of the total cycle time which minimizes the average supply current, greatly improving efficiency. Figure 1 shows an example of Burst Mode operation. The switching frequency is dependent on the inductor value, peak current, input voltage and output voltage.

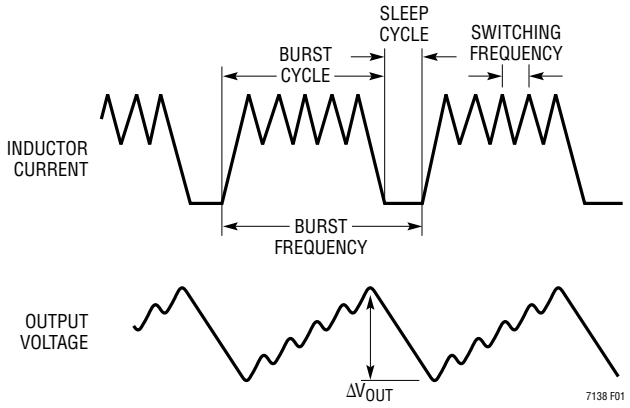

Figure 1. Burst Mode Operation

Main Control Loop

The LTC7138 uses the V_{PRG1} and V_{PRG2} control pins to connect internal feedback resistors to the V_{FB} pin. This enables fixed outputs of 1.8V, 3.3V or 5V without increasing component count, input supply current or exposure to noise on the sensitive input to the feedback comparator. External feedback resistors (adjustable mode) can be used by connecting both V_{PRG1} and V_{PRG2} to ground.

In adjustable mode the feedback comparator monitors the voltage on the V_{FB} pin and compares it to an internal 800mV reference. If this voltage is greater than the reference, the comparator activates a sleep mode in which the power switch and current comparators are disabled, reducing the V_{IN} pin supply current to only 12µA. As the load current discharges the output capacitor, the voltage on the V_{FB} pin decreases. When this voltage falls 5mV below the 800mV reference, the feedback comparator trips and enables burst cycles.

At the beginning of the burst cycle, the internal high side power switch (P-channel MOSFET) is turned on and the inductor current begins to ramp up. The inductor current increases until either the current exceeds the peak current comparator threshold or the voltage on the V_{FB} pin exceeds 800mV, at which time the switch is turned off and the inductor current is carried by the external catch diode. The inductor current, then sensed through the ANODE pin, ramps down until the current falls below the valley current comparator threshold. If the voltage on the V_{FB} pin is still less than the 800mV reference, the power switch is turned on again and another cycle commences. The average current during a burst cycle will normally be greater than the average load current. For this architecture, the maximum average output current is equal to 75% of the peak current.

The hysteretic nature of this control architecture results in a switching frequency that is a function of the input voltage, output voltage, and inductor value. This behavior provides inherent short-circuit protection. If the output is shorted to ground, the inductor current will decay very slowly during a single switching cycle. Since the high side switch turns on only when the inductor current is below the valley current trip threshold, the LTC7138 inherently switches at a lower frequency during start-up or short-circuit conditions.

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OPERATION (Refer to Block Diagram)

Start-Up and Shutdown

If the voltage on the RUN pin is less than 0.7V, the LTC7138 enters a shutdown mode in which all internal circuitry is disabled, reducing the DC supply current to 1.4µA. When the voltage on the RUN pin exceeds 1.21V, normal operation of the main control loop is enabled. The RUN pin comparator has 110mV of internal hysteresis, and therefore must fall below 1.1V to disable the main control loop.

An internal 1ms soft-start function limits the ramp rate of the output voltage on start-up to prevent excessive input supply droop. If a longer ramp time and consequently less supply droop is desired, a capacitor can be placed from the SS pin to ground. The 5µA current that is sourced out of this pin will create a smooth voltage ramp on the capacitor. If this ramp rate is slower than the internal 1ms soft-start, then the output voltage will be limited by the ramp rate on the SS pin. The internal and external soft-start functions are reset on start-up, after an undervoltage or overvoltage event on the input supply, and after an overtemperature shutdown.

Peak Inductor Current Programming

The peak current comparator nominally limits the peak inductor current to 610mA. This peak inductor current can be adjusted by placing a resistor from the I_{SET} pin to ground. The 5µA current sourced out of this pin through the resistor generates a voltage that adjusts the peak current comparator threshold. The valley current threshold tracks the peak current threshold setting, and is typically 60% of the peak current.

During sleep mode, the current sourced out of the I_{SET} pin is reduced to 1µA. The I_{SET} current is increased back to 5µA on the first switching cycle after exiting sleep mode. The I_{SET} current reduction in sleep mode, along with adding a filtering network, R_{ISET} and C_{ISET}, from the I_{SET} pin to ground, provides a method of reducing light load output voltage ripple at the expense of lower efficiency and slightly degraded load step transient response.

For applications requiring higher output current, the LTC7138 provides a feedback comparator output pin (FBO) for combining the output current of multiple LTC7138s. By connecting the FBO pin of a master LTC7138 to the V_{FB} pin of one or more slave LTC7138s, the output currents can be combined to source 400mA times the number of LTC7138s.

Dropout Operation

When the input supply decreases toward the output supply, the duty cycle increases to maintain regulation. The P-channel MOSFET switch in the LTC7138 allows the duty cycle to increase all the way to 100%. At 100% duty cycle, the P-channel MOSFET stays on continuously, providing output current equal to the peak current, which is greater than the maximum load current when not in dropout.

Input Voltage and Overtemperature Protection

When using the LTC7138, care must be taken not to exceed any of the ratings specified in the Absolute Maximum Ratings section. As an added safeguard, however, the LTC7138 incorporates an overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC7138 will enter thermal shutdown mode. The power switch will be turned off and the SW node will become high impedance. After the part has cooled below 160°C, it will restart. The overtemperature level is not production tested.

The LTC7138 additionally implements protection features which inhibit switching when the input voltage is not within a programmable operating range. By use of a resistive divider from the input supply to ground, the RUN and OVLO pins serve as a precise input supply voltage monitor. Switching is disabled when either the RUN pin falls below 1.1V or the OVLO pin rises above 1.21V, which can be configured to limit switching to a specific range of input supply voltage. Furthermore, if the input voltage falls below 3.5V typical (3.8V maximum), an internal undervoltage detector disables switching.

When switching is disabled, the LTC7138 can safely sustain input voltages up to the absolute maximum rating of 140V. Input supply undervoltage or overvoltage events trigger a soft-start reset, which results in a graceful recovery from an input supply transient.

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APPLICATIONS INFORMATION

The basic LTC7138 application circuit is shown on the front page of this data sheet. External component selection is determined by the maximum load current requirement and begins with the selection of the peak current programming resistor, R_{ISET}. The inductor value L can then be determined, followed by capacitors C_{IN} and C_{OUT}.

Maximum Output Current

The maximum average output current is determined by the peak current trip threshold and the valley current trip threshold. With the I_{SET} pin open, the peak current comparator has a minimum threshold of 540mA. The valley current comparator has a minimum threshold of 50% of the peak current, or 270mA. At maximum load, the inductor current ramps between the peak and valley current thresholds, which results in a maximum load current that is the average of the two, or 405mA. For applications that demand less current, the peak current threshold can be reduced to as low as 140mA, which provides 100mA average output current. This lower peak current allows the efficiency and component selection to be optimized for lower current applications. For applications that require more than 400mA, multiple LTC7138s can be connected in parallel using the FBO pin. See the Higher Current Applications section for more information.

The peak current threshold is linearly proportional to the voltage on the I_{SET} pin, with 280mV and 1V corresponding to 140mA and 540mA peak current, respectively. The valley current threshold correspondingly changes with the voltage on the I_{SET} pin to remain at 50% of the programmed peak current. This pin may be driven by an external voltage source to modulate the peak current, which may be beneficial in some applications. Usually, the peak current is programmed with an appropriately chosen resistor (R_{ISET}) between the I_{SET} pin and ground. The voltage generated on the I_{SET} pin by R_{ISET} and the internal 5µA current source sets the peak current. The value of resistor to achieve a maximum average output current can be computed by using Figure 2 or the following equation:

$$R_{ISET} = I_{OUT(MAX)} \bullet \frac{1k\Omega}{2mA}$$

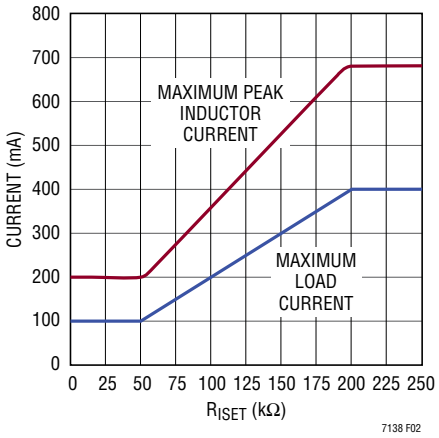

Figure 2. R_{ISET} Selection

where 100mA < $I_{OUT(MAX)}$ < 405mA. This equation gives the maximum load current supplied using the minimum peak and valley current. For inductor selection, the maximum peak current can then be approximated for a given R_{ISET} resistor value as:

$$I_{PEAK(MAX)} \approx R_{ISET} \bullet \frac{3.3mA}{1k\Omega} + 30mA$$

The peak current is internally limited to be within the range of 140mA to 540mA. Shorting the I_{SET} pin to ground programs the current limit to 140mA (100mA average output current), and leaving it floating sets the current limit to the maximum value of 540mA (405mA average output current). The internal 5µA current source is reduced to 1µA in sleep mode to maximize efficiency and to facilitate a trade-off between efficiency and light load output voltage ripple, as described in the Optimizing Output Voltage Ripple section.

Inductor Selection

For the LTC7138, which has relatively low output current and very high input voltage, switching losses typically dominate the power loss equation. For this architecture, higher inductor values lower the switching frequency which decreases switching loss at the expense of higher DC resistance and lower saturation current. Therefore choosing the largest inductor value that satisfies both

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board area and saturation current requirements yields the highest efficiency in most LTC7138 applications.

A good first choice for the inductor can be calculated based on the maximum operating input voltage and the I_{SET} pin resistor. If the I_{SET} pin is shorted to ground or left open, use 50k or 200k respectively for R_{ISET} in the following equation.

$$L = 220\mu H \bullet \frac{V_{IN(MAX)}}{150V} \bullet \frac{200k\Omega}{R_{ISET}}$$

An additional constraint on the inductor value is the LTC7138's 150ns minimum switch on-time. Therefore, in order to avoid excessive overshoot in the inductor current, the inductor value must be chosen so that it is larger than a minimum value which can be computed as follows:

$$L > \frac{V_{IN(MAX)} \bullet 150ns}{I_{PEAK} \bullet 0.3} \bullet 1.2$$

where $V_{IN(MAX)}$ is the maximum input supply voltage when switching is enabled, I_{PEAK} is the peak current, and the factor of 1.2 accounts for typical inductor tolerance and variation over temperature. With the I_{SET} pin open, this minimum inductor value is approximately equal to $V_{IN(MAX)} \bullet 1\mu H/V$.

Although the previous equation provides a minimum inductor value, higher efficiency is typically achieved with a larger inductor value, which produces a lower switching frequency. The recommended range of inductor values for small surface mount inductors as a function of peak current is shown in Figure 3. For applications where board area is not a limiting factor, inductors with larger cores can be used, which extends the recommended range of Figure 3 to larger values.

For applications that have large input supply transients, the OVLO pin can be used to disable switching above the maximum operating voltage $V_{IN(MAX)}$ so that the minimum inductor value is not artificially limited by a transient condition. Inductor values that violate the above equation will cause the peak current to overshoot and permanent damage to the part may occur.

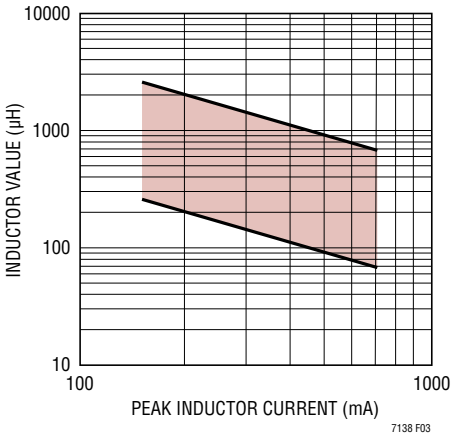

Figure 3. Recommended Inductor Values for Maximum Efficiency

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of the more expensive ferrite cores. Actual core loss is independent of core size for a fixed inductor value but is very dependent of the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy but generally cost more than powdered iron core inductors with similar charac-

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teristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, TDK, Toko, and Sumida.

Catch Diode Selection

The catch diode (D1 from Block Diagram) conducts current only during the switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output load current. The maximum average diode current occurs with a shorted output at the high line. For this worst-case condition, the diode current will approach 75% of the programmed peak current. The diode reverse voltage rating should be greater than the maximum operating input voltage. When the OVLO pin is used to limit the maximum operating input voltage, the diode reverse voltage should be greater than the OVLO pin setting, but may be lower than the maximum input voltage during overvoltage lockout.

For high efficiency at full load, it is important to select a catch diode with a low reverse recovery time and low forward voltage drop. As a result, Schottky diodes are often used as catch diodes. However, Schottky diodes generally exhibit much higher leakage than silicon diodes. In sleep, the catch diode leakage current will appear as load current, and may significantly reduce light load efficiency. Diodes with low leakage often have larger forward voltage drops at a given current, so a trade-off can exist between light load and full load efficiency.

The selection of Schottky diodes with high reverse voltage ratings is limited relative to that of silicon diodes. Therefore, for low reverse leakage and part availability, some applications may prefer a silicon diode. If a silicon diode is necessary, be sure to select a diode with a specified low reverse recovery time to maximize efficiency.

C_{IN} and C_{OUT} Selection

The input capacitor, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. C_{IN} should be sized to provide the energy required to magnetize the inductor without causing a large decrease in input voltage (ΔV_{IN}). The relationship between C_{IN} and ΔV_{IN} is given by:

$$C_{IN} > \frac{L \bullet I_{PEAK}^2}{2 \bullet V_{IN} \bullet \Delta V_{IN}}$$

It is recommended to use a larger value for C_{IN} than calculated by the previous equation since capacitance decreases with applied voltage. In general, a 1µF X7R ceramic capacitor is a good choice for C_{IN} in most LTC7138 applications.

To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based only on 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The output capacitor, C_{OUT}, filters the inductor's ripple current and stores energy to satisfy the load current when the LTC7138 is in sleep. The output ripple has a lower limit of $V_{OUT}/160$ due to the 5mV typical hysteresis of the feedback comparator. The time delay of the comparator adds an additional ripple voltage that is a function of the load current. During this delay time, the LTC7138 continues to switch and supply current to the output. The output ripple

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at light load can be approximated by:

$$\Delta V_{OUT} \approx \left(\frac{I_{PEAK}}{2} - I_{LOAD} \right) \bullet \frac{4 \bullet 10^{-6}}{C_{OUT}} + \frac{V_{OUT}}{160}$$

The output ripple is a maximum at no load and approaches lower limit of $V_{OUT}/160$ at full load. Choose the output capacitor C_{OUT} to limit the output voltage ripple ΔV_{OUT} using the following equation:

$$C_{OUT} \geq \frac{I_{PEAK} \bullet 2 \bullet 10^{-6}}{\Delta V_{OUT} - \frac{V_{OUT}}{160}}$$

The value of the output capacitor must also be large enough to accept the energy stored in the inductor without a large change in output voltage during a single switching cycle.

Setting this voltage step equal to 1% of the output voltage, the output capacitor must be:

$$C_{OUT} > \frac{L}{2} \bullet \left(\frac{I_{PEAK}}{V_{OUT}} \right)^2 \bullet \frac{100\%}{1\%}$$

Typically, a capacitor that satisfies the voltage ripple requirement is adequate to filter the inductor ripple. To avoid overheating, the output capacitor must also be sized to handle the ripple current generated by the inductor. The worst-case ripple current in the output capacitor is given by $I_{RMS} = I_{PEAK}/2$. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important only to use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have high voltage coefficient and audible piezoelectric effects. The high quality factor (Q) of ceramic capacitors in series with trace inductance can also lead to significant input voltage ringing.

Input Voltage Steps

If the input voltage falls below the regulated output voltage, the body diode of the internal MOSFET will conduct current from the output supply to the input supply. If the input voltage falls rapidly, the voltage across the inductor will be significant and may saturate the inductor. A large current will then flow through the MOSFET body diode, resulting in excessive power dissipation that may damage the part.

If rapid voltage steps are expected on the input supply, put a small silicon or Schottky diode in series with the V_{IN} pin to prevent reverse current and inductor saturation, shown below as D1 in Figure 4. The diode should be sized for a reverse voltage of greater than the regulated output voltage, and to withstand repetitive currents higher than the maximum peak current of the LTC7138.

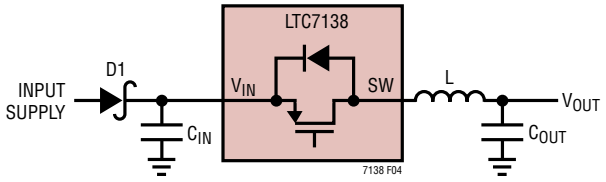

Figure 4. Preventing Current Flow to the Input

Ceramic Capacitors and Audible Noise

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and

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the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

For applications with inductive source impedance, such as a long wire, a series RC network may be required in parallel with C_{IN} to dampen the ringing of the input supply. Figure 5 shows this circuit and the typical values required to dampen the ringing. Refer to Application Note 88 for additional information on suppressing input supply transients.

Ceramic capacitors are also piezoelectric. The LTC7138's burst frequency depends on the load current, and in some applications the LTC7138 can excite the ceramic capacitor at audio frequencies, generating audible noise. This noise is typically very quiet to a casual ear; however, if the noise is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

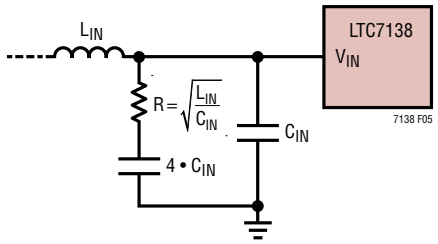

Figure 5. Series RC to Reduce V_{IN} Ringing

Output Voltage Programming

The LTC7138 has three fixed output voltage modes and an adjustable mode that can be selected with the V_{PRG1} and V_{PRG2} pins. The fixed output modes use an internal feedback divider which enables higher efficiency, higher noise immunity, and lower output voltage ripple for 5V, 3.3V, and 1.8V applications. To select the fixed 5V output voltage, connect V_{PRG1} to SS and V_{PRG2} to GND. For 3.3V, connect V_{PRG1} to GND and V_{PRG2} to SS. For 1.8V, connect both V_{PRG1} and V_{PRG2} to SS. For any of the fixed output voltage options, directly connect the V_{FB} pin to V_{OUT}.

For the adjustable output mode (V_{PRG1} = V_{PRG2} = GND), the output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 6. The output voltage can range from 0.8V to V_{IN}. Be careful to keep the divider resistors very close to the V_{FB} pin to minimize noise pick-up on the sensitive V_{FB} trace.

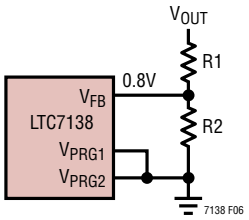

Figure 6. Setting the Output Voltage with External Resistors

To minimize the no-load supply current, resistor values in the megohm range may be used; however, large resistor values should be used with caution. The feedback divider is the only load current when in shutdown. If PCB leakage current to the output node or switch node exceeds the load current, the output voltage will be pulled up. In normal operation, this is generally a minor concern since the load current is much greater than the leakage.

To avoid excessively large values of R1 in high output voltage applications ($V_{OUT} \geq 10V$), a combination of external and internal resistors can be used to set the output voltage. This has an additional benefit of increasing the noise

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immunity on the V_{FB} pin. Figure 7 shows the LTC7138 with the V_{FB} pin configured for a 5V fixed output with an external divider to generate a higher output voltage. The internal 5M resistance appears in parallel with R2, and the value of R2 must be adjusted accordingly. R2 should be chosen to be less than 200k to keep the output voltage variation less than 1% due to the tolerance of the LTC7138's internal resistor.

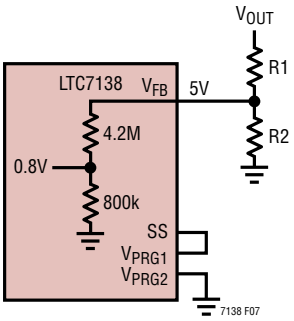

Figure 7. Setting the Output Voltage with External and Internal Resistors

RUN Pin and Overvoltage/Undervoltage Lockout

The LTC7138 has a low power shutdown mode controlled by the RUN pin. Pulling the RUN pin below 0.7V puts the LTC7138 into a low quiescent current shutdown mode (I_Q ~ 1.4µA). When the RUN pin is greater than 1.21V, switching is enabled. Figure 8 shows examples of configurations for driving the RUN pin from logic.

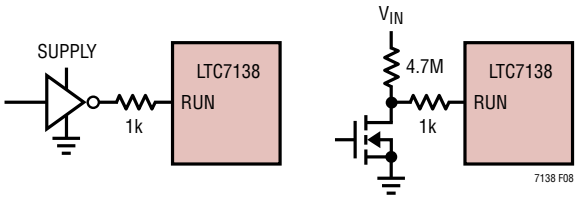

Figure 8. RUN Pin Interface to Logic

The RUN and OVLO pins can alternatively be configured as precise undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistive divider from V_{IN} to ground. A simple resistive divider can be used as shown in Figure 9 to meet specific V_{IN} voltage requirements.

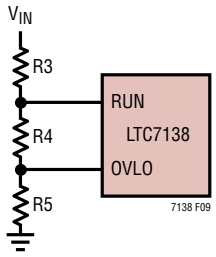

Figure 9. Adjustable UV and OV Lockout

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC7138, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megohm range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R4 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}. The individual values of R3, R4 and R5 can then be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ OVLO Threshold}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.21V}{\text{Rising } V_{IN} \text{ UVLO Threshold}} - R5$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not need a precise external OVLO, the OVLO pin should be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with R5 = 0Ω.

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Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal V_{IN} UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω.

Be aware that the OVLO pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the OVLO pin from exceeding 6V, the following relation should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R3+R4+R5} \right) < 6V$$

If this equation cannot be satisfied in the application, connect a 4.7V Zener diode between the OVLO pin and ground to clamp the OVLO pin voltage.

Soft-Start

Soft-start is implemented by ramping the effective reference voltage from 0V to 0.8V. To increase the duration of the soft-start, place a capacitor from the SS pin to ground. An internal 5µA pull-up current will charge this capacitor. The value of the soft-start capacitor can be calculated by the following equation:

$$C_{SS} = \text{Soft-Start Time} \bullet \frac{5\mu A}{0.8V}$$

The minimum soft-start time is limited to the internal soft-start timer of 1ms. When the LTC7138 detects a fault condition (input supply undervoltage/overvoltage or overtemperature) or when the RUN pin falls below 1.1V, the SS pin is quickly pulled to ground and the internal soft-start timer is reset. This ensures an orderly restart when using an external soft-start capacitor.

Note that the soft-start capacitor may not be the limiting factor in the output voltage ramp. The maximum output current, which is equal to half of the peak current, must charge the output capacitor from 0V to its regulated value. For small peak currents or large output capacitors, this ramp time can be significant. Therefore, the output voltage ramp time from 0V to the regulated V_{OUT} value is limited to a minimum of

$$\text{Ramp Time} \geq \frac{1.33 \bullet C_{OUT}}{I_{PEAK}} V_{OUT}$$

Optimizing Output Voltage Ripple

After the peak current resistor and inductor have been selected to meet the load current and frequency requirements, an optional capacitor, C_{ISET} can be added in parallel with R_{ISET} to reduce the output voltage ripple dependency on load current.

At light loads the output voltage ripple will be a maximum. The peak inductor current is controlled by the voltage on the I_{SET} pin. The current out of the I_{SET} pin is 5µA while the LTC7138 is active and is reduced to 1µA during sleep mode. The I_{SET} current will return to 5µA on the first switching cycle after sleep mode. Placing a parallel RC network to ground on the I_{SET} pin filters the I_{SET} voltage as the LTC7138 enters and exits sleep mode, which in turn will affect the output voltage ripple, efficiency, and load step transient performance.

Higher Current Applications

For applications that require more than 400mA, the LTC7138 provides a feedback comparator output pin (FBO) for driving additional LTC7138s. When the FBO pin of a master LTC7138 is connected to the V_{FB} pin of one or more slave LTC7138s, the master controls the burst cycle of the slaves.

Figure 10 shows an example of a 5V, 800mA regulator using two LTC7138s. The master is configured for a 5V fixed output with external soft-start and V_{IN} UVLO/OVLO levels set by the RUN and OVLO pins. Since the slave is directly controlled by the master, its SS pin should be floating, RUN should be tied to V_{IN}, and OVLO should be tied to ground. Furthermore, the slave should be configured for a 1.8V fixed output (V_{PRG1} = V_{PRG2} = SS) to set the

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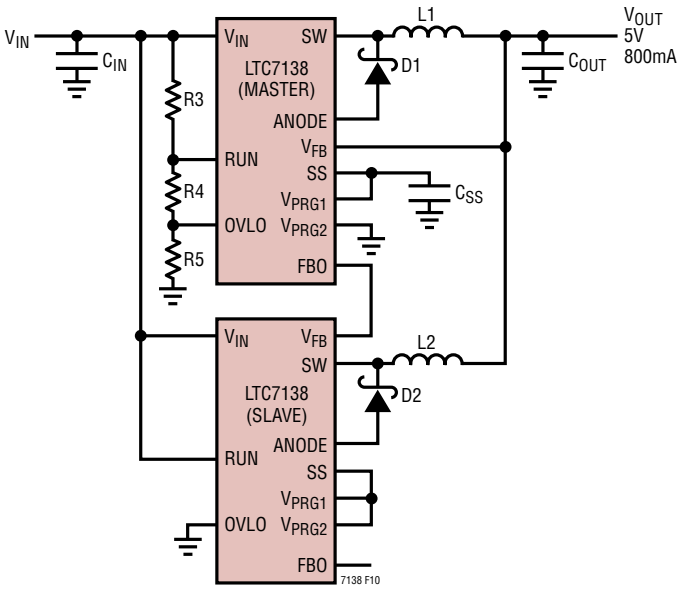

Figure 10. 5V, 800mA Regulator

V_{FB} pin threshold at 1.8V. The inductors L1 and L2 do not necessarily have to be the same, but should both meet the criteria described in the Inductor Selection section.

Thermal Considerations

In most applications, the LTC7138 does not dissipate much heat due to its high efficiency. But, in applications where the LTC7138 is running at high ambient temperature with low supply voltage and high duty cycles, such as dropout, the heat dissipated may exceed the maximum junction temperature of the part.

To prevent the LTC7138 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise from ambient to junction is given by:

$$T_R = P_D \bullet \theta_{JA}$$

Where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature is given by:

$$T_J = T_A + T_R$$

Generally, the worst-case power dissipation is in dropout at low input voltage. In dropout, the LTC7138 can provide a DC current as high as the full 575mA peak current to the output. At low input voltage, this current flows through a higher resistance MOSFET, which dissipates more power.

As an example, consider the LTC7138 in dropout at an input voltage of 5V, a load current of 610mA and an ambient temperature of 85°C. From the Typical Performance graphs of Switch On-Resistance, the $R_{DS(ON)}$ of the top switch at V_{IN} = 5V and 100°C is approximately 3.2Ω. Therefore, the power dissipated by the part is:

$$P_D = (I_{LOAD})^2 \bullet R_{DS(ON)} = (610mA)^2 \bullet 3.2\Omega = 1.19W$$

For the MSOP package the θ_{JA} is 40°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 85°C + 1.19W \bullet \frac{40°C}{W} = 133°C$$

which is below the maximum junction temperature of 150°C.

Note that the while the LTC7138 is in dropout, it can provide output current that is equal to the peak current of the part. This can increase the chip power dissipation dramatically and may cause the internal overtemperature protection circuitry to trigger at 180°C and shut down the LTC7138.

Pin Clearance/Creepage Considerations

The LTC7138 MSE package has been uniquely designed to meet high voltage clearance and creepage requirements. Pins 2, 4, 13, and 15 are omitted to increase the spacing between adjacent high voltage solder pads (V_{IN}, SW, and RUN) to a minimum of 0.657mm which is sufficient for most applications. For more information, refer to the printed circuit board design standards described in IPC-2221 (www.ipc.org).

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Design Example

As a design example, consider using the LTC7138 in an application with the following specifications: V_{IN} = 36V to 72V (48V nominal), V_{OUT} = 12V, I_{OUT} = 400mA, and that switching is enabled when V_{IN} is between 30V and 90V.

First, calculate the inductor value:

$$L = 220\mu H \bullet \frac{90V}{150V} = 132\mu H$$

Choose a 150µH inductor as a standard value. Next, verify that this meets the L_{MIN} requirement at the maximum input voltage:

$$L_{MIN} = \frac{90V \bullet 150ns}{0.610A \bullet 0.3} \bullet 1.2 = 89\mu H$$

Therefore, the minimum inductor requirement is satisfied and the 150µH inductor value may be used.

Next, C_{IN} and C_{OUT} are selected. For this design, C_{IN} should be sized for a current rating of at least:

$$I_{RMS} = 400mA \bullet \frac{12V}{36V} \bullet \sqrt{\frac{36V}{12V} - 1} \cong 189mA_{RMS}$$

The value of C_{IN} is selected to keep the input from drooping less than 1V at low line:

$$C_{IN} > \frac{150\mu H \bullet 0.61A^2}{2 \bullet 36V \bullet 1V} \cong 0.76\mu F$$

Since the capacitance of capacitors decreases with DC bias, a 1µF capacitor should be chosen.

The catch diode should have a reverse voltage rating of greater than the overvoltage lockout setting of 90V. It should also be rated for an average forward current of at least:

$$I_{D(AVG)} = 400mA \frac{90V - 12V}{90V} = 347mA$$

For margin, select a catch diode with a reverse breakdown of at least 100V and an average current of 400mA or higher.

C_{OUT} will be selected based on a value large enough to satisfy the output voltage ripple requirement. For a 1% output ripple (120mV), the value of the output capacitor can be calculated from:

$$C_{OUT} \geq \frac{0.61A \bullet 2 \bullet 10^{-6}}{120mV - \frac{12V}{160}} \cong 27\mu F$$

C_{OUT} also needs an ESR that will satisfy the output voltage ripple requirement. The required ESR can be calculated from:

$$ESR < \frac{120mV}{0.61A} \cong 197m\Omega$$

A 33µF ceramic capacitor has significantly less ESR than 197mΩ. The output voltage can now be programmed by choosing the values of R1 and R2. Since the output voltage is higher than 10V, the LTC7138 should be set for a 5V fixed output with an external divider to divide the 12V output down to 5V. R2 is chosen to be less than 200k to keep the output voltage variation to less than 1% due to the internal 5M resistor tolerance. Set R2 = 196k and calculate R1 as:

$$R1 = \frac{12V - 5V}{5V} \bullet (196k\Omega \,||\, 5M\Omega) = 264k\Omega$$

Choose a standard value of 267k for R1.

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APPLICATIONS INFORMATION

The undervoltage and overvoltage lockout requirements on V_{IN} can be satisfied with a resistive divider from V_{IN} to the RUN and OVLO pins (refer to Figure 9). Choose R3 + R4 + R5 = 2.5M to minimize the loading on V_{IN}. Calculate R3, R4 and R5 as follows:

$$R5 = \frac{1.21V \bullet 2.5M\Omega}{V_{IN\_OV(RISING)}} = 33.6k$$

$$R4 = \frac{1.21V \bullet 2.5M\Omega}{V_{IN\_UV(RISING)}} - R5 = 67.2k$$

$$R3 = 2.5M\Omega - R4 - R5 = 2.4M$$

Since specific resistor values in the megohm range are generally less available, it may be necessary to scale R3, R4, and R5 to a standard value of R3. For this example, choose R3 = 2.2M and scale R4 and R5 by 2.2M/2.4M. Then, R4 = 61.6k and R5 = 30.8k. Choose standard values of R3 = 2.2M, R4 = 62k, and R5 = 30.9k. Note that the falling thresholds for both UVLO and OVLO will be 10% less than the rising thresholds, or 27V and 81V respectively.

The I_{SET} pin should be left open in this example to select maximum peak current (610mA). Figure 11 shows a complete schematic for this design example.

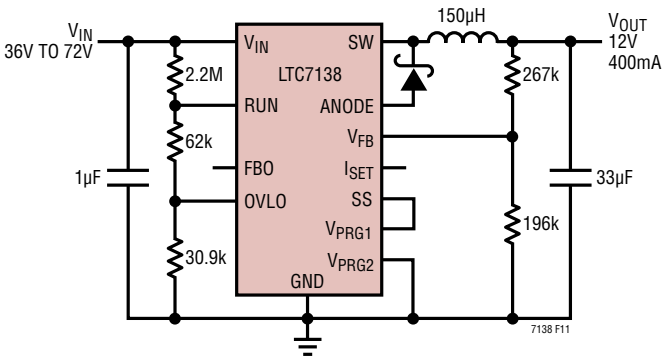
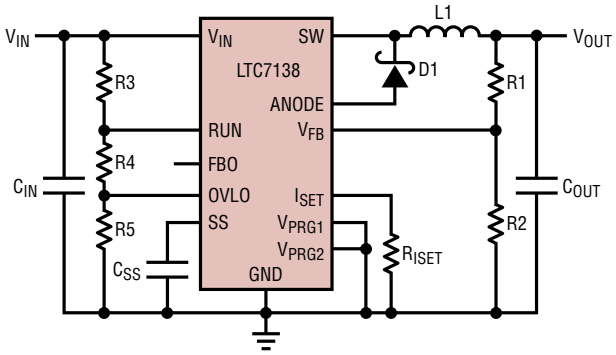


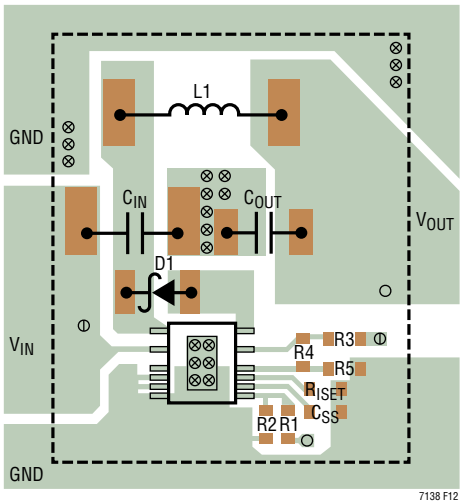
Figure 11. 36V to 72V Input to 12V Output, 400mA Regulator

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC7138. Check the following in your layout:

1. Large switched currents flow in the power switch, catch diode, and input capacitor. The loop formed by these components should be as small as possible. A ground plane is recommended to minimize ground impedance.
2. Connect the (+) terminal of the input capacitor, C_{IN}, as close as possible to the V_{IN} pin. This capacitor provides the AC current into the internal power MOSFET.
3. Keep the switching node, SW, away from all sensitive small signal nodes. The rapid transitions on the switching node can couple to high impedance nodes, in particular V_{FB}, and create increased output ripple.





⊗ VIAS TO GROUND PLANE
Φ VIAS TO INPUT SUPPLY (V_{IN})
○ VIAS TO OUTPUT SUPPLY (V_{OUT})
– – OUTLINE OF LOCAL GROUND PLANE

Figure 12. Example PCB Layout

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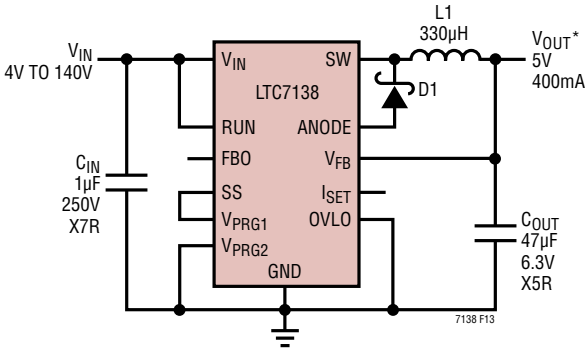
TYPICAL APPLICATIONS



L1: COILCRAFT MSS1278T-334KL
D1: DIODES INC PDS3200

*V_{OUT} = V_{IN} FOR V_{IN} < 5V

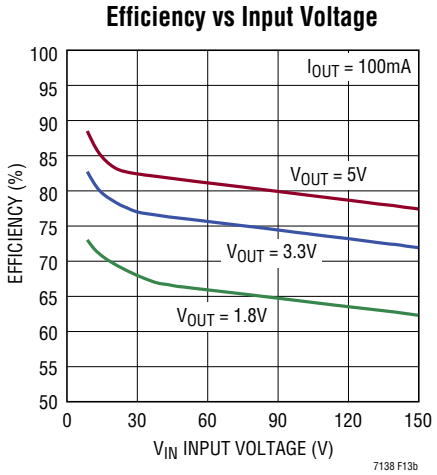
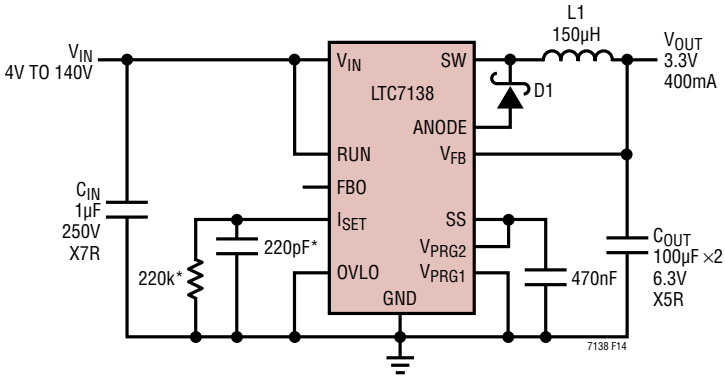


Figure 13. High Efficiency 400mA Regulator



L1: SUMIDA CDRH104RNP-151NC
D1: VISHAY U1D
*OPTIONAL COMPONENTS FOR LOWER LIGHT-LOAD OUTPUT VOLAGE RIPPLE

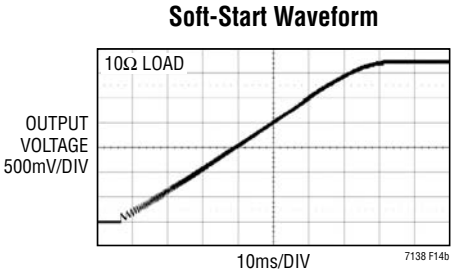
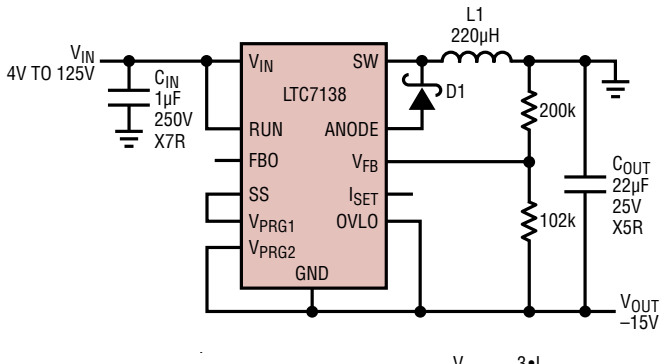


Figure 14. 3.3V/400mA Regulator with 75ms Soft-Start

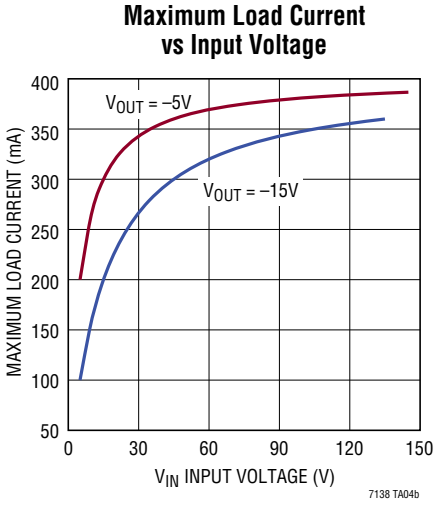
4V to 125V Input to –15V Output Positive-to-Negative Regulator



$$\text{MAXIMUM LOAD CURRENT} \approx \frac{V_{IN}}{V_{IN}+|V_{OUT}|} \bullet \frac{3 \bullet I_{PEAK}}{4}$$

MAXIMUM INPUT VOLTAGE = 140 –|V_{OUT}|

L1: TDK SLF12555-221MR72
D1: ST MICRO STTH102A



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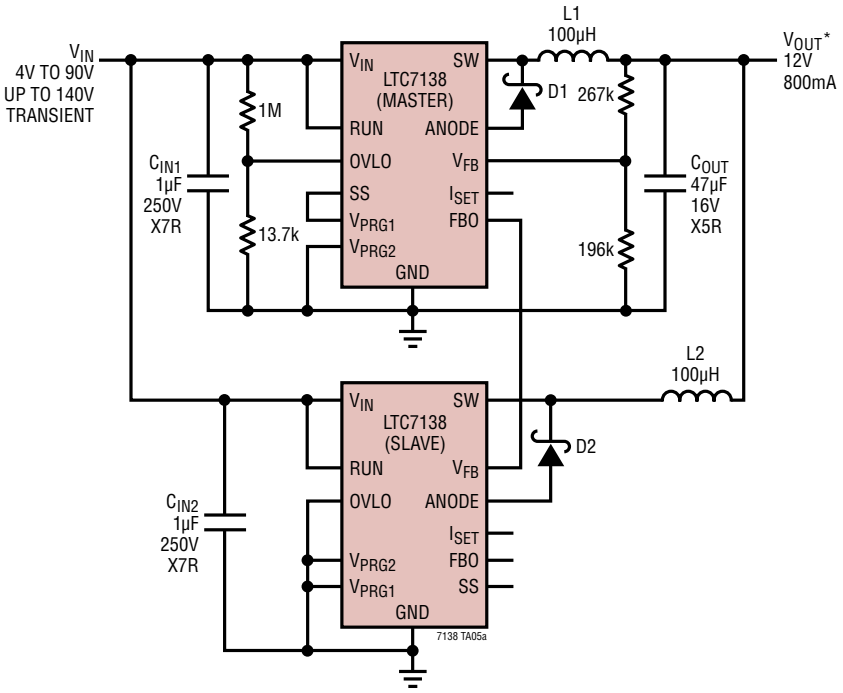
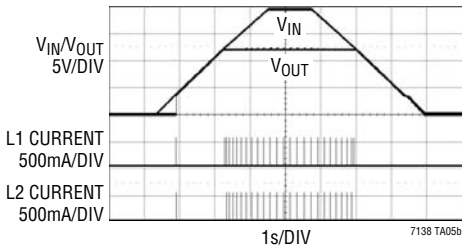
TYPICAL APPLICATIONS

4V to 90V Input to 12V/800mA Output Regulator with Overvoltage Lockout

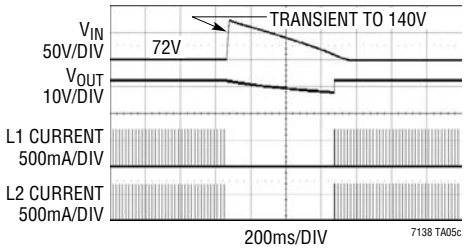


L1/L2: WÜRTH 744 770 910 1
D1/D2: CENTRAL SEMI CMSH1-100M-LTN
*V_{OUT} = V_{IN} FOR V_{IN} < 12V

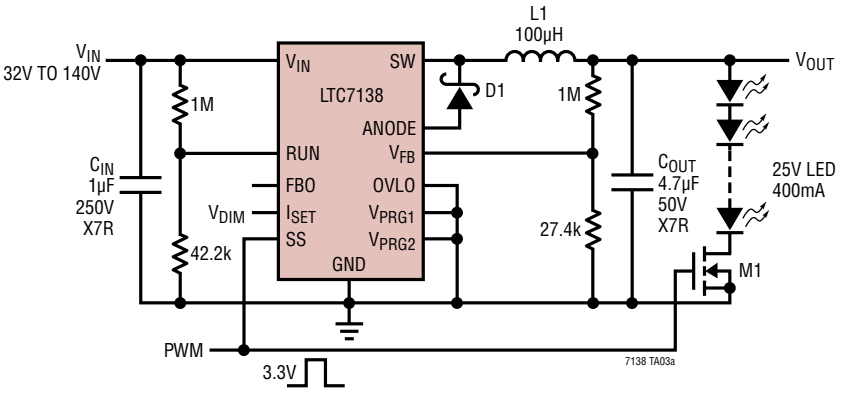
Low Dropout Startup and Shutdown



Overvoltage Lockout Operation



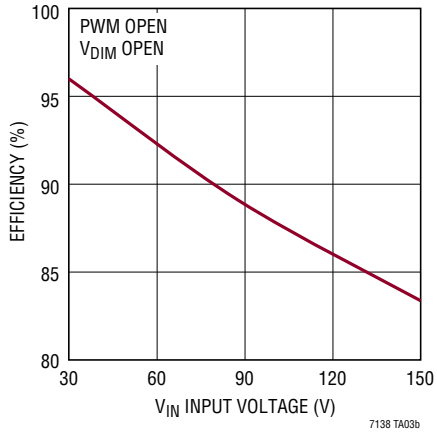
10W LED Driver



L1: TDK SLF10145T-101M
D1: TOSHIBA CRH01
M1: VISHAY SILICONIX Si2356DS

V_{DIM} = 0.1V TO 1V FOR 10:1 ANALOG DIMMING
PWM = SQUARE WAVE FOR DIGITAL DIMMING
30V OVERVOLTAGE PROTECTION ON V_{OUT}

Efficiency vs Input Voltage



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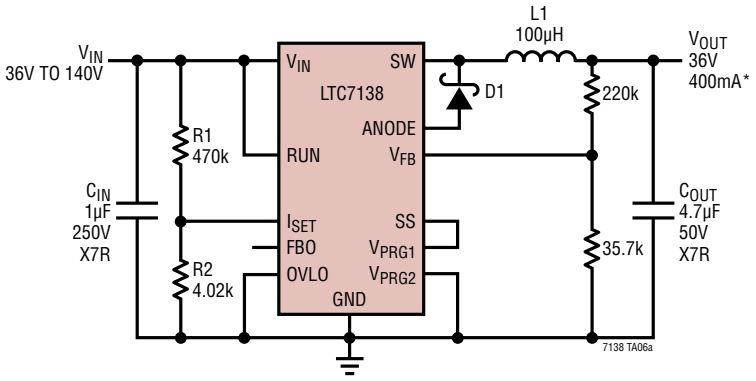
TYPICAL APPLICATIONS

36V to 140V to 36V/400mA with 120mA Input Current Limit

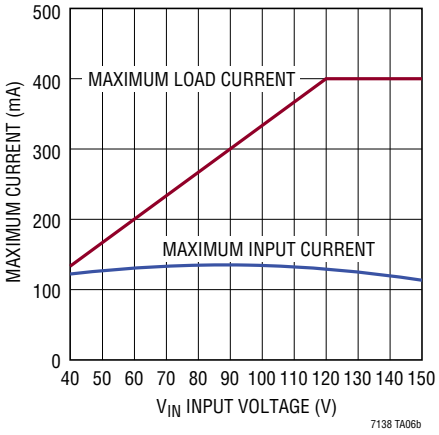


$$\text{INPUT CURRENT LIMIT} = \frac{V_{OUT}}{2.5} \bullet \frac{R2}{R1+R2} \bullet \left(1+\frac{5\mu A \bullet R1}{V_{IN}}\right) \approx \frac{V_{OUT}}{2.5} \bullet \frac{R2}{R1+R2}$$

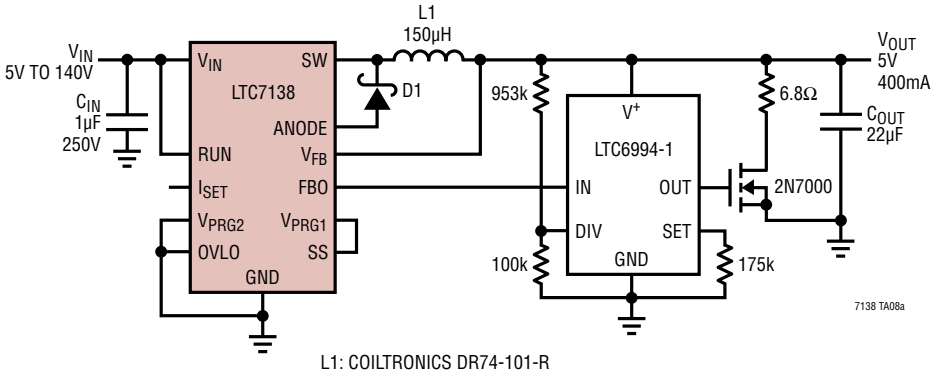
$$*\text{MAXIMUM LOAD CURRENT} = \frac{V_{IN}}{36V} \bullet 120mA \leq 400mA$$

L1: TDK SLF12555T-101M1R1
D1: ROHM RF101L2S

Maximum Load and Input Current vs Input Voltage

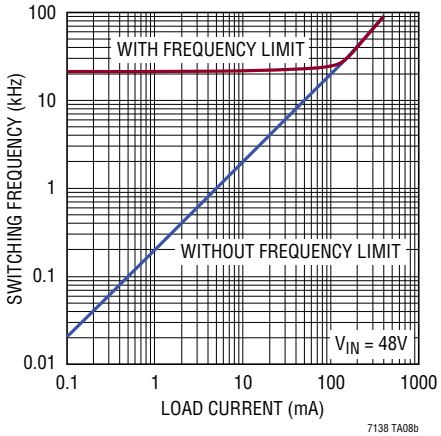


5V to 140V Input to 5V/400mA Output with 20kHz Minimum Switching Frequency

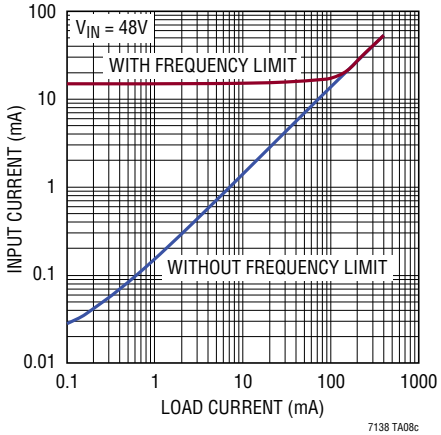


L1: COILTRONICS DR74-101-R
D1: DIODES INC MURS120-13-F

Switching Frequency vs Load Current



Input Current vs Load Current



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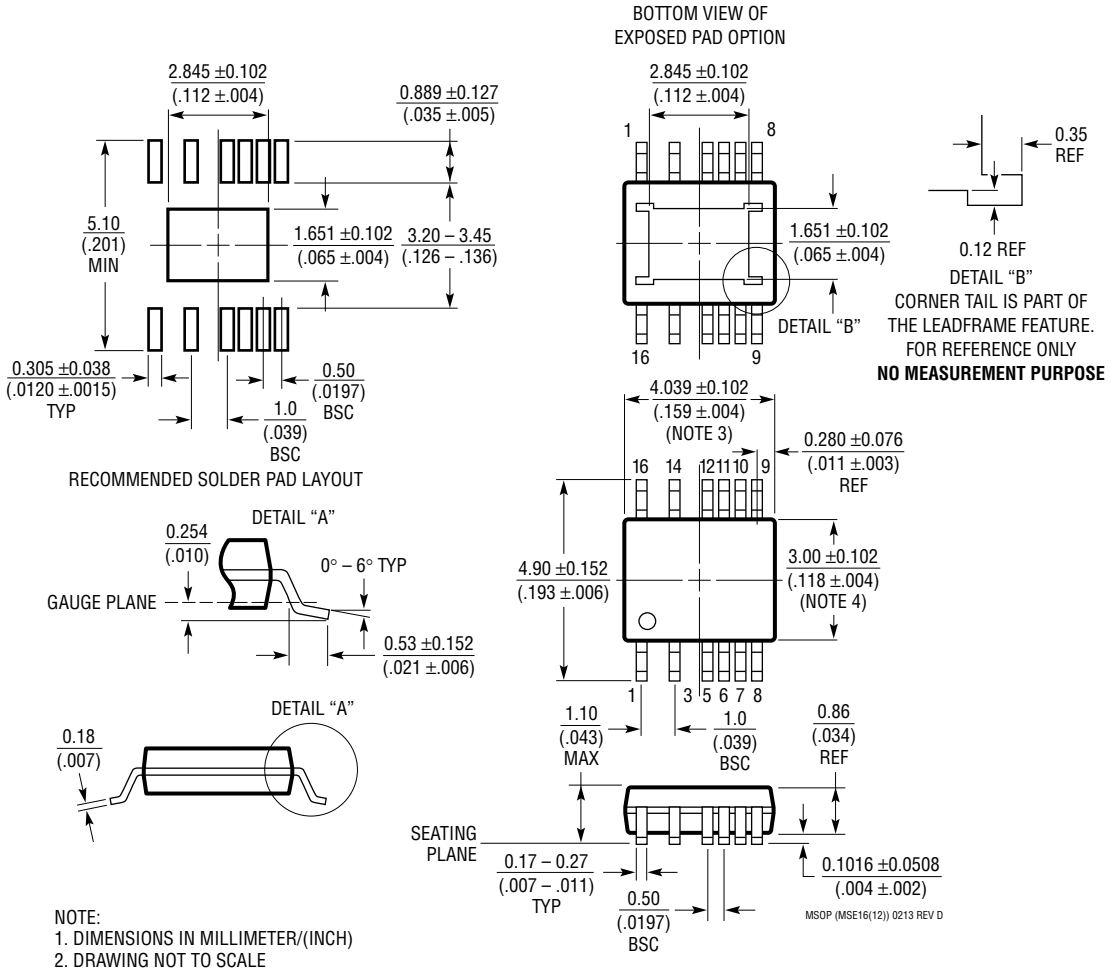
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
Variation: MSE16 (12)
16-Lead Plastic MSOP with 4 Pins Removed
Exposed Die Pad
(Reference LTC DWG # 05-08-1871 Rev D)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

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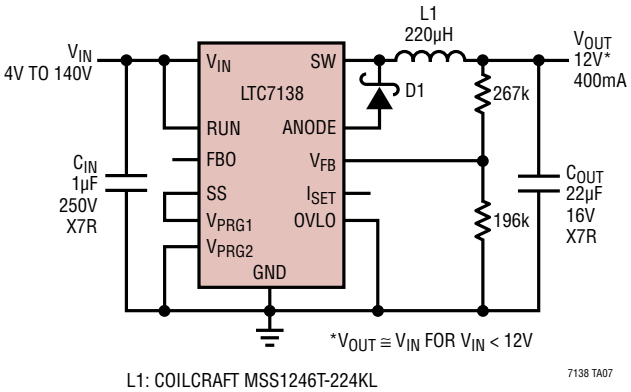
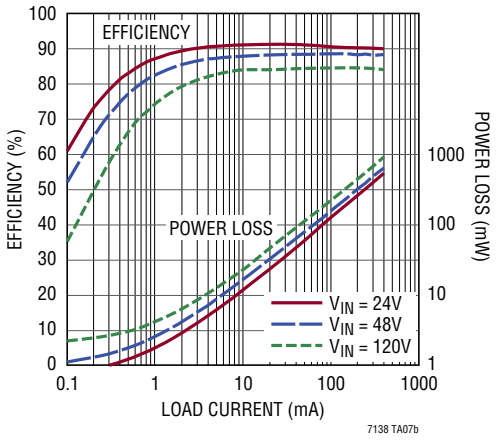
TYPICAL APPLICATION

12V/400mA Automotive Supply



L1: COILCRAFT MSS1246T-224KL
D1: DIODES INC SBR1U200P1-7

Efficiency and Power Loss vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3638	140V, 250mA Micropower Step-Down DC/DC Regulator	V_{IN}: 4V to 140V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 1.4µA, MS16E Package
LTC3639	150V, 100mA Synchronous Micropower Step-Down DC/DC Regulator	V_{IN}: 4V to 150V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 1.4µA, MS16E Package
LTC3637	76V, 1A High Efficiency Step-Down DC/DC Regulator	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 3µA, 3mm × 5mm DFN16, MSOP16E Packages
LTC3630A	76V, 500mA Synchronous Step-Down DC/DC Regulator	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} = 5µA, 3mm × 5mm DFN16, MSOP16E Packages
LTC3810	100V Synchronous Step-Down DC/DC Controller	V_{IN}: 6.4V to 100V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2mA, I_{SD} < 240µA, SSOP28 Package
LTC3631/LTC3631-3.3 LTC3631-5	45V (Transient to 60V), 100mA Synchronous Step-Down DC/DC Regulator	V_{IN}: 4.5V to 45V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 3µA, 3mm × 3mm DFN8, MSOP8 Packages
LTC3642	45V (Transient to 60V), 50mA Synchronous Step-Down DC/DC Regulator	V_{IN}: 4.5V to 45V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 3µA, 3mm × 3mm DFN8, MSOP8 Packages
LTC3632	50V (Transient to 60V), 20mA Synchronous Step-Down DC/DC Regulator	V_{IN}: 4.5V to 45V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, I_{SD} < 3µA, 3mm × 3mm DFN8, MSOP8 Packages
LTC3891	60V Synchronous Step-Down DC/DC Controller with Burst Mode Operation	V_{IN}: 4V to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 50µA, I_{SD} < 14µA, 3mm × 4mm QFN20, TSSOP20E Packages
LTC4366-1/LTC4366-2	High Voltage Surge Stopper	V_{IN}: 9V to >500V, Adjustable Output Clamp Voltage, I_{SD} < 14µA, 2mm × 3mm DFN8, TSOT-8 Packages

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