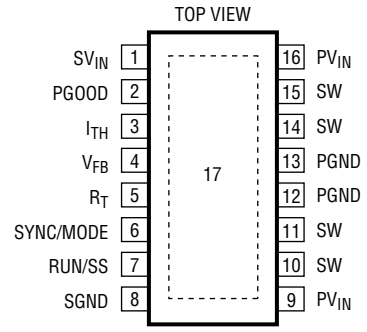
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

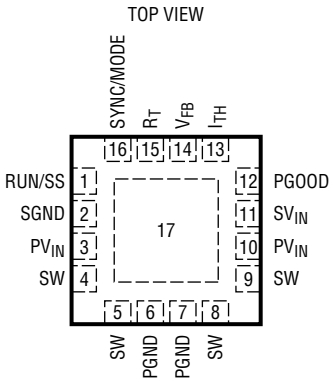
Input Supply Voltage ..... –0.3V to 6V
$I_{TH}$, RUN/SS, $V_{FB}$, PGOOD,
SYNC/MODE Voltages ..... –0.3 to $V_{IN}$
SW Voltages ..... –0.3V to ($V_{IN}$ + 0.3V)

Operating Junction Temperature Range (Notes 2, 5)
E-, I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




FE PACKAGE
16-LEAD PLASTIC TSSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 38°C/W, $\theta_{JC}$ = 10°C/W
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB




UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 37°C/W, $\theta_{JC}$ = 5°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE CONNECTED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3412AEFE#PBF | LTC3412AEFE#TRPBF | 3412AEFE | 16-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3412AIFE#PBF | LTC3412AIFE#TRPBF | 3412AIFE | 16-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3412AMPFE#PBF | LTC3412AMPFE#TRPBF | 3412AMPFE | 16-Lead Plastic TSSOP | –55°C to 125°C |
| LTC3412AEUF#PBF | LTC3412AEUF#TRPBF | 3412A | 16-Lead (4mm × 4mm) Plastic QFN | –40°C to 125°C |
| LTC3412AIUF#PBF | LTC3412AIUF#TRPBF | 3412A | 16-Lead (4mm × 4mm) Plastic QFN | –40°C to 125°C |
| **LEAD BASED FINISH** | **TAPE AND REEL** | **PART MARKING*** | **PACKAGE DESCRIPTION** | **TEMPERATURE RANGE** |
| LTC3412AEFE | LTC3412AEFE#TR | 3412AEFE | 16-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3412AIFE | LTC3412AIFE#TR | 3412AIFE | 16-Lead Plastic TSSOP | –40°C to 125°C |
| LTC3412AMPFE | LTC3412AMPFE#TR | 3412AMPFE | 16-Lead Plastic TSSOP | –55°C to 125°C |
| LTC3412AEUF | LTC3412AEUF#TR | 3412A | 16-Lead (4mm × 4mm) Plastic QFN | –40°C to 125°C |
| LTC3412AIUF | LTC3412AIUF#TR | 3412A | 16-Lead (4mm × 4mm) Plastic QFN | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C. $V_{IN}$ = 3.3V unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $SV_{IN}$ | Signal Input Voltage Range | | | 2.25 | | 5.5 | V |
| $V_{FB}$ | Regulated Feedback Voltage | (Note 3)<br>E-, I-Grades<br>MP-Grade | <br>●<br>● | <br>0.784<br>0.780 | <br>0.800<br>0.800 | <br>0.816<br>0.816 | <br>V<br>V |
| $I_{FB}$ | Voltage Feedback Leakage Current | | | | 0.1 | 0.2 | µA |
| $\Delta V_{FB}$ | Reference Voltage Line Regulation | $V_{IN}$ = 2.7V to 5.5V (Note 3) | ● | | 0.04 | 0.2 | %V |
| $V_{LOADREG}$ | Output Voltage Load Regulation | Measured in Servo Loop, $V_{ITH}$ = 0.36V<br>Measured in Servo Loop, $V_{ITH}$ = 0.84V | ●<br>● | | 0.02<br>–0.02 | 0.2<br>–0.2 | %<br>% |
| $\Delta V_{PGOOD}$ | Power Good Range | | | | ±7.5 | ±9 | % |
| $R_{PGOOD}$ | Power Good Pull-Down Resistance | | | | 120 | 200 | Ω |
| $I_Q$ | Input DC Bias Current<br>Active Current<br>Sleep<br>Shutdown | (Note 4)<br>$V_{FB}$ = 0.78V, $V_{ITH}$ = 1V<br>$V_{FB}$ = 1V, $V_{ITH}$ = 0V<br>$V_{RUN}$ = 0V, $V_{MODE}$ = 0V | | <br><br><br> | <br>250<br>64<br>0.02 | <br>330<br>80<br>1 | <br>µA<br>µA<br>µA |
| $f_{OSC}$ | Switching Frequency<br>Switching Frequency Range | $R_{OSC}$ = 294kΩ<br>(Note 6) | | 0.88<br>0.3 | 1 | 1.1<br>4 | MHz<br>MHz |
| $f_{SYNC}$ | SYNC Capture Range | (Note 6) | | 0.3 | | 4 | MHz |
| $R_{PFET}$ | $R_{DS(ON)}$ of P-Channel FET | $I_{SW}$ = 1A (Note 7) | | | 77 | 110 | mΩ |
| $R_{NFET}$ | $R_{DS(ON)}$ of N-Channel FET | $I_{SW}$ = –1A (Note 7) | | | 65 | 90 | mΩ |
| $I_{LIMIT}$ | Peak Current Limit | | | 4.5 | 6 | | A |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | | | 1.75 | 2 | 2.25 | V |
| $I_{LSW}$ | SW Leakage Current | $V_{RUN}$ = 0V, $V_{IN}$ = 5.5V | | | 0.1 | 1 | µA |
| $V_{RUN}$ | RUN Threshold | | | 0.5 | 0.65 | 0.8 | V |
| $I_{RUN}$ | RUN/SS Leakage Current | | | | | 1 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3412AE is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3412AI is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range. The LTC3412AMP is guaranteed and tested to meet performance specifications over the full –55°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 3:** The LTC3412A is tested in a feedback loop that adjusts $V_{FB}$ to achieve a specified error amplifier output voltage ($I_{TH}$).

**Note 4:** Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

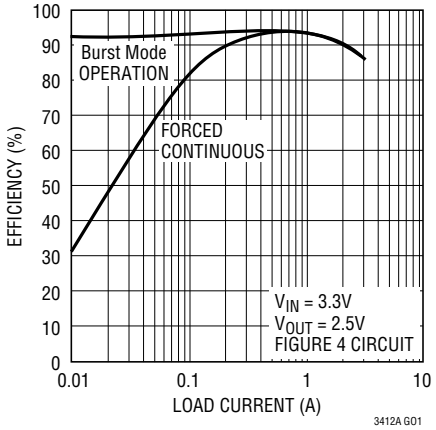
**Note 5:** $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation as follows: LTC3412AFE: $T_J = T_A + P_D$ (38°C/W)
LTC3412AUF: $T_J = T_A + P_D$ (34°C/W)

**Note 6:** 4MHz operation is guaranteed by design and not production tested.

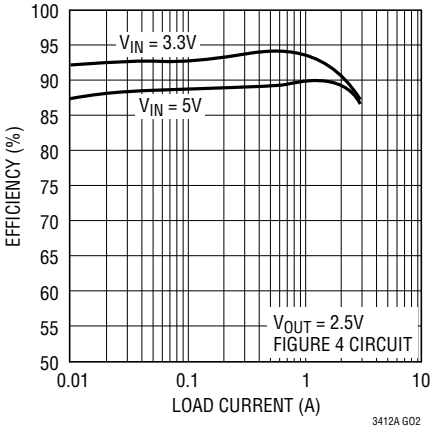
**Note 7:** Switch on resistance is guaranteed by design and test condition in the UF package and by final test correlation in the FE package.

# TYPICAL PERFORMANCE CHARACTERISTICS

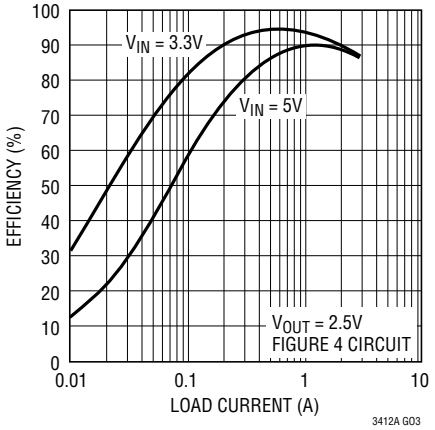
### Efficiency vs Load Current



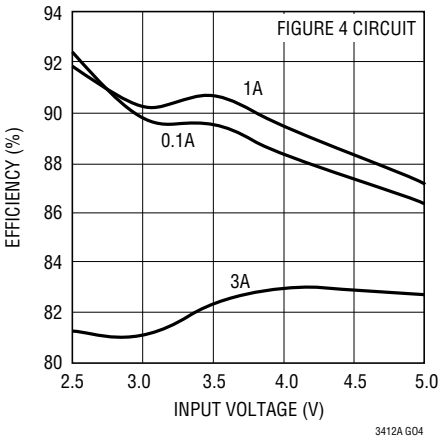

### Efficiency vs Load Current, Burst Mode Operation



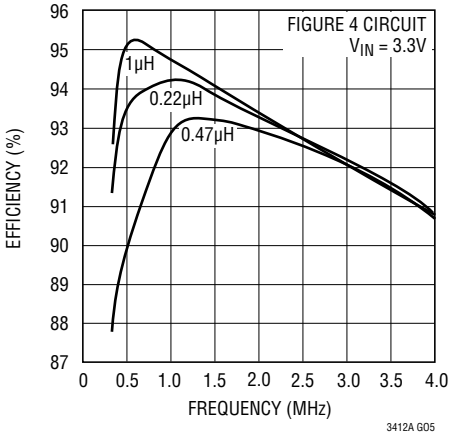

### Efficiency vs Load Current, Forced Continuous Operation



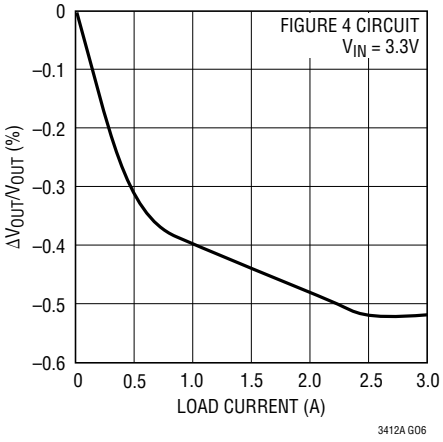

### Efficiency vs Input Voltage



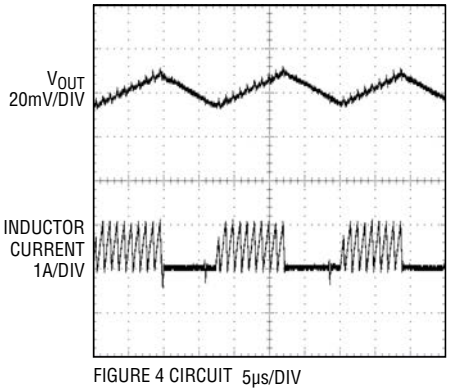

### Efficiency vs Frequency



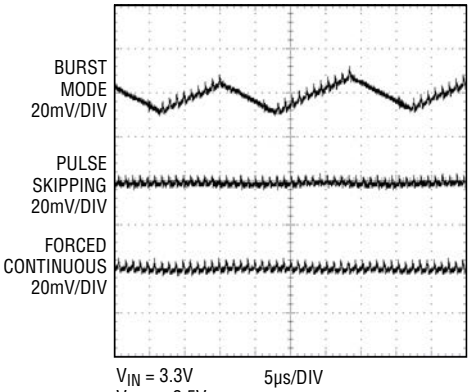

### Load Regulation



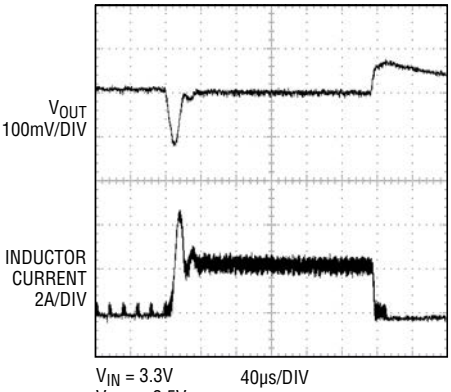

### Burst Mode Operation




### Output Voltage Ripple

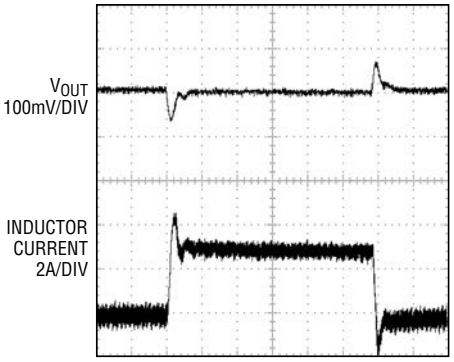



### Load Step Transient Burst Mode Operation



# TYPICAL PERFORMANCE CHARACTERISTICS

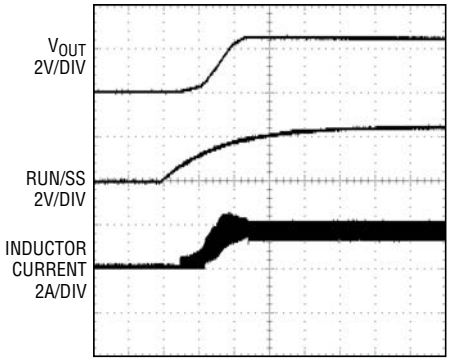
### Load Step Transient Forced Continuous




$V_{IN}$ = 3.3V 40µs/DIV
$V_{OUT}$ =2.5V
f = 1MHz
LOAD STEP = 0A TO 3A
FIGURE 4 CIRCUIT

3412A G10

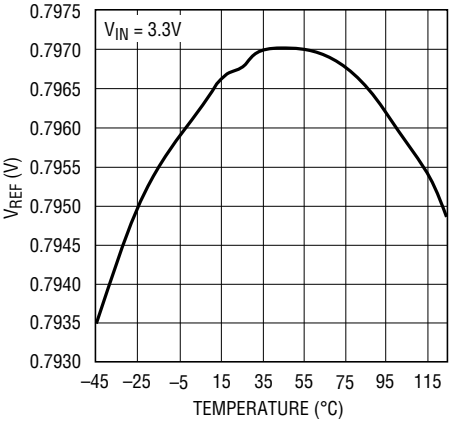
### Start-Up Transient




$V_{IN}$ = 3.3V 1ms/DIV
$V_{OUT}$ =2.5V
LOAD STEP = 2A
FIGURE 4 CIRCUIT

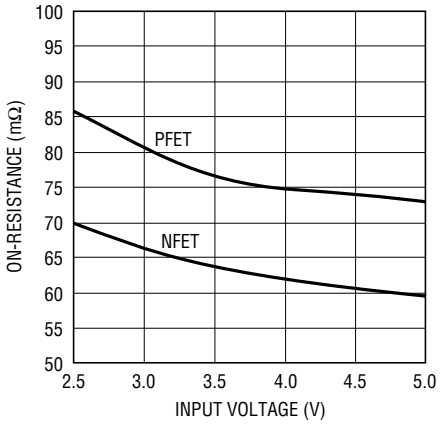
3412A G11

### $V_{REF}$ vs Temperature



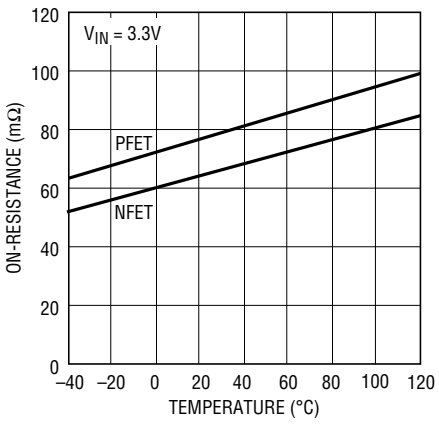

3412A G12

### Switch On-Resistance vs Input Voltage



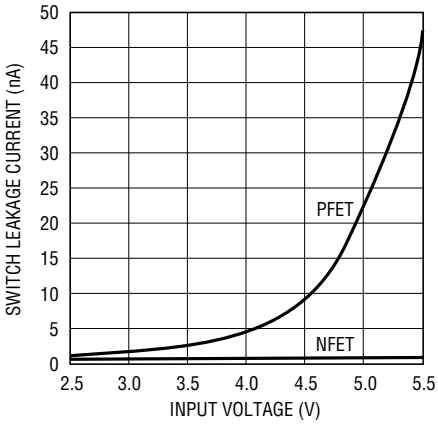

3412A G13

### Switch On-Resistance vs Temperature



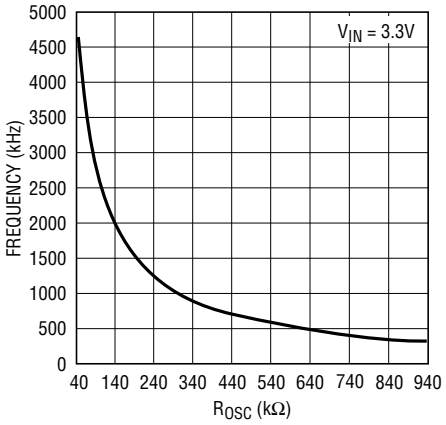

3412A G14

### Switch Leakage Current vs Input Voltage



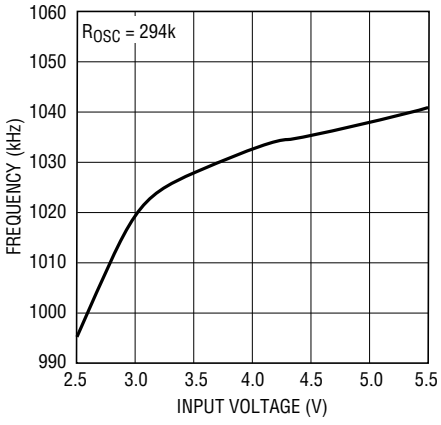

3412A G15

### Frequency vs $R_{OSC}$



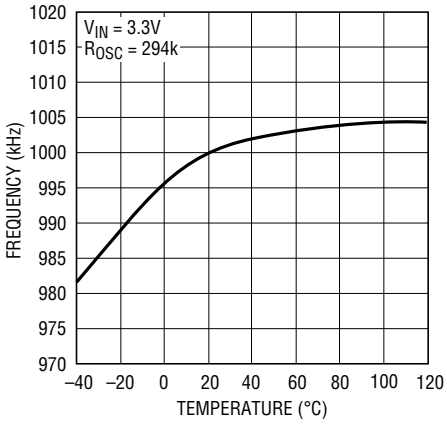

3412A G16

### Frequency vs Input Voltage




3412A G17

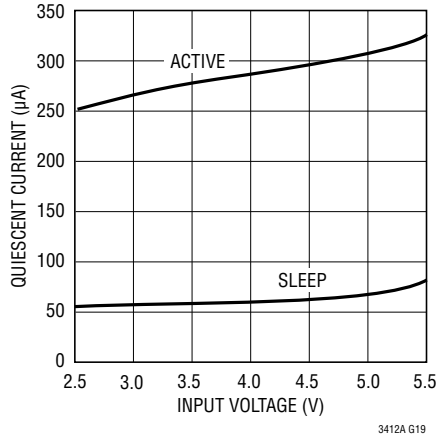
### Frequency vs Temperature



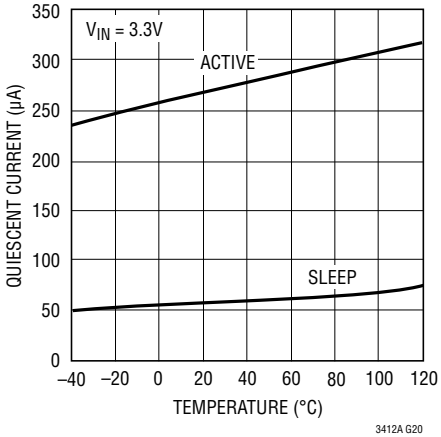

3412A G18

## TYPICAL PERFORMANCE CHARACTERISTICS

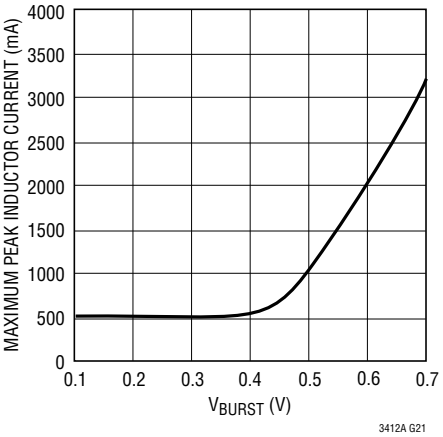
**Quiescent Current vs Input Voltage**



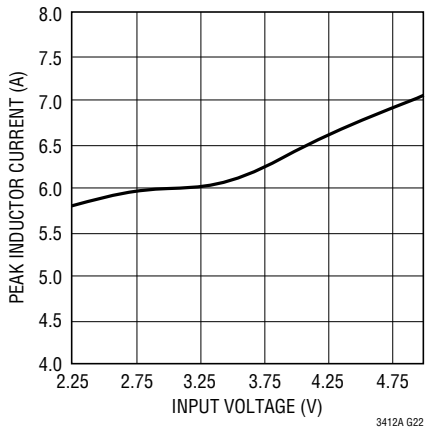

**Quiescent Current vs Temperature**




**Minimum Peak Inductor Current vs Burst Clamp Voltage**




**Peak Current vs Input Voltage**



## PIN FUNCTIONS (FE/UHF)

**$SV_{IN}$ (Pin 1/Pin 11):** Signal Input Supply. Decouple this pin to SGND with a capacitor.

**PGOOD (Pin 2/Pin 12):** Power Good Output. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of regulation point.

**$I_{TH}$ (Pin 3/Pin 13):** Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is from 0.2V to 1.4V with 0.4V corresponding to the zero-sense voltage (zero current).

**$V_{FB}$ (Pin 4/Pin 14):** Feedback Pin. Receives the feedback voltage from a resistive divider connected across the output.

**$R_T$ (Pin 5/Pin 15):** Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency.

**SYNC/MODE (Pin 6/Pin 16):** Mode Select and External Clock Synchronization Input. To select forced continuous, tie to $SV_{IN}$. Connecting this pin to a voltage between 0V and 1V selects Burst Mode operation with the burst clamp set to the pin voltage.

**RUN/SS (Pin 7/Pin 1):** Run Control and Soft-Start Input. Forcing this pin below 0.5V shuts down the LTC3412A. In shutdown all functions are disabled drawing <1µA of supply current. A capacitor to ground from this pin sets the ramp time to full output current.

**SGND (Pin 8/Pin 2):** Signal Ground. All small-signal components, compensation components and the exposed pad on the bottom side of the IC should connect to this ground, which in turn connects to PGND at one point.

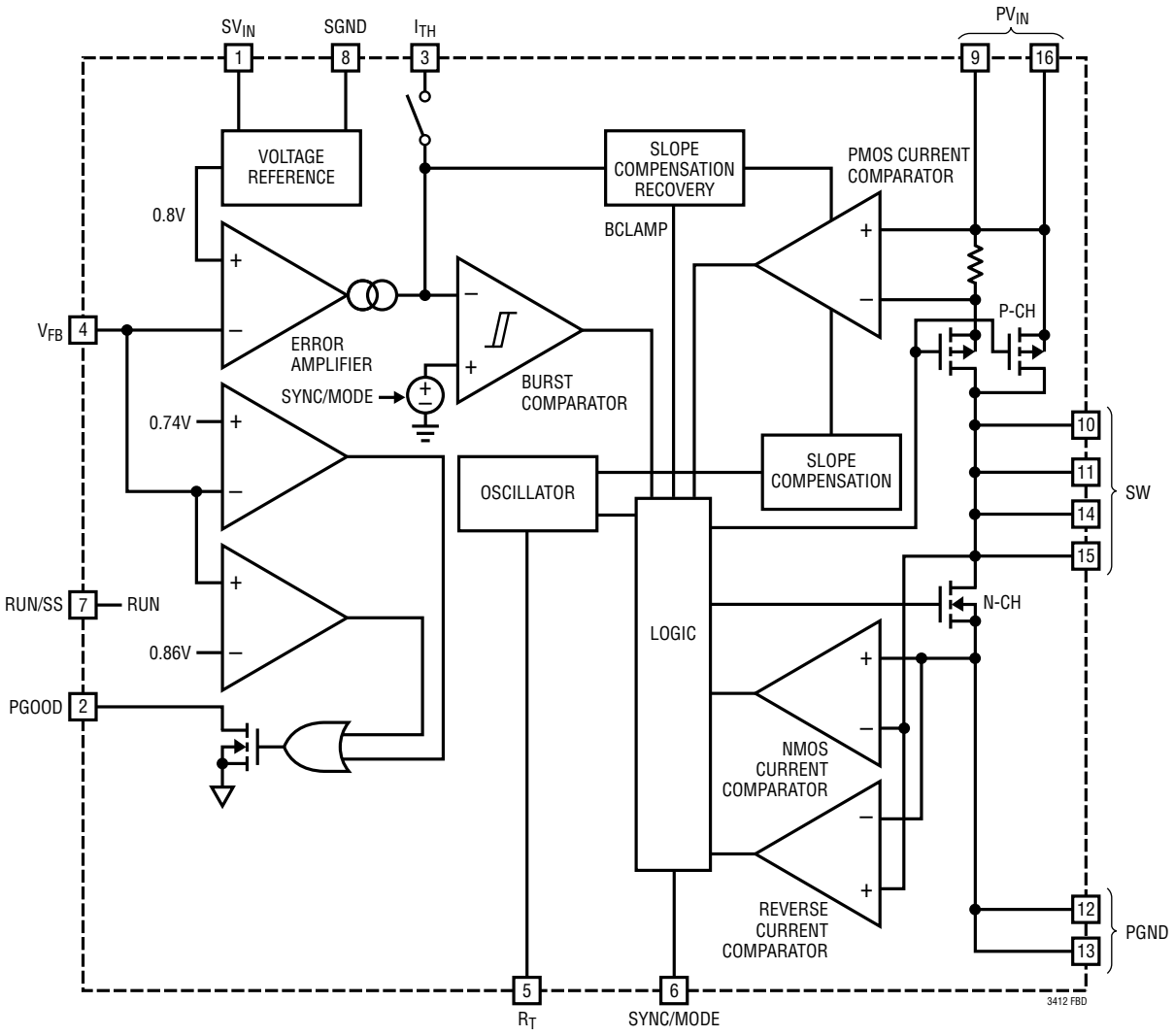
**$PV_{IN}$ (Pins 9, 16/Pins 3, 10):** Power Input Supply. Decouple this pin to PGND with a capacitor.

**SW (Pins 10, 11, 14, 15/Pins 4, 5, 8, 9):** Switch Node Connection to the Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

**PGND (Pins 12, 13/Pins 6, 7):** Power Ground. Connect this pin close to the (–) terminal of $C_{IN}$ and $C_{OUT}$.

**Exposed Pad (Pin 17/Pin 17):** Signal Ground. Must be soldered to PCB for electrical connection and rated thermal performance.

## FUNCTIONAL BLOCK DIAGRAM




## OPERATION

### Main Control Loop

The LTC3412A is a monolithic, constant-frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the current comparator trips and turns off the top power MOSFET. The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the $I_{TH}$ pin. The error amplifier adjusts the voltage on the $I_{TH}$ pin by comparing the feedback signal from a resistor divider on the $V_{FB}$ pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the $I_{TH}$ voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-channel MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle. The bottom current limit is set at –1.3A for forced continuous mode and 0A for Burst Mode operation.

## OPERATION

The operating frequency is externally set by an external resistor connected between the $R_T$ pin and ground. The practical switching frequency can range from 300kHz to 4MHz.

Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage comes out of regulation by ±7.5%. In an overvoltage condition, the top power MOSFET is turned off and the bottom power MOSFET is switched on until either the overvoltage condition clears or the bottom MOSFET's current limit is reached.

### Forced Continuous Mode

Connecting the SYNC/MODE pin to $SV_{IN}$ will disable Burst Mode operation and force continuous current operation. At light loads, forced continuous mode operation is less efficient than Burst Mode operation, but may be desirable in some applications where it is necessary to keep switching harmonics out of a signal band. The output voltage ripple is minimized in this mode.

### Burst Mode Operation

Connecting the SYNC/MODE pin to a voltage in the range of 0V to 1V enables Burst Mode operation. In Burst Mode operation, the internal power MOSFETs operate intermittently at light loads. This increases efficiency by minimizing switching losses. During Burst Mode operation, the minimum peak inductor current is externally set by the voltage on the SYNC/MODE pin and the voltage on the $I_{TH}$ pin is monitored by the burst comparator to determine when sleep mode is enabled and disabled. When the average inductor current is greater than the load current, the voltage on the $I_{TH}$ pin drops. As the $I_{TH}$ voltage falls below 150mV, the burst comparator trips and enables sleep mode. During sleep mode, the top power MOSFET is held off and the $I_{TH}$ pin is disconnected from the output of the error amplifier. The majority of the internal circuitry is also turned off to reduce the quiescent current to 64µA while the load current is solely supplied by the output capacitor. When the output voltage drops, the $I_{TH}$ pin is reconnected to the output of the error amplifier and the top power MOSFET along with all the internal circuitry is switched back on. This process repeats at a rate that is dependent on the load demand.

Pulse-skipping operation is implemented by connecting the SYNC/MODE pin to ground. This forces the burst clamp level to be at 0V. As the load current decreases, the peak inductor current will be determined by the voltage on the $I_{TH}$ pin until the $I_{TH}$ voltage drops below 400mV. At this point, the peak inductor current is determined by the minimum on-time of the current comparator. If the load demand is less than the average of the minimum on-time inductor current, switching cycles will be skipped to keep the output voltage in regulation.

### Frequency Synchronization

The internal oscillator of the LTC3412A can be synchronized to an external clock connected to the SYNC/MODE pin. The frequency of the external clock can be in the range of 300kHz to 4MHz. For this application, the oscillator timing resistor should be chosen to correspond to a frequency that is 25% lower than the synchronization frequency. During synchronization, the burst clamp is set to 0V, and each switching cycle begins at the falling edge of the clock signal.

### Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-channel MOSFET and the inductor.

### Low Supply Operation

The LTC3412A is designed to operate down to an input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-channel and N-channel power switches increases. The user should calculate the power dissipation when the LTC3412A is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

## APPLICATIONS INFORMATION

### Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the LTC3412A, however, slope compensation recovery is implemented to keep the maximum inductor peak current constant throughout the range of duty cycles. This keeps the maximum output current relatively constant regardless of duty cycle.

### Short-Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. To prevent current runaway from occurring, a secondary current limit is imposed on the inductor current. If the inductor valley current increases larger than 4.4A, the top power MOSFET will be held off and switching cycles will be skipped until the inductor current is reduced.

The basic LTC3412A application circuit is shown in Figure 1. External component selection is determined by the maximum load current and begins with the selection of the operating frequency and inductor value followed by $C_{IN}$ and $C_{OUT}$.

### Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency of the LTC3412A is determined by an external resistor that is connected between pin $R_T$ and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{OSC} = \frac{3.08 \bullet 10^{11}}{f}(\Omega) - 10k\Omega$$

Although frequencies as high as 4MHz are possible, the minimum on-time of the LTC3412A imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns; therefore, the minimum duty cycle is equal to 100 • 110ns • f(Hz).

### Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current $\Delta I_L$ increases with higher $V_{IN}$ or $V_{OUT}$ and decreases with higher inductance.

$$\Delta I_L = \left(\frac{V_{OUT}}{fL}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces the core losses in the inductor, the ESR losses in the output capacitors, and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor.

A reasonable starting point for selecting the ripple current is $\Delta I_L = 0.4(I_{MAX})$. The largest ripple current occurs at the highest $V_{IN}$. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \left(\frac{V_{OUT}}{f\Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition to low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

### Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

## APPLICATIONS INFORMATION

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price verus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

### $C_{IN}$ and $C_{OUT}$ Selection

The input capacitance, $C_{IN}$, is needed to filter the trapezoidal wave current at the source of the top MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT/2}$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of $C_{OUT}$ is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, $\Delta V_{OUT}$, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

## APPLICATIONS INFORMATION

### Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8V\left(1+\frac{R2}{R1}\right)$$

The resistive divider allows pin $V_{FB}$ to sense a fraction of the output voltage as shown in Figure 2.

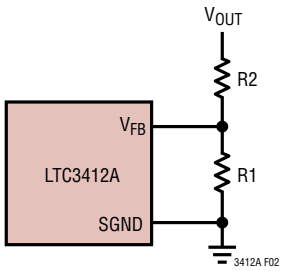



**Figure 2. Setting the Output Voltage**

### Burst Clamp Programming

If the voltage on the SYNC/MODE pin is less than $V_{IN}$ by 1V, Burst Mode operation is enabled. During Burst Mode Operation, the voltage on the SYNC/MODE pin determines the burst clamp level, which sets the minimum peak inductor current, $I_{BURST}$. To select the burst clamp level, use the graph of Minimum Peak Inductor Current vs Burst Clamp Voltage in the Typical Performance Characteristics section.

$V_{BURST}$ is the voltage on the SYNC/MODE pin. $I_{BURST}$ can only be programmed in the range of 0A to 6A. For values of $V_{BURST}$ greater than 1V, $I_{BURST}$ is set at 6A. For values of $V_{BURST}$ less than 0.4V, $I_{BURST}$ is set at 0A. As the output load current drops, the peak inductor currents decrease to keep the output voltage in regulation. When the output load current demands a peak inductor current that is less than $I_{BURST}$, the burst clamp will force the peak inductor current to remain equal to $I_{BURST}$ regardless of further reductions in the load current. Since the average inductor current is greater than the output load current, the voltage on the $I_{TH}$ pin will decrease. When the $I_{TH}$ voltage drops to 150mV, sleep mode is enabled in which both power MOSFETs are shut off along with most of the circuitry to minimize power consumption. All circuitry is turned back on and the power MOSFETs begin switching again when the output voltage drops out of regulation.

The value for $I_{BURST}$ is determined by the desired amount of output voltage ripple. As the value of $I_{BURST}$ increases, the sleep period between pulses and the output voltage ripple increase. The burst clamp voltage, $V_{BURST}$, can be set by a resistor divider from the $V_{FB}$ pin to the SGND pin as shown in Figure 1.

Pulse skipping, which is a compromise between low output voltage ripple and efficiency, can be implemented by connecting pin SYNC/MODEto ground. This sets $I_{BURST}$ to 0A. In this condition, the peak inductor current is limited by the minimum on-time of the current comparator. The lowest output voltage ripple is achieved while still operating discontinuously. During very light output loads, pulse skipping allows only a few switching cycles to be skipped while maintaining the output voltage in regulation.

### Frequency Synchronization

The LTC3412A's internal oscillator can be synchronized to an external clock signal. During synchronization, the top MOSFET turn-on is locked to the **falling** edge of the external frequency source. The synchronization frequency range is 300kHz to 4MHz. Synchronization only occurs if the external frequency is greater than the frequency set by the external resistor. Because slope compensation is generated by the oscillator's RC circuit, the external frequency should be set 25% higher than the frequency set by the external resistor to ensure that adequate slope compensation is present.

### Soft-Start

The RUN/SS pin provides a means to shut down the LTC3412A as well as a timer for soft-start. Pulling the RUN/SS pin below 0.5V places the LTC3412A in a low quiescent current shutdown state ($I_Q$ < 1µA).

The LTC3412A contains an internal soft-start clamp that gradually raises the clamp on $I_{TH}$ after the RUN/SS pin is pulled above 2V. The full current range becomes available on $I_{TH}$ after 1024 switching cycles. If a longer soft-start period is desired, the clamp on $I_{TH}$ can be set externally with a resistor and capacitor on the RUN/SS pin as shown in Figure 1. The soft-start duration can be calculated by using the following formula:

$$t_{SS} = R_{SS}\,C_{SS}\,\ln\left(\frac{V_{IN}}{V_{IN}-1.8V}\right)(\text{SECONDS})$$

## APPLICATIONS INFORMATION

### Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: $V_{IN}$ quiescent current and $I^2R$ losses.

The $V_{IN}$ quiescent current loss dominates the efficiency loss at very low load currents whereas the $I^2R$ loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The $V_{IN}$ quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from $V_{IN}$ to ground. The resulting dQ/dt is the current out of $V_{IN}$ that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(QT + QB)$ where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to $V_{IN}$; thus, their effects will be more pronounced at higher supply voltages.
2. $I^2R$ losses are calculated from the resistances of the internal switches, $R_{SW}$, and external inductor $R_L$. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1 – DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. To obtain $I^2R$ losses, simply add $R_{SW}$ to $R_L$ and multiply the result by the square of the average output current.

Other losses including $C_{IN}$ and $C_{OUT}$ ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

### Thermal Considerations

In most applications, the LTC3412A does not dissipate much heat due to its high efficiency.

However, in applications where the LTC3412A is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3412A from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$t_r = (P_D)(\theta_{JA})$$

where $P_D$ is the power dissipated by the regulator and $\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature. For the 16-lead exposed TSSOP package, the $\theta_{JA}$ is 38°C/W. For the 16-lead QFN package the $\theta_{JA}$ is 34°C/W.

The junction temperature, $T_J$, is given by:

$$T_J = T_A + t_r$$

where $T_A$ is the ambient temperature.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$). To maximize the thermal performance of the LTC3412A, the Exposed Pad should be soldered to a ground plane.

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current.

## APPLICATIONS INFORMATION

When a load step occurs, $V_{OUT}$ immediately shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$ generating a feedback error signal used by the regulator to return $V_{OUT}$ to its steady-state value. During this recovery time, $V_{OUT}$ can be monitored for overshoot or ringing that would indicate a stability problem. The $I_{TH}$ pin external components and output capacitor shown in Figure 1 will provide adequate compensation for most applications.

### Design Example

As a design example, consider using the LTC3412A in an application with the following specifications:

$V_{IN}$ = 3.3V, $V_{OUT}$ = 2.5V, $I_{OUT(MAX)}$ = 3A,
$I_{OUT(MIN)}$ = 100mA, f = 1MHz.

Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

First, calculate the timing resistor:

$$R_{OSC} = \frac{3.08 \bullet 10^{11}}{1 \bullet 10^{6}} - 10k = 298k$$

Use a standard value of 294k. Next, calculate the inductor value for about 40% ripple current at maximum $V_{IN}$:

$$L = \left(\frac{2.5V}{(1MHz)(1.2A)}\right)\left(1 - \frac{2.5V}{3.3V}\right) = 0.51\mu H$$

Using a 0.47µH inductor results in a maximum ripple current of:

$$\Delta I_L = \left(\frac{2.5V}{(1MHz)(0.47\mu H)}\right)\left(1 - \frac{2.5V}{3.3V}\right) = 1.29A$$

$C_{OUT}$ will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 100µF ceramic capacitors will be used.
$C_{IN}$ should be sized for a maximum current rating of:

$$I_{RMS} = (3A)\left(\frac{2.5V}{3.3V}\right)\sqrt{\frac{3.3V}{2.5V} - 1} = 1.29A_{RMS}$$

Decoupling the $PV_{IN}$ and $SV_{IN}$ pins with two 22µF capacitors is adequate for most applications.

The burst clamp and output voltage can now be programmed by choosing the values of R1, R2 and R3. The voltage on pin MODE will be set to 0.50V by the resistor divider consisting of R2 and R3. According to the graph of Minimum Peak Inductor Current vs Burst Clamp Voltage in the Typical Performance Characteristics section, a burst clamp voltage of 0.5V will set the minimum inductor current, $I_{BURST}$, to approximately 1.1A.

If we set the sum of R2 and R3 to 185k, then the following equations can be solved:

$$R2 + R3 = 185k$$

$$1 + \frac{R2}{R3} = \frac{0.8V}{0.50V}$$

The two equations shown above result in the following values for R2 and R3: R2 = 69.8k , R3 = 115k. The value of R1 can now be determined by solving the following equation.

$$1 + \frac{R1}{185k} = \frac{2.5V}{0.8V}$$

$$R1 = 392k$$

A value of 392k will be selected for R1. Figure 4 shows the complete schematic for this design example.

### PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3412A. Check the following in your layout:

1. A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small signal components returning to the SGND pin at one point which is then connected to the PGND pin close to the LTC3412A.
2. Connect the (+) terminal of the input capacitor(s), $C_{IN}$, as close as possible to the $PV_{IN}$ pin. This capacitor provides the AC current into the internal power MOSFETs.

## APPLICATIONS INFORMATION

3. Keep the switching node, SW, away from all sensitive small-signal nodes.
4. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net ($PV_{IN}$, $SV_{IN}$, $V_{OUT}$, PGND, SGND, or any other DC rail in your system).
5. Connect the $V_{FB}$ pin directly to the feedback resistors. The resistor divider must be connected between $V_{OUT}$ and SGND.

**Top** **Bottom**

**Figure 3. LTC3412A Layout Diagram**

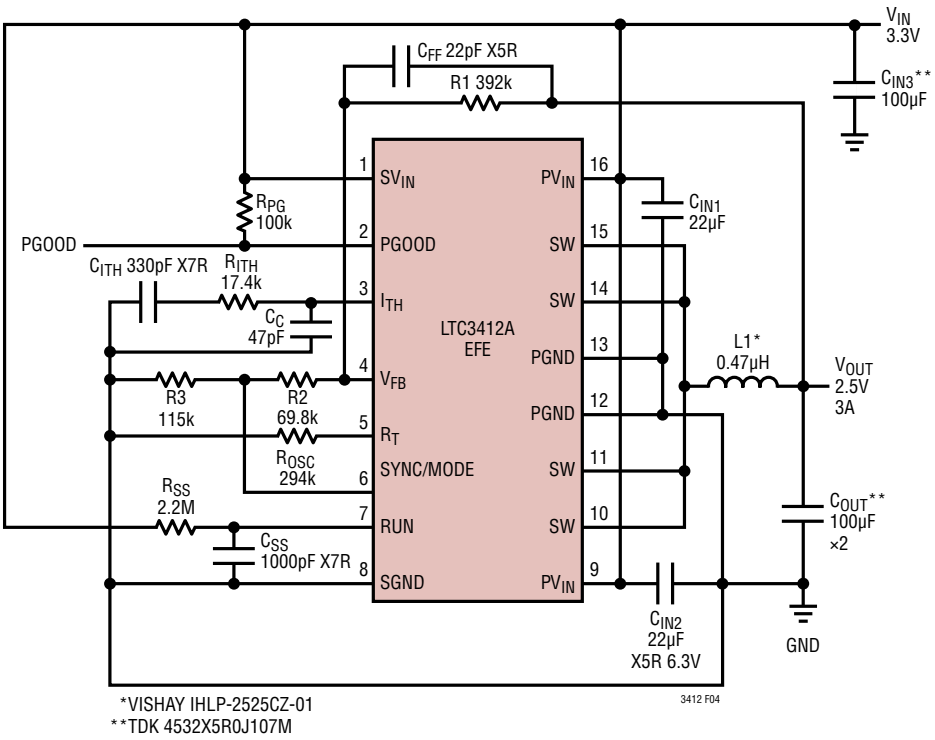
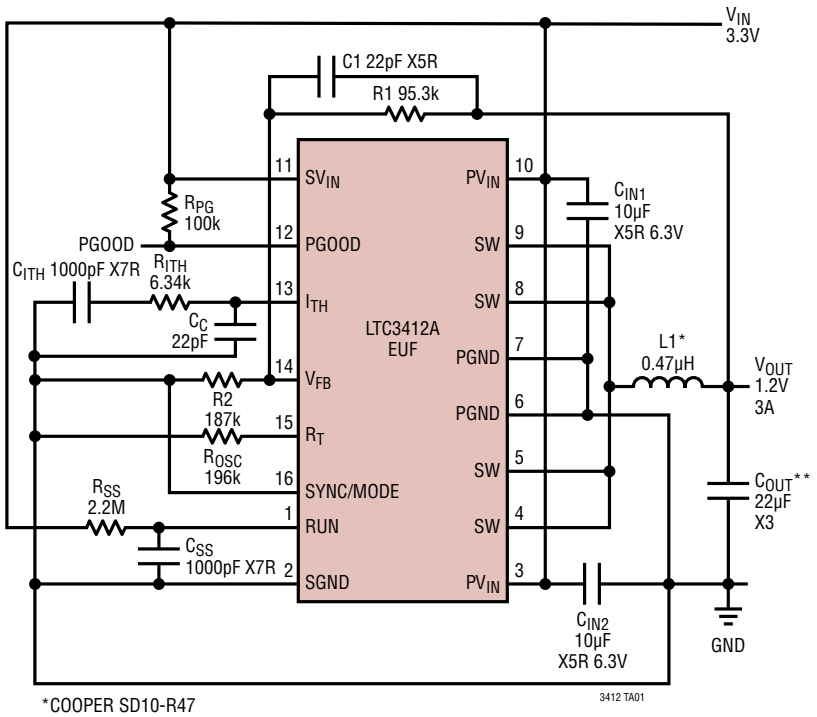



**Figure 4. 3.3V to 2.5V, 3A Regulator at 1MHz, Burst Mode Operation**

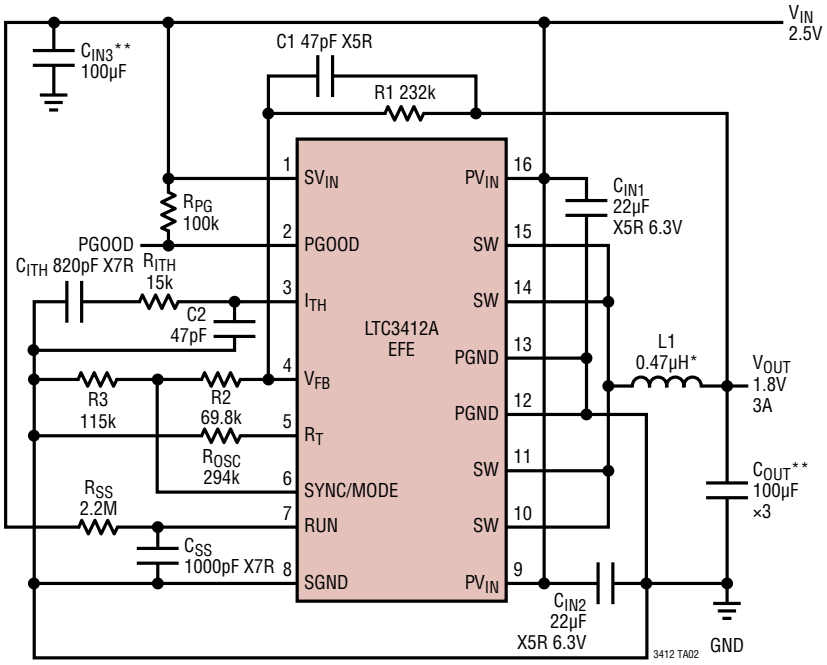
# TYPICAL APPLICATIONS

### 1.2V, 3A, 1.5MHz 1mm Height Regulator Using All Ceramic Capacitors




*COOPER SD10-R47
**TAIYO YUDEN AMK212BJ226MD-B

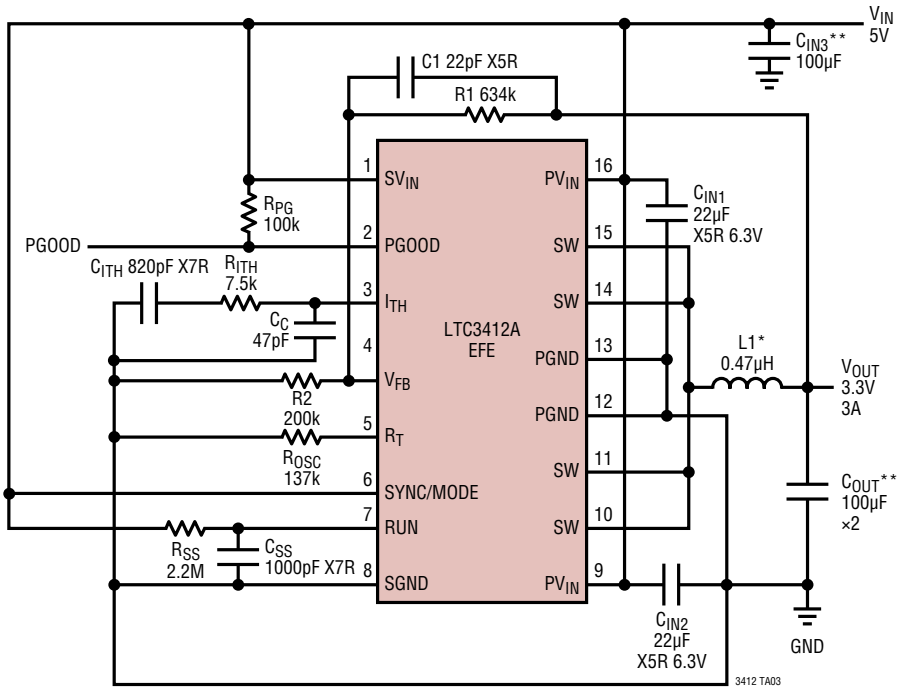
### 1.8V, 3A Step-Down Regulator at 1MHz, Burst Mode Operation




*VISHAY IHLP-2525CZ-01
**TDK C4532X5R0J107M

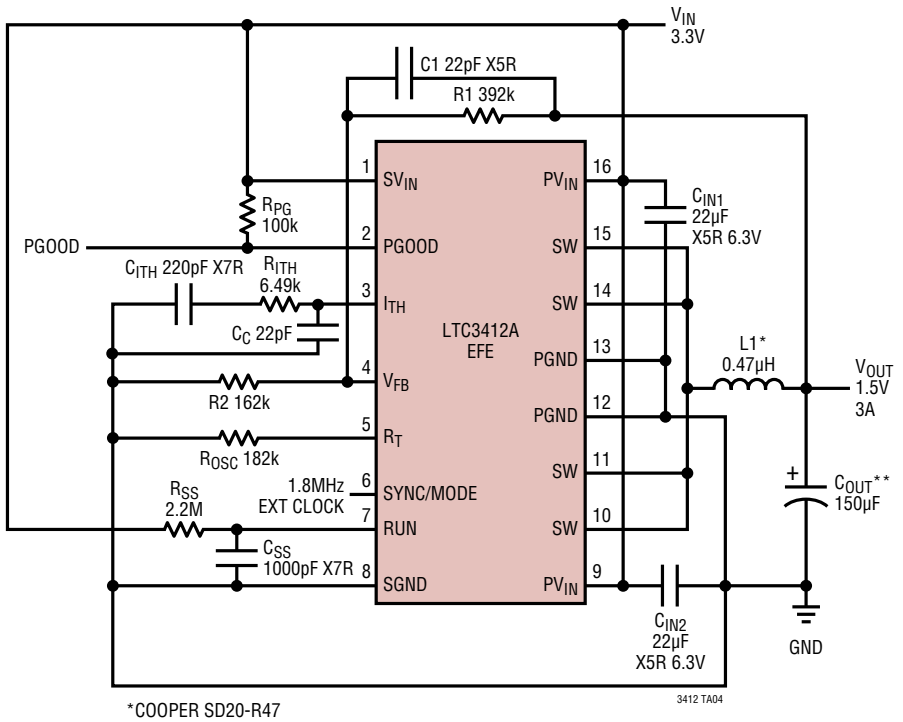
# TYPICAL APPLICATIONS

### 3.3V, 3A Step-Down Regulator at 2MHz, Forced Continuous Mode Operation




*VISHAY IHLP-2525CZ-01
**TDK C4532X5R0J107M

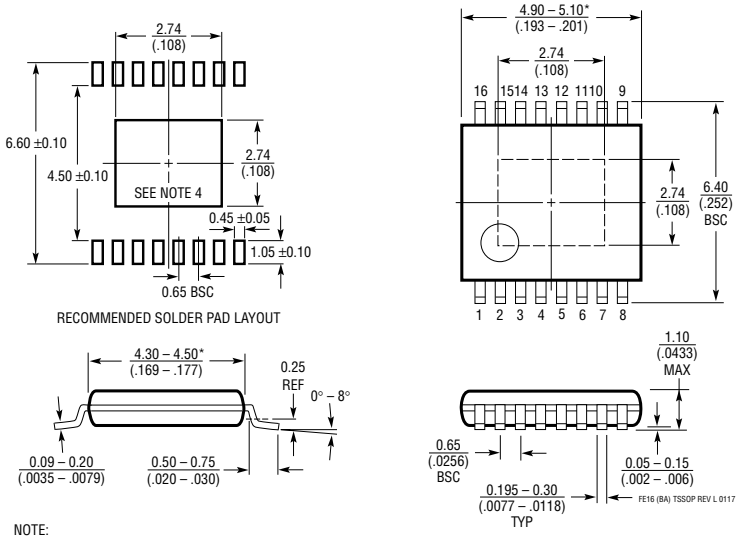
### 2.5V, 3A Step-Down Regulator Synchronized to 1.8MHz




*COOPER SD20-R47
**SANYO POSCAP 4TPE150MAZB

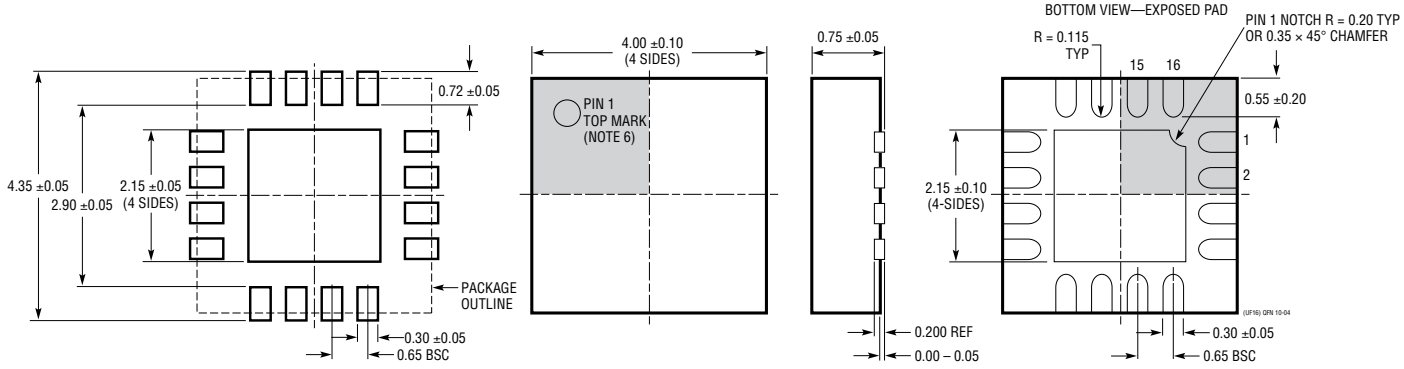
# PACKAGE DESCRIPTION

**FE Package**
**16-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1663 Rev L)
**Exposed Pad Variation BA**




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

**UF Package**
**16-Lead Plastic QFN (4mm × 4mm)**
(Reference LTC DWG # 05-08-1692 Rev Ø)




NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY (Revision history begins at Rev E)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| E | 03/10 | Changed Temperature Range for E- and I-Grades to –40°C to 125°C in Absolute Maximum Ratings and Order Information Sections | 2 |
| | | Changed from $T_A$ = 25°C to $T_A \approx T_J$ = 25°C in the Electrical Characteristics Heading | 3 |
| | | Updated Note 2 | 3 |
| F | 05/17 | Add Storage Temperature to Absolute Maximum Ratings | 2 |
| G | 02/21 | Added LTC3412AMPFE#PBF/TRPBF to Ordering Table | 2 |

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1878 | 600mA ($I_{OUT}$), 550kHz, Synchronous Step-Down DC/DC Converter | 96% Efficiency, $V_{IN}$: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 10µA $I_{SD}$ <1µA, MS8 Package |
| LTC1879 | 1.20A ($I_{OUT}$), 550kHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.7V to 10V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 15µA, $I_{SD}$ <1µA, TSSOP16 Package |
| LT1934/LT1934-1 | 300mA ($I_{OUT}$), Constant Off-Time, High Efficiency Step-Down DC/DC Converter | 90% Efficiency, $V_{IN}$: 3.2V to 34V, $V_{OUT(MIN)}$ = 1.25V, $I_Q$ = 14µA, $I_{SD}$ <1µA, ThinSOT™ Package |
| LTC3404 | 600mA ($I_{OUT}$), 1.4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.7V to 6V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 10µA, $I_{SD}$ <1µA, MS8 Package |
| LTC3405/LTC3405A | 300mA ($I_{OUT}$), 1.5MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 20µA, $I_{SD}$ <1µA, ThinSOT Package |
| LTC3406/LTC3406B | 600mA ($I_{OUT}$), 1.5MHz, Synchronous Step-Down DC/DC Converter | 96% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 20µA, $I_{SD}$ <1µA, ThinSOT Package |
| LTC3407 | Dual 600mA ($I_{OUT}$), 1.5MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ <1µA, MS10E and 3mm × 3mm DFN Packages |
| LTC3411 | 1.25A ($I_{OUT}$), 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60µA, $I_{SD}$ <1µA, MS10 and 3mm × 3mm DFN Packages |
| LTC3412 | 2.5A ($I_{OUT}$), 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 60µA, $I_{SD}$ <1µA, TSSOP16E Package |
| LTC3413 | 3A ($I_{OUT}$ Sink/Source), 2MHz, Monolithic Synchronous Regulator for DDR/QDR Memory Termination | 90% Efficiency, $V_{IN}$: 2.25V to 5.5V, $V_{OUT(MIN)}$ = $V_{REF/2}$, $I_Q$ = 280µA, $I_{SD}$ <1µA, TSSOP16E Package |
| LTC3414 | 4A ($I_{OUT}$), 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 64µA, $I_{SD}$ <1µA, TSSOP20E Package |
| LTC3416 | 4A ($I_{OUT}$), 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 64µA, $I_{SD}$ <1µA, TSSOP20E Package |
| LTC3418 | 8A ($I_{OUT}$), 4MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, $I_Q$ = 380µA, $I_{SD}$ <1µA, QFN Package |
| LT3430 | 60V, 2.75A ($I_{OUT}$), 200kHz, High Efficiency Step-Down DC/DC Converter | 90% Efficiency, $V_{IN}$: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, $I_Q$ = 2.5mA, $I_{SD}$ 25µA, TSSOP16E Package |
| LTC3440 | 600mA ($I_{OUT}$), 2MHz, Synchronous Buck-Boost DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT}$: 2.5V to 5.5V, $I_Q$ = 25µA, $I_{SD}$ <1µA, DFN Package |
| LTC3441 | 1.2A ($I_{OUT}$), 1MHz, Synchronous Buck-Boost DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.4V to 5.5V, $V_{OUT}$: 2.4V to 5.25V, $I_Q$ = 25µA, $I_{SD}$ <1µA, DFN Package |
| LTC3548 | 400mA/800mA Dual Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ <40µA, $I_{SD}$ <1µA, MS8E and DFN Packages |