

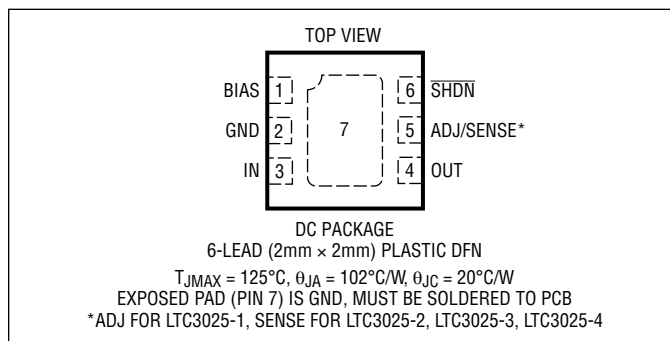
LTC3025-1/LTC3025-2/ LTC3025-3/LTC3025-4

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{BIAS} , V_{IN} to GND	–0.3V to 6V
SHDN to GND.....	–0.3V to 6V
SENSE, ADJ to GND.....	–0.3V to 6V
V_{OUT}	–0.3V to $V_{IN} + 0.3V$ or 6V
Operating Junction Temperature Range (Note 3).....	–40°C to 125°C
Storage Temperature Range	–65°C to 125°C
Output Short-Circuit Duration	Indefinite

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3025EDC-1#PBF	LTC3025EDC-1#TRPBF	LDDW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-1#PBF	LTC3025IDC-1#TRPBF	LDDW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025EDC-2#PBF	LTC3025EDC-2#TRPBF	LDMK	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-2#PBF	LTC3025IDC-2#TRPBF	LDMK	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025EDC-3#PBF	LTC3025EDC-3#TRPBF	LDQS	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-3#PBF	LTC3025IDC-3#TRPBF	LDQS	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025EDC-4#PBF	LTC3025EDC-4#TRPBF	LDPQ	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-4#PBF	LTC3025IDC-4#TRPBF	LDPQ	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3025EDC-1	LTC3025EDC-1#TR	LDDW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-1	LTC3025IDC-1#TR	LDDW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025EDC-2	LTC3025EDC-2#TR	LDMK	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-2	LTC3025IDC-2#TR	LDMK	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025EDC-3	LTC3025EDC-3#TR	LDQS	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-3	LTC3025IDC-3#TR	LDQS	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025EDC-4	LTC3025EDC-4#TR	LDPQ	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-4	LTC3025IDC-4#TR	LDPQ	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC3025EDC-1#WPBF	LTC3025EDC-1#WTRPBF	LDDW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3025IDC-1#WPBF	LTC3025IDC-1#WTRPBF	LDDW	6-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

****Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications.** These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

LTC3025-1/LTC3025-2/ LTC3025-3/LTC3025-4

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 1.5\text{V}$, $V_{BIAS} = 3.6\text{V}$, $C_{OUT} = 1\mu\text{F}$, $C_{IN} = 0.1\mu\text{F}$, $C_{BIAS} = 0.1\mu\text{F}$ (all capacitors ceramic) unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{IN} Operating Voltage (Note 4)	LTC3025-1	●	0.9		5.5	V
	LTC3025-2	●	1.4		5.5	V
	LTC3025-3	●	1.7		5.5	V
	LTC3025-4	●	2.0		5.5	V
V _{BIAS} Operating Voltage (Note 4)	LTC3025-1	●	2.5		5.5	V
	LTC3025-2	●	2.7		5.5	V
	LTC3025-3	●	3.0		5.5	V
	LTC3025-4	●	3.3		5.5	V
V _{BIAS} Undervoltage Lockout		●		2.2	2.5	V
V _{IN} Operating Current	I _{OUT} = 10μA, V _{OUT} = 1.2V, LTC3025-1	●		4	10	μA
V _{IN} Operating Current	I _{OUT} = 0μA, LTC3025-2/LTC3025-3/LTC3025-4	●		4	10	μA
V _{BIAS} Operating Current	I _{OUT} = 10μA, V _{OUT} = 1.2V, LTC3025-1	●		50	80	μA
V _{BIAS} Operating Current	I _{OUT} = 0μA, LTC3025-2/LTC3025-3/LTC3025-4	●		50	80	μA
V _{IN} Shutdown Current	V _{SHDN} = 0V			1	5	μA
V _{BIAS} Shutdown Current	V _{SHDN} = 0V			0.01	1	μA
V _{ADJ} Regulation Voltage (Note 5)	1mA ≤ I _{OUT} ≤ 500mA, V _{OUT} = 1.2V, 1.5V ≤ V _{IN} ≤ 5V, LTC3025-1 1mA ≤ I _{OUT} ≤ 500mA, V _{OUT} = 1.2V, 1.5V ≤ V _{IN} ≤ 5V, LTC3025-1	●	0.395	0.4	0.405	V
			0.392	0.4	0.408	V
V _{SENSE} Regulation Voltage (Note 5)	1mA ≤ I _{OUT} ≤ 500mA, 1.5V ≤ V _{IN} ≤ 5V, LTC3025-2 1mA ≤ I _{OUT} ≤ 500mA, 1.5V ≤ V _{IN} ≤ 5V, LTC3025-2	●	1.185	1.2	1.215	V
			1.176	1.2	1.224	V
V _{SENSE} Regulation Voltage (Note 5)	1mA ≤ I _{OUT} ≤ 500mA, 1.7V ≤ V _{IN} ≤ 5V, LTC3025-3 1mA ≤ I _{OUT} ≤ 500mA, 1.7V ≤ V _{IN} ≤ 5V, LTC3025-3	●	1.481	1.5	1.519	V
			1.470	1.5	1.530	V
V _{SENSE} Regulation Voltage (Note 5)	1mA ≤ I _{OUT} ≤ 500mA, 2.0V ≤ V _{IN} ≤ 5V, LTC3025-4 1mA ≤ I _{OUT} ≤ 500mA, 2.0V ≤ V _{IN} ≤ 5V, LTC3025-4	●	1.777	1.8	1.823	V
			1.764	1.8	1.836	V
I _{ADJ} ADJ Input Current	V _{ADJ} = 0.45V, LTC3025-1		−50	0	50	nA
OUT Load Regulation (Referred to ADJ Pin)	ΔI _{OUT} = 1mA to 500mA, LTC3025-1			−0.35		mV
OUT Load Regulation	ΔI _{OUT} = 1mA to 500mA, LTC3025-2			−1		mV
	ΔI _{OUT} = 1mA to 500mA, LTC3025-3			−1.3		mV
	ΔI _{OUT} = 1mA to 500mA, LTC3025-4			−1.5		mV
V _{IN} Line Regulation (Referred to ADJ Pin)	V _{IN} = 1.5V to 5V, V _{BIAS} = 3.6V, V _{OUT} = 1.2V, I _{OUT} = 1mA, LTC3025-1			0.07		mV
V _{IN} Line Regulation	V _{IN} = 1.5V to 5V, V _{BIAS} = 3.6V, I _{OUT} = 1mA, LTC3025-2			0.21		mV
	V _{IN} = 1.8V to 5V, V _{BIAS} = 3.6V, I _{OUT} = 1mA, LTC3025-3			0.26		mV
	V _{IN} = 2.1V to 5V, V _{BIAS} = 3.6V, I _{OUT} = 1mA, LTC3025-4			0.32		mV
V _{BIAS} Line Regulation	V _{IN} = 1.5V, V _{BIAS} = 2.7V to 5V, V _{OUT} = 1.2V, I _{OUT} = 1mA, LTC3025-1	●		4.5	16.5	mV
V _{BIAS} Line Regulation	V _{IN} = 1.5V, V _{BIAS} = 2.7V to 5V, I _{OUT} = 1mA, LTC3025-2	●		4.5	16.5	mV
	V _{IN} = 1.8V, V _{BIAS} = 3.0V to 5V, I _{OUT} = 1mA, LTC3025-3	●		4.5	16.5	mV
	V _{IN} = 2.1V, V _{BIAS} = 3.3V to 5V, I _{OUT} = 1mA, LTC3025-4	●		4.5	16.5	mV
V _{IN} to V _{OUT} Dropout Voltage (Notes 4, 6)	V _{BIAS} = 3V, V _{IN} = 1.5V, I _{OUT} = 500mA, V _{ADJ} = 0.37V(LTC3025-1), V _{SENSE} = 1.15V(LTC3025-2)	●		85	120	mV
					170	mV
V _{IN} to V _{OUT} Dropout Voltage (Notes 4, 6)	V _{BIAS} = 3.1V, V _{IN} = 1.7V, I _{OUT} = 500mA, V _{SENSE} = 1.45V(LTC3025-3)	●		90	130	mV
					185	mV

LTC3025-1/LTC3025-2/ LTC3025-3/LTC3025-4

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 1.5\text{V}$, $V_{BIAS} = 3.6\text{V}$, $C_{OUT} = 1\mu\text{F}$, $C_{IN} = 0.1\mu\text{F}$, $C_{BIAS} = 0.1\mu\text{F}$ (all capacitors ceramic) unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} to V_{OUT} Dropout Voltage (Notes 4, 6)	$V_{BIAS} = 3.4\text{V}$, $V_{IN} = 2.0\text{V}$, $I_{OUT} = 500\text{mA}$, $V_{SENSE} = 1.75\text{V}$ (LTC3025-4)	●	90	130 185	mV mV
V_{BIAS} to V_{OUT} Dropout Voltage (Note 4)	LTC3025-1	●		1.5	V
I_{OUT} Continuous Output Current		●	500		mA
I_{OUT} Current Limit	$V_{ADJ} = 0\text{V}$ (LTC3025-1), $V_{SENSE} = 0\text{V}$ (LTC3025-2/LTC3025-3/LTC3025-4)		1130		mA
e_n Output Voltage Noise	$f = 10\text{Hz}$ to 100kHz , $I_{OUT} = 300\text{mA}$		80		μV_{RMS}
V_{IH} $\overline{\text{SHDN}}$ Input High Voltage		●	0.9		V
V_{IL} $\overline{\text{SHDN}}$ Input Low Voltage		●		0.3	V
I_{IH} $\overline{\text{SHDN}}$ Input High Current	$\overline{\text{SHDN}} = 1.2\text{V}$		-1	1	μA
I_L $\overline{\text{SHDN}}$ Input Low Current	$\overline{\text{SHDN}} = 0\text{V}$		-1	1	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LTC3025-X regulators are tested and specified under pulse load conditions such that $T_J \approx T_A$. The LTC3025E-X are guaranteed to meet performance specifications from 0°C and 125°C . Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3025I-X are guaranteed to meet performance specifications over the full -40°C to 125°C operating junction temperature range.

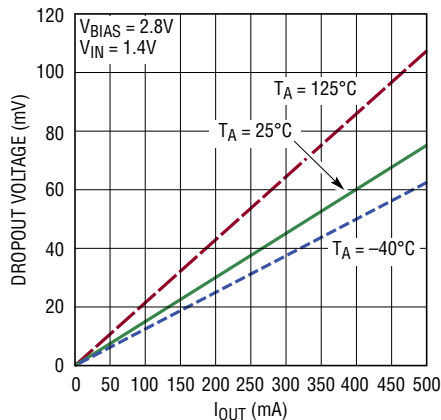
Note 4: For the LTC3025-1, a regulated output voltage will only be available when the minimum IN and BIAS operating voltages as well as the IN to OUT and BIAS to OUT dropout voltages are all satisfied. For the LTC3025-2/LTC3025-3/LTC3025-4 the minimum IN operating voltage assumes $I_{OUT} = 500\text{mA}$. For correct regulation at $I_{OUT} < 500\text{mA}$ the minimum IN operating voltage decreases to the maximum V_{SENSE} Regulation Voltage as I_{OUT} decreases to 0mA (i.e. $V_{IN\text{MIN}} = 1.312\text{V}$ at $I_{OUT} = 250\text{mA}$ for the LTC3025-2).

Note 5: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

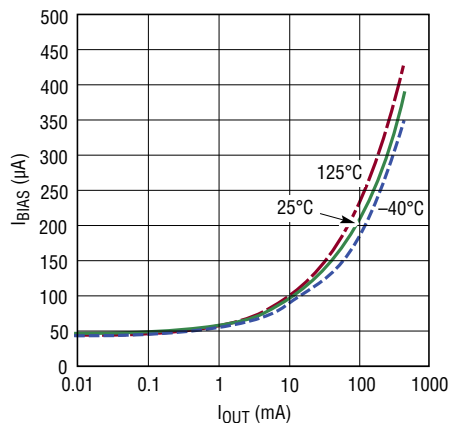
Note 6: Dropout voltage is minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to $V_{IN} - V_{\text{DROPOUT}}$.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

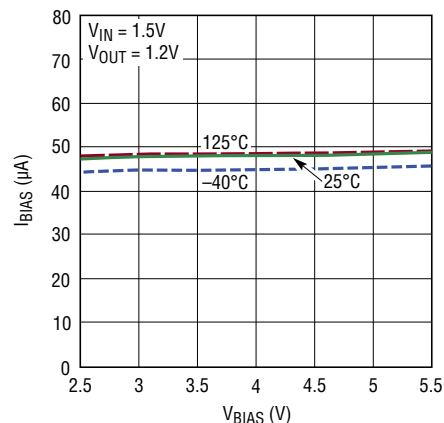
V_{IN} to V_{OUT} Dropout Voltage vs I_{OUT}



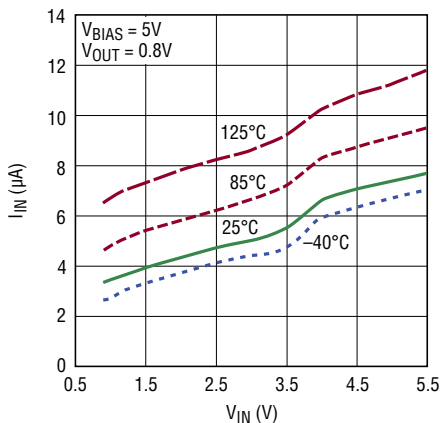
Operating BIAS Current vs Output Current



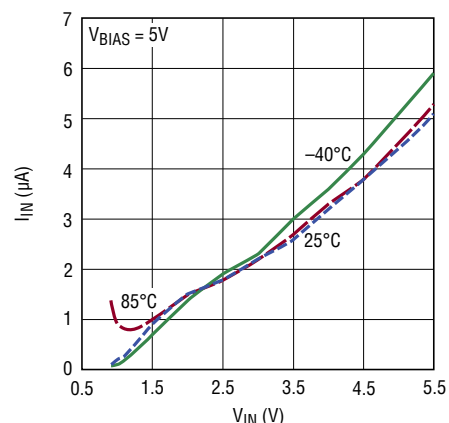
BIAS No Load Operating Current



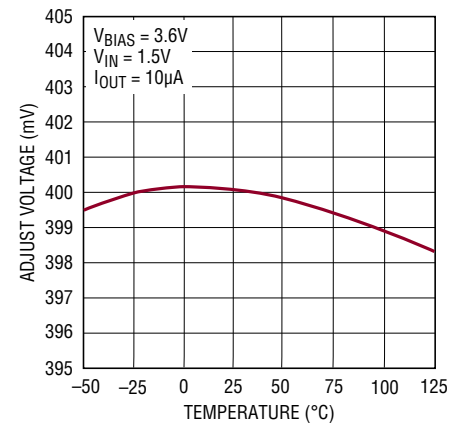
V_{IN} No Load Operating Current



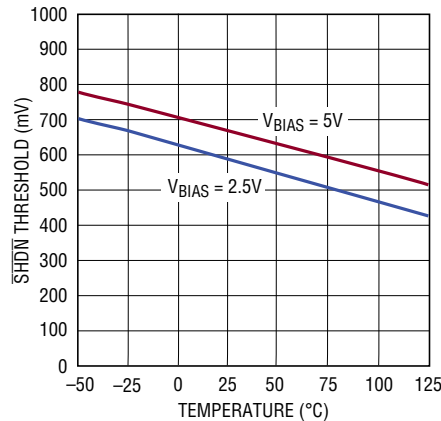
V_{IN} Shutdown Current



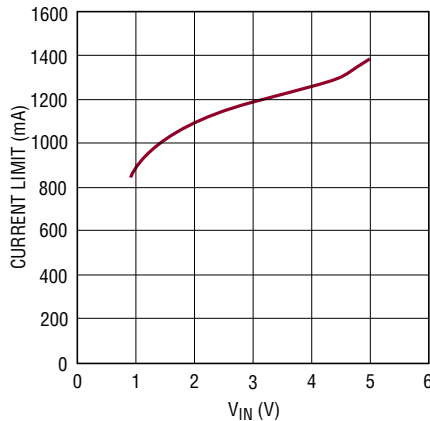
Adjust Voltage vs Temperature



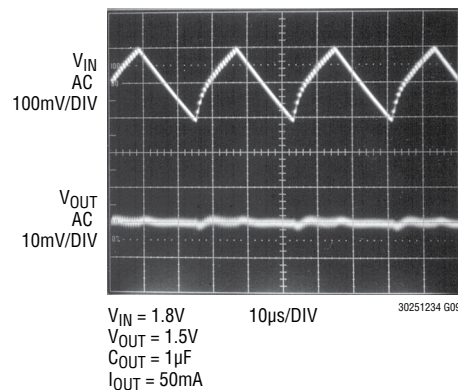
SHDN Threshold vs Temperature



Current Limit vs V_{IN} Voltage

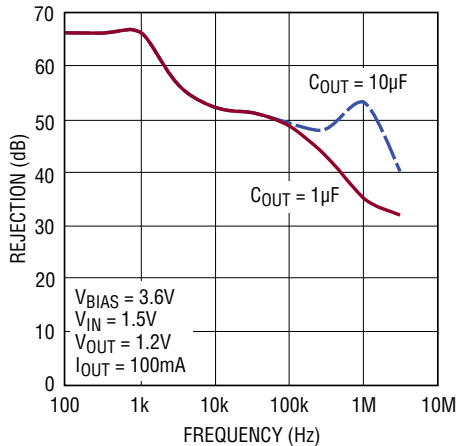


Burst Mode DC/DC Buck Ripple Rejection

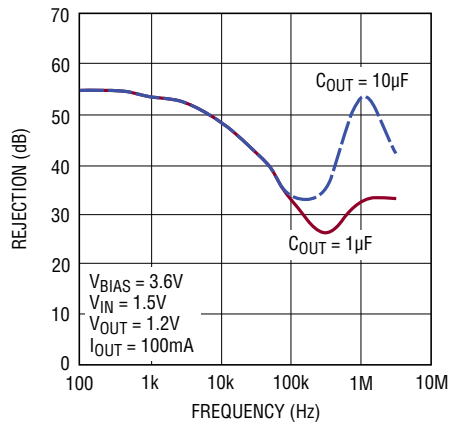


TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

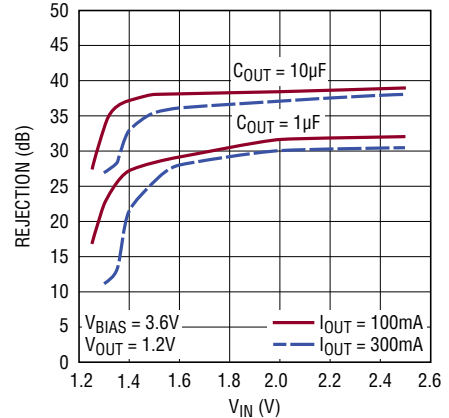
**V_{IN} Ripple Rejection
vs Frequency**



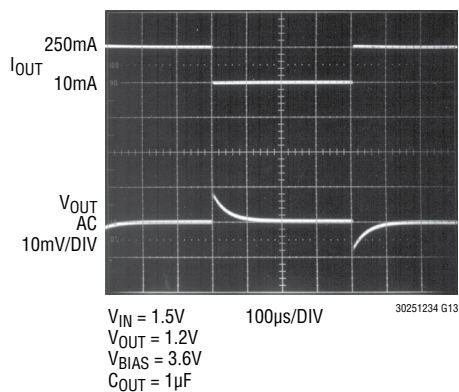
**BIAS Ripple Rejection
vs Frequency**



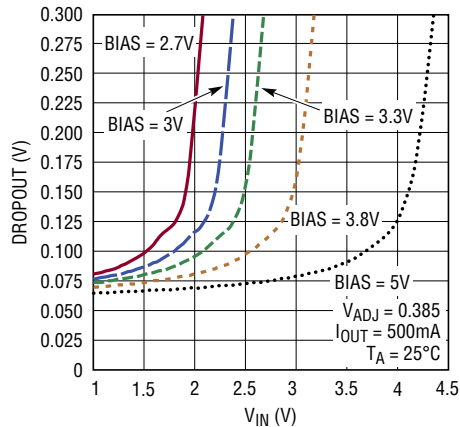
3MHz V_{IN} Supply Rejection



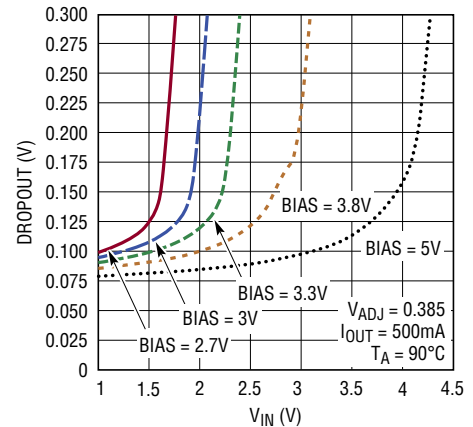
Transient Response



**V_{IN} to V_{OUT} Dropout Voltage
vs V_{IN} (25°C) LTC3025-1**



**V_{IN} to V_{OUT} Dropout Voltage
vs V_{IN} (90°C) LTC3025-1**



PIN FUNCTIONS

BIAS (Pin 1): BIAS Input Voltage. BIAS provides internal power for LTC3025-X circuitry. The BIAS pin should be locally bypassed to ground if the LTC3025-X is more than a few inches away from another source of bulk capacitance. In general, the output impedance of a battery rises with frequency, so it is usually advisable to include an input bypass capacitor in battery-powered circuits. A capacitor in the range of 0.01 μ F to 0.1 μ F is usually sufficient.

GND (Pin 2): Ground. Connect to a ground plane.

IN (Pin 3): Input Supply Voltage. The output load current is supplied directly from IN. The IN pin should be locally bypassed to ground if the LTC3025-X is more than a few inches away from another source of bulk capacitance. In general, the output impedance of a battery rises with frequency, so it is usually advisable to include an input bypass capacitor when supplying IN from a battery. A capacitor in the range of 0.1 μ F to 1 μ F is usually sufficient.

OUT (Pin 4): Regulated Output Voltage. The OUT pin supplies power to the load. A minimum ceramic output capacitor of at least 1 μ F is required to ensure stability. Larger output capacitors may be required for applications with large transient loads to limit peak voltage transients.

See the Applications Information section for more information on output capacitance.

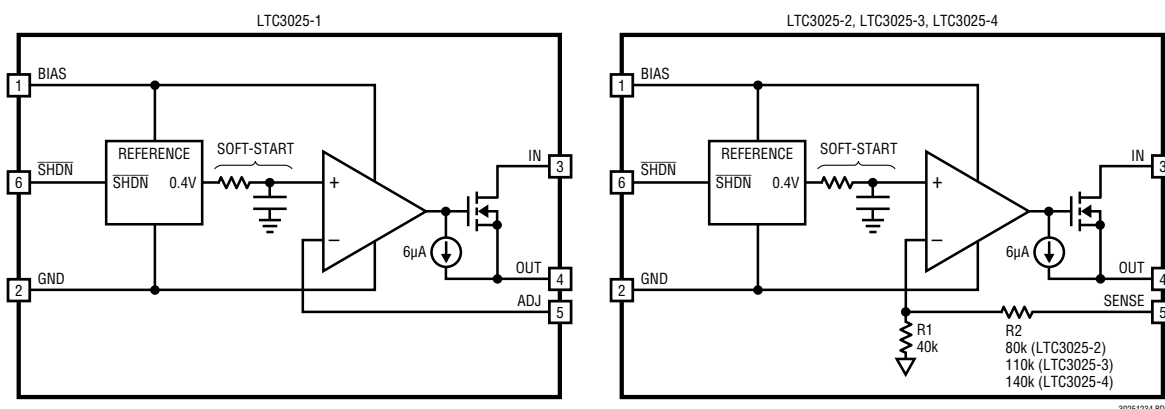
ADJ (Pin 5) LTC3025-1: Adjust Input. This is the input to the error amplifier. The ADJ pin reference voltage is 0.4V referenced to ground. The output voltage range is 0.4V to 3.6V and is typically set by connecting ADJ to a resistor divider from OUT to GND. See Figure 2.

SENSE (Pin 5) LTC3025-2, LTC3025-3, LTC3025-4: Output Sense. The sense is the input to the resistor divider driving the error amplifier. Optimum regulation will be obtained at the point where SENSE is connected to OUT. The SENSE pin bias current is 10 μ A at the nominal rated output voltage.

SHDN (Pin 6): Shutdown Input, Active Low. This pin is used to put the LTC3025-X into shutdown. The SHDN pin current is typically less than 10nA. The SHDN pin cannot be left floating and must be tied to a valid logic level (such as BIAS) if not used.

GND (Exposed Pad Pin 7): Ground and Heat Sink. Must be soldered to PCB ground plane or large pad for optimal thermal performance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Operation (Refer to Block Diagram)

The LTC3025-X is a micropower, VLDO (very low dropout) linear regulator which operates from input voltages as low as 0.9V. The device provides a highly accurate output that is capable of supplying 500mA of output current with a typical dropout voltage of only 85mV. A single ceramic capacitor as small as 1 μ F is all that is required for output bypassing. A low reference voltage allows the LTC3025-1 output to be programmed to much lower voltages than available in common LDOs (range of 0.4V to 3.6V). The LTC3025-2/LTC3025-3/LTC3025-4 have fixed outputs of 1.2V, 1.5V and 1.8V respectively, eliminating the need for an external resistor divider.

As shown in the Block Diagram, the BIAS input supplies the internal reference and LDO circuitry while all output current comes directly from the IN input for high efficiency regulation. The low quiescent supply currents $I_{IN} = 4\mu$ A, $I_{BIAS} = 50\mu$ A drop to $I_{IN} = 1\mu$ A, $I_{BIAS} = 0.01\mu$ A typical in shutdown making the LTC3025-X an ideal choice for use in battery-powered systems.

The device includes current limit and thermal overload protection. The fast transient response of the follower output stage overcomes the traditional trade off between dropout voltage, quiescent current and load transient response inherent in most LDO regulator architectures. The LTC3025-X also includes overshoot detection circuitry which brings the output back into regulation when going from heavy to light output loads (see Figure 1).

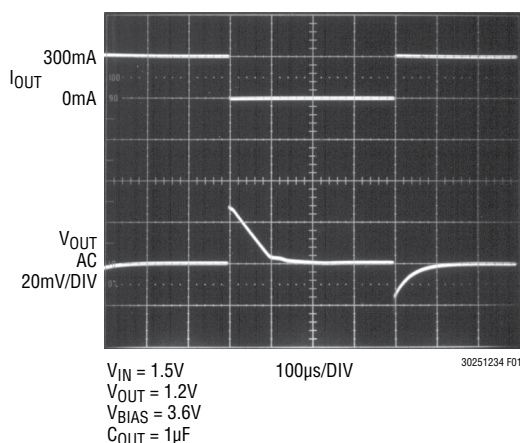


Figure 1. LTC3025-X Transient Response

Adjustable Output Voltage (LTC3025-1)

The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output to maintain the ADJ pin voltage at 0.4V (referenced to ground). Thus, the current in R1 is equal to $0.4V/R1$. For good transient response, stability, and accuracy, the current in R1 should be at least 8 μ A, thus the value of R1 should be no greater than 50k. The current in R2 is the current in R1 plus the ADJ pin bias current. Since the ADJ pin bias current is typically <10nA, it can be ignored in the output voltage calculation. The output voltage can be calculated using the formula in Figure 2. Note that in shutdown the output is turned off and the divider current will be zero once C_{OUT} is discharged.

The LTC3025-1 operates at a relatively high gain of -0.7μ V/mA referred to the ADJ input. Thus a load current change of 1mA to 500mA produces a -0.35 mV drop at the ADJ input. To calculate the change referred to the output simply multiply by the gain of the feedback network (i. e., $1 + R2/R1$). For example, to program the output for 1.2V choose $R2/R1 = 2$. In this example, an output current change of 1mA to 500mA produces $-0.35\text{mV} \cdot (1 + 2) = 1.05\text{mV}$ drop at the output.

Because the ADJ pin is relatively high impedance (depending on the resistor divider used), stray capacitance at this pin should be minimized (<10pF) to prevent phase shift in the error amplifier loop. Additionally, special attention should be given to any stray capacitances that can couple external signals onto the ADJ pin producing undesirable output ripple. For optimum performance connect the ADJ pin to R1 and R2 with a short PCB trace and minimize all other stray capacitance to the ADJ pin.

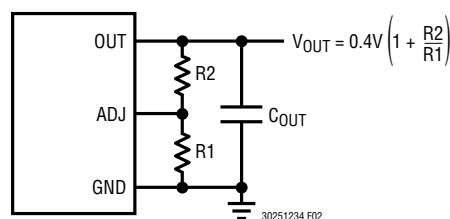


Figure 2. Programming the LTC3025-1

APPLICATIONS INFORMATION

Output Capacitance and Transient Response

The LTC3025-X is designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of $1\mu\text{F}$ with an ESR of 0.05Ω or less is recommended to ensure stability. The LTC3025-X is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Note that bypass capacitors used to decouple individual components powered by the LTC3025-X will increase the effective output capacitor value. High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic capacitor must be in parallel at the output. There is no minimum ESR or maximum capacitor size requirements.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit large voltage and temperature coefficients as shown in Figure 3 and Figure 4. When used with a 2V regulator, a $1\mu\text{F}$ Y5V capacitor can lose as much as 75% of its initial capacitance over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are usually more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. In all cases,

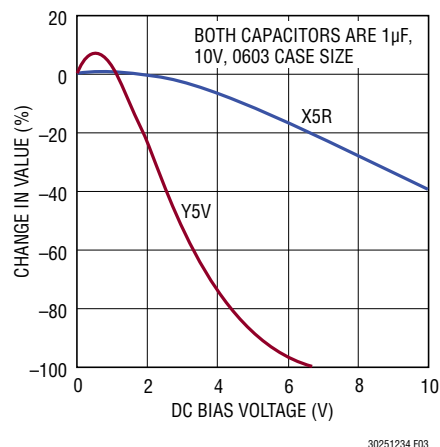


Figure 3. Ceramic Capacitor DC Bias Characteristics

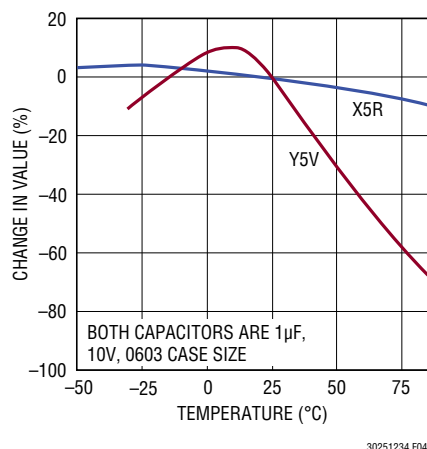


Figure 4. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

the output capacitance should never drop below 0.4 μ F, or instability or degraded performance may occur.

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be the output current multiplied by the input/output voltage differential:

$$(I_{OUT})(V_{IN} - V_{OUT})$$

Note that the BIAS current is less than 500 μ A even under heavy loads, so its power consumption can be ignored for thermal calculations.

The LTC3025-X has internal thermal limiting designed to protect the device during momentary overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered. For surface mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

The LTC3025-X 2mm $\times$ 2mm DFN package is specified as having a junction-to-ambient thermal resistance of 102°C/W, which assumes a minimal heat spreading copper plane. The actual thermal resistance can be reduced substantially by connecting the package directly to a good heat spreading ground plane. When soldered to 2500mm² double-sided 1 oz. copper plane, the actual junction-to-ambient thermal resistance can be less than 60°C/W.

Calculating Junction Temperature

Example: Given an output voltage of 1.2V, an input voltage of 1.8V to 3V, an output current range of 0mA to 100mA

and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT})$$

where:

$$I_{OUT(MAX)} = 100\text{mA}$$

$$V_{IN(MAX)} = 3\text{V}$$

So:

$$P = 100\text{mA}(3\text{V} - 1.2\text{V}) = 0.18\text{W}$$

Even under worst-case conditions, the LTC3025-X's BIAS pin power dissipation is only about 1mW, thus can be ignored. Assuming a junction-to-ambient thermal resistance of 102°C/W, the junction temperature rise above ambient will be approximately equal to:

$$0.18\text{W}(102^\circ\text{C/W}) = 18.4^\circ\text{C}$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_J = 50^\circ\text{C} + 18.4^\circ\text{C} = 68.4^\circ\text{C}$$

Short-Circuit/Thermal Protection

The LTC3025-X has built-in short-circuit current limiting as well as overtemperature protection. During short-circuit conditions, internal circuitry automatically limits the output current to approximately 1130mA. At higher temperatures, or in cases where internal power dissipation causes excessive self heating on chip, the thermal shutdown circuitry will shut down the LDO when the junction temperature exceeds approximately 150°C. It will re enable the LDO once the junction temperature drops back to approximately 140°C. The LTC3025-X will cycle in and out of thermal shutdown without latch-up or damage until the overstress condition is removed. Long

APPLICATIONS INFORMATION

term overstress ($T_J > 125^\circ\text{C}$) should be avoided as it can degrade the performance or shorten the life of the part.

Soft-Start Operation

The LTC3025-X includes a soft-start feature to prevent excessive current flow during start-up. When the LDO is enabled, the soft-start circuitry gradually increases the LDO reference voltage from 0V to 0.4V over a period of about 600 μs . There is a short 700 μs delay from the

time the part is enabled until the LDO output starts to rise. Figure 5 shows the start-up and shutdown output waveform.

V_{OUT} Start-Up and Supply Sequencing

During power-up, the output shutdown circuitry is not active below V_{IN} of about 0.65V DC (typical). As a result, the output voltage can drift up during power-up due to leakage current ($<1\text{ mA}$ typical) from V_{IN} to V_{OUT} . At 0.9V input, the shutdown circuitry is active and the output is actively held off. This usually causes no circuit problems and is similar to 3-terminal regulators such as the LT3080, LT1086 and LT317 which have no ground pin and can have the output rise under some conditions. A slowly rising V_{IN} with the part enabled may result in non-monotonic ramping of V_{OUT} due to LDO circuitry becoming active at V_{IN} of about 0.65V (typical) as well.

With fast rising inputs ($>1\text{V/ms}$) or with sufficient resistive load on V_{OUT} , output voltage rise during power-up is reduced or eliminated. Such conditions also reduce or eliminate non-monotonic initial power-up with the part enabled. If V_{BIAS} is sequenced up before V_{IN} , the leakage current from V_{IN} to V_{OUT} may increase until the shutdown circuitry is active at a V_{IN} of about 0.65V typical. Thus, to minimize V_{OUT} rise during start-up, sequence up V_{IN} before V_{BIAS} . At $V_{IN} = 0.9\text{V}$, the output is actively held off in shutdown or it is actively held on when enabled under all conditions.

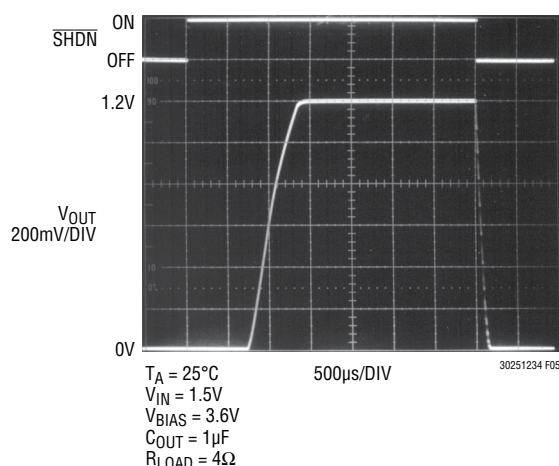
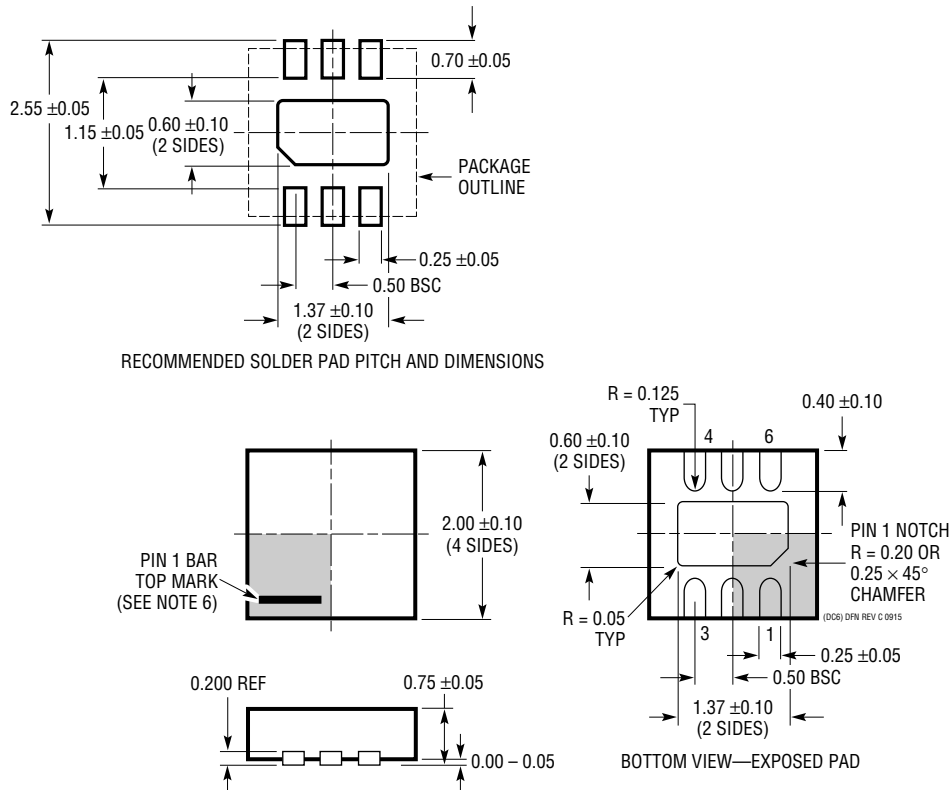


Figure 5. Output Start-Up and Shutdown

PACKAGE DESCRIPTION

DC6 Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703 Rev C)



NOTE:

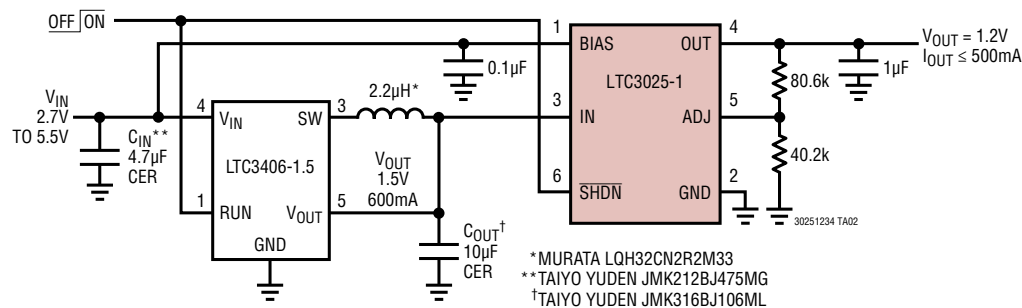
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev E)

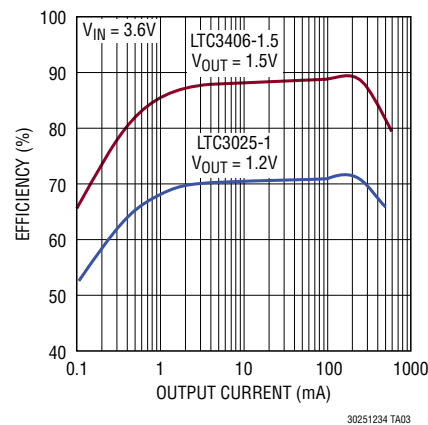
REV	DATE	DESCRIPTION	PAGE NUMBER
E	07/10	Added (Note 3) notation to “The ● denotes” statement in Electrical Characteristics section.	3, 4
		Updated Pin 7 in Pin Functions.	7
		Added “V _{OUT} Start-Up and Supply Sequencing” section.	11
		Updated Related Parts section.	14
F	04/11	Updated y-axis on graphs G14 and G15.	6
G	09/21	Added AEC-Q100 Qualification in Progress.	1
		Added “AUTOMOTIVE PRODUCTS**” table plus supplemental text.	2

TYPICAL APPLICATION

High Efficiency 1.5V Step-Down Converter with Efficient 1.2V VLDO Output



Efficiency vs Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1761	100mA, Low Noise Micropower, LDO	V _{IN} : 1.8V to 20V, V _{OUT(MIN)} = 1.22V, V _{DO} = 0.30V, I _Q = 20µA, I _{SD} < 1µA, V _{OUT} = Adj, 1.5V, 1.8V, 2V, 2.5V, 2.8V, 3V, 3.3V, 5V, ThinSOT™ Package. Low Noise < 20µV _{RMS} -P, Stable with 1µF Ceramic Capacitors
LT1762	150mA, Low Noise Micropower LDO	V _{IN} : 1.8V to 20V, V _{OUT(MIN)} = 1.22V, V _{DO} = 0.30V, I _Q = 25µA, I _{SD} < 1µA, V _{OUT} = Adj, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µV _{RMS} -P
LTC1844	150mA, Very Low Dropout LDO	V _{IN} : 1.6V to 6.5V, V _{OUT(MIN)} = 1.25V, V _{DO} = 0.08V, I _Q = 40µA, I _{SD} < 1µA, V _{OUT} = Adj, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V, ThinSOT Package. Low Noise < 30µV _{RMS} -P, Stable with 1µF Ceramic Capacitors
LT1962	300mA, Low Noise Micropower LDO	V _{IN} : 1.8V to 20V, V _{OUT(MIN)} = 1.22V, V _{DO} = 0.27V, I _Q = 30µA, I _{SD} < 1µA, V _{OUT} = 1.5, 1.8V, 2.5V, 3V, 3.3V, 5V, MS8 Package. Low Noise < 20µV _{RMS} -P
LT1964	200mA, Low Noise Micropower, Negative LDO	V _{IN} : -0.9V to -20V, V _{OUT(MIN)} = -1.21V, V _{DO} = 0.34V, I _Q = 30µA, I _{SD} < 3µA, V _{OUT} = Adj, -5V, ThinSOT Package. Low Noise < 30µV _{RMS} -P, Stable with Ceramic Capacitors
LT3020	100mA, Low Voltage, VLDO	V _{IN} : 0.9V to 10V, V _{OUT(MIN)} = 0.20V, V _{DO} = 0.15V, I _Q = 120µA, I _{SD} < 3µA, V _{OUT} = Adj, DFN, MS8 Package
LTC3025	300mA Micropower VLDO Linear Regulator	45mV Dropout Voltage, Low Noise: 80µV _{RMS} , V _{IN} : 0.9V to 5.5V, Low I _Q = 54µA, 2mm × 2mm 6-Lead DFN Package
LTC3026	1.5A, Low Input Voltage VLDO Regulator	V _{IN} : 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (with External 5V Rail), V _{DO} = 0.1V, I _Q = 950µA, Stable with 10µF Ceramic Capacitors, DFN-10 and MSOP-10 Packages

Rev. G