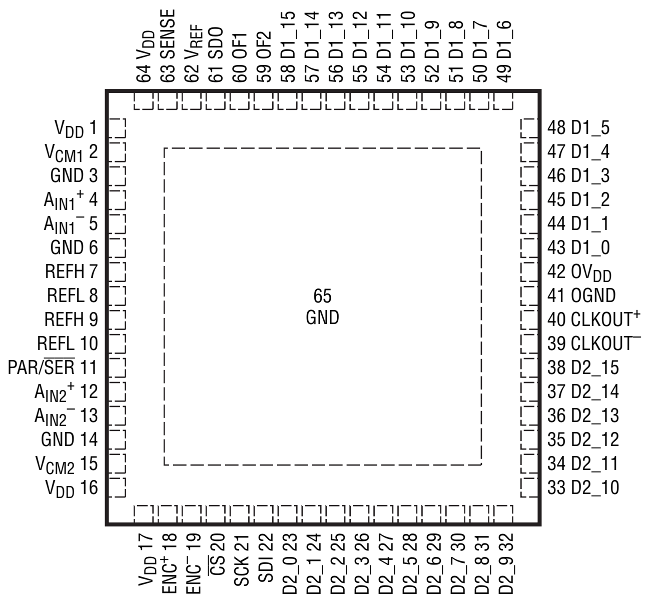
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages (V_{DD}, OV_{DD})	–0.3V to 2V
Analog Input Voltage (A_{IN}^+, A_{IN}^-, PAR/$\overline{SER}$, SENSE) (Note 3)	–0.3V to (V_{DD} + 0.2V)
Digital Input Voltage (ENC^+, ENC^-, $\overline{CS}$, SDI, SCK) (Note 4)	–0.3V to 3.9V
SDO (Note 4)	–0.3V to 3.9V
Digital Output Voltage	–0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range	
LTC2185C, 2184C, 2183C	0°C to 70°C
LTC2185I, 2184I, 2183I	–40°C to 85°C
Storage Temperature Range	–65°C to 150°C

PIN CONFIGURATIONS

FULL-RATE CMOS OUTPUT MODE

TOP VIEW

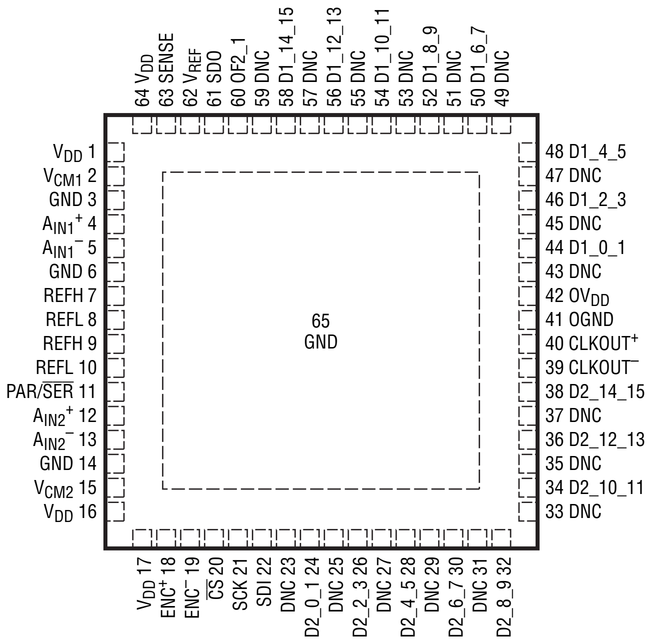


UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 20°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

DOUBLE DATA RATE CMOS OUTPUT MODE

TOP VIEW

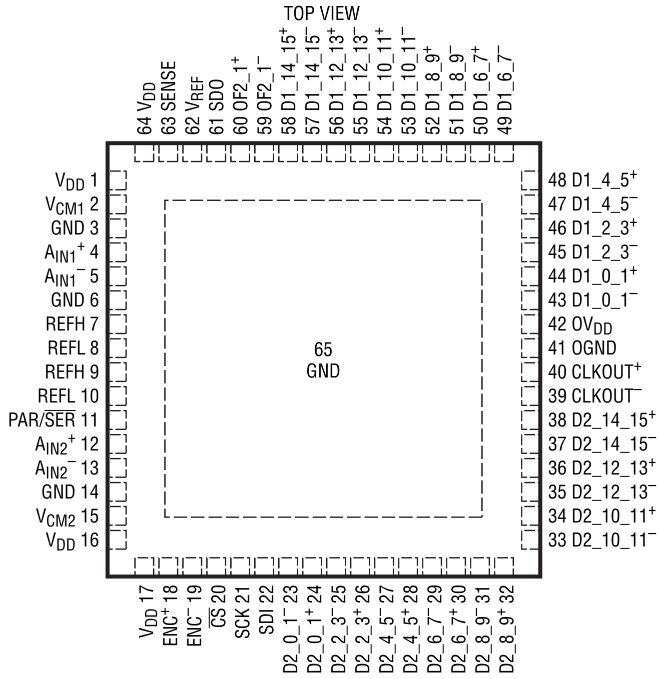


UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 20°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

PIN CONFIGURATIONS

DOUBLE DATA RATE LVDS OUTPUT MODE



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

$T_{JMAX} = 150°C$, $\theta_{JA} = 20°C/W$
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2185CUP#PBF	LTC2185CUP#TRPBF	LTC2185UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2185IUP#PBF	LTC2185IUP#TRPBF	LTC2185UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C
LTC2184CUP#PBF	LTC2184CUP#TRPBF	LTC2184UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2184IUP#PBF	LTC2184IUP#TRPBF	LTC2184UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C
LTC2183CUP#PBF	LTC2183CUP#TRPBF	LTC2183UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2183IUP#PBF	LTC2183IUP#TRPBF	LTC2183UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

PARAMETER	CONDITIONS		LTC2185			LTC2184			LTC2183			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution (No Missing Codes)		●	16			16			16			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–7.5	±2	7.5	–7.5	±2	7.5	–7.5	±2	7.5	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.5	0.9	–0.9	±0.5	0.9	–0.9	±0.5	0.9	LSB
Offset Error	(Note 7)	●	–7	±1.5	7	–7	±1.5	7	–7	±1.5	7	mV
Gain Error	Internal Reference			±1.5			±1.5			±1.5		%FS
	External Reference	●	–2.3	–0.9	0.3	–2.1	–0.8	0.4	–1.8	–0.5	0.8	%FS
Offset Drift				±10			±10			±10		µV/°C
Full-Scale Drift	Internal Reference			±30			±30			±30		ppm/°C
	External Reference			±10			±10			±10		ppm/°C
Gain Matching				±0.3			±0.3			±0.3		%FS
Offset Matching				±1.5			±1.5			±1.5		mV
Transition Noise				3.4			3.5			3.2		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ – A_{IN}^–$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^–$)/2	Differential Analog Input (Note 8)	●	0.7	V_{CM}	1.25	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 125Msps			200		µA
		Per Pin, 105Msps			170		µA
		Per Pin, 80Msps			130		µA
I_{IN1}	Analog Input Leakage Current (No Encode)	0 < A_{IN}^+, $A_{IN}^–$ < V_{DD}	●	–1.5		1.5	µA
I_{IN2}	PAR/$\overline{\text{SER}}$ Input Leakage Current	0 < PAR/$\overline{\text{SER}}$ < V_{DD}	●	–3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625 < SENSE < 1.3V	●	–3		3	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter	Single-Ended Encode			0.07		ps_{RMS}
		Differential Encode			0.09		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full-Power Bandwidth	Figure 6 Test Circuit			550		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

				LTC2185			LTC2184			LTC2183			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
SNR	Signal-to-Noise Ratio	5MHz Input			76.8			76.7			77.1		dBFS
		70MHz Input	●	74.8	76.6		74.8	76.5		75.1	76.9		dBFS
		140MHz Input			76.1			76			76.4		dBFS
SFDR	Spurious Free Dynamic Range 2nd Harmonic	5MHz Input			90			90			90		dBFS
		70MHz Input	●	79	89		81	89		81	89		dBFS
		140MHz Input			84			84			84		dBFS
	Spurious Free Dynamic Range 3rd Harmonic	5MHz Input			90			90			90		dBFS
		70MHz Input	●	82	89		81	89		82	89		dBFS
		140MHz Input			84			84			84		dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input			95			95			95		dBFS
		70MHz Input	●	89	95		89	95		89	95		dBFS
		140MHz Input			95			95			95		dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input			76.6			76.5			76.9		dBFS
		70MHz Input	●	73.3	76.2		73.9	76.1		74.4	76.5		dBFS
		140MHz Input			75.1			75			75.3		dBFS
	Crosstalk	10MHz Input			–110			–110			–110		dBc

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{CM} Output Voltage	$I_{OUT} = 0$		$0.5 \cdot V_{DD} - 25mV$	$0.5 \cdot V_{DD}$	$0.5 \cdot V_{DD} + 25mV$	V
V_{CM} Output Temperature Drift				±25		ppm/°C
V_{CM} Output Resistance	$-600\mu A < I_{OUT} < 1mA$			4		Ω
V_{REF} Output Voltage	$I_{OUT} = 0$		1.225	1.250	1.275	V
V_{REF} Output Temperature Drift				±25		ppm/°C
V_{REF} Output Resistance	$-400\mu A < I_{OUT} < 1mA$			7		Ω
V_{REF} Line Regulation	$1.7V < V_{DD} < 1.9V$			0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC$^+$, ENC$^–$)							
Differential Encode Mode (ENC$^–$ Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2 	 1.6	V V
V_{IN}	Input Voltage Range	ENC$^+$, ENC$^–$ to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 10)			10		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF
Single-Ended Encode Mode (ENC$^–$ Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
V_{IN}	Input Voltage Range	ENC$^+$ to GND	●	0		3.6	V
R_{IN}	Input Resistance	(See Figure 11)			30		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 8)			3		pF
SDO OUTPUT (Serial Programming Mode. Open-Drain Output. Requires 2kΩ Pull-Up Resistor if SDO is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance	(Note 8)			3		pF
DIGITAL DATA OUTPUTS (CMOS MODES: FULL DATA RATE AND DOUBLE DATA RATE)							
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –500µA	●	1.750	1.790		V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●		0.010	0.050	V
OV_{DD} = 1.5V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.488		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.010		V
OV_{DD} = 1.2V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.185		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.010		V
DIGITAL DATA OUTPUTS (LVDS MODE)							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● 	247 	350 175	454 	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	● 	1.125 	1.250 1.250	1.375 	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTC2185			LTC2184			LTC2183			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CMOS Output Modes: Full Data Rate and Double Data Rate													
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.1	1.8	1.9	1.1	1.8	1.9	1.1	1.8	1.9	V
I_{VDD}	Analog Supply Current	DC Input Sine Wave Input	●		206 209	228		171 173	188		111 113	124	mA mA
I_{OVDD}	Digital Supply Current	Sine Wave Input, OV_{DD} = 1.2V			10			8			6		mA
P_{DISS}	Power Dissipation	DC Input Sine Wave Input, OV_{DD} = 1.2V	●		370 388	410		308 321	339		200 211	223	mW mW
LVDS Output Mode													
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{VDD}	Analog Supply Current	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	 ●		211 213	 233		175 177	 193		115 117	 128	mA mA
I_{OVDD}	Digital Supply Current (OV_{DD} = 1.8V)	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	 ●		40 76	 86		40 75	 85		39 75	 84	mA mA
P_{DISS}	Power Dissipation	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	 ●		452 520	 574		387 454	 500		277 346	 382	mW mW
All Output Modes													
P_{SLEEP}	Sleep Mode Power				1			1			1		mW
P_{NAP}	Nap Mode Power				16			16			16		mW
$P_{DIFFCLK}$	Power Increase with Differential Encode Mode Enabled (No increase for Nap or Sleep Modes)				20			20			20		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2185			LTC2184			LTC2183			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_S	Sampling Frequency	(Note 10)	●	1		125	1		105	1		80	MHz
t_L	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	500 500	4.52 2	4.76 4.76	500 500	5.93 2	6.25 6.25	500 500	ns ns
t_H	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	500 500	4.52 2	4.76 4.76	500 500	5.93 2	6.25 6.25	500 500	ns ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (CMOS Modes: Full Data Rate and Double Data Rate)							
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.1	1.7	3.1	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1	1.4	2.6	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency	Full Data Rate Mode Double Data Rate Mode			6 6.5		Cycles Cycles

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (LVDS Mode)							
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.1	1.8	3.2	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1	1.5	2.7	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D – t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency				6.5		Cycles
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: $V_{DD} = OV_{DD}$ = 1.8V, f_{SAMPLE} = 125MHz (LTC2185), 105MHz (LTC2184), or 80MHz (LTC2183), LVDS outputs, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2's complement output mode.

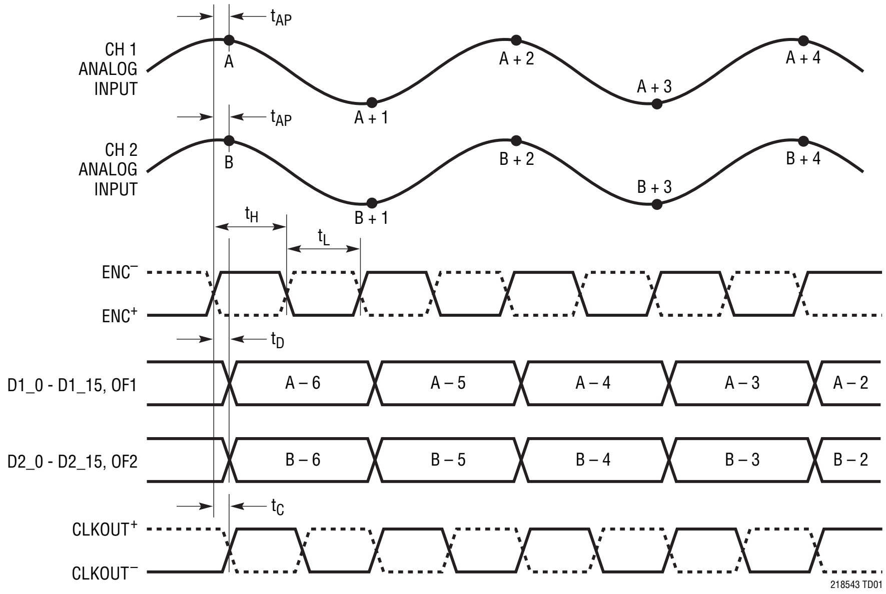
Note 8: Guaranteed by design, not subject to test.

Note 9: V_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTC2185), 105MHz (LTC2184), or 80MHz (LTC2183), CMOS outputs, ENC^+ = single-ended 1.8V square wave, ENC^- = 0V, input range = $2V_{P-P}$ with differential drive, 5pF load on each digital output unless otherwise noted. The supply current and power dissipation specifications are totals for the entire IC, not per channel.

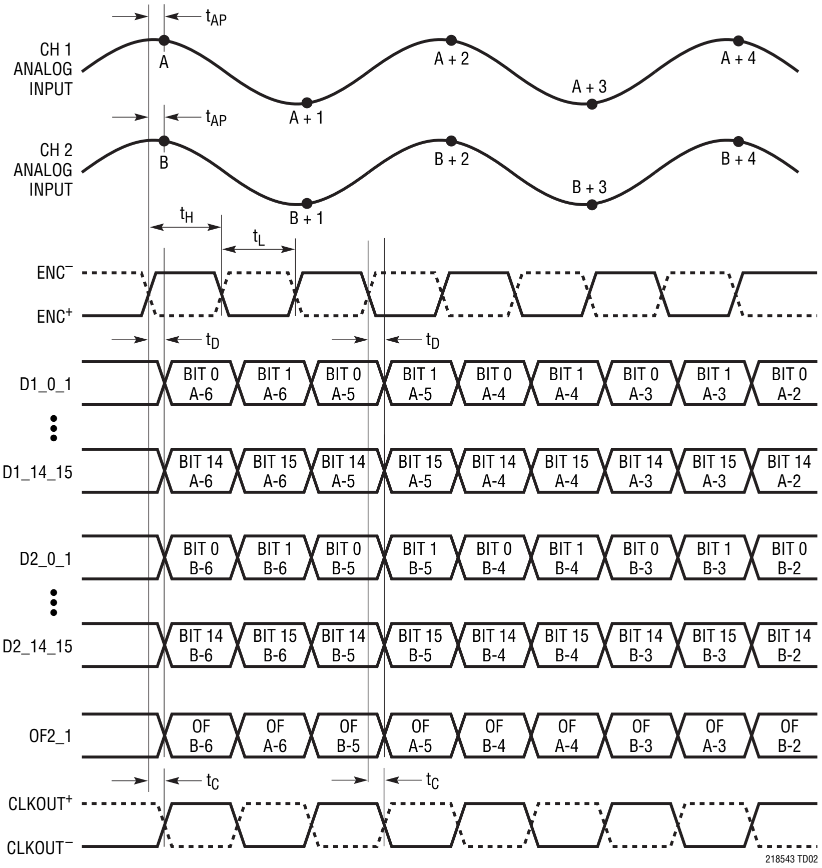
Note 10: Recommended operating conditions.

TIMING DIAGRAMS

Full-Rate CMOS Output Mode Timing
All Outputs Are Single-Ended and Have CMOS Levels

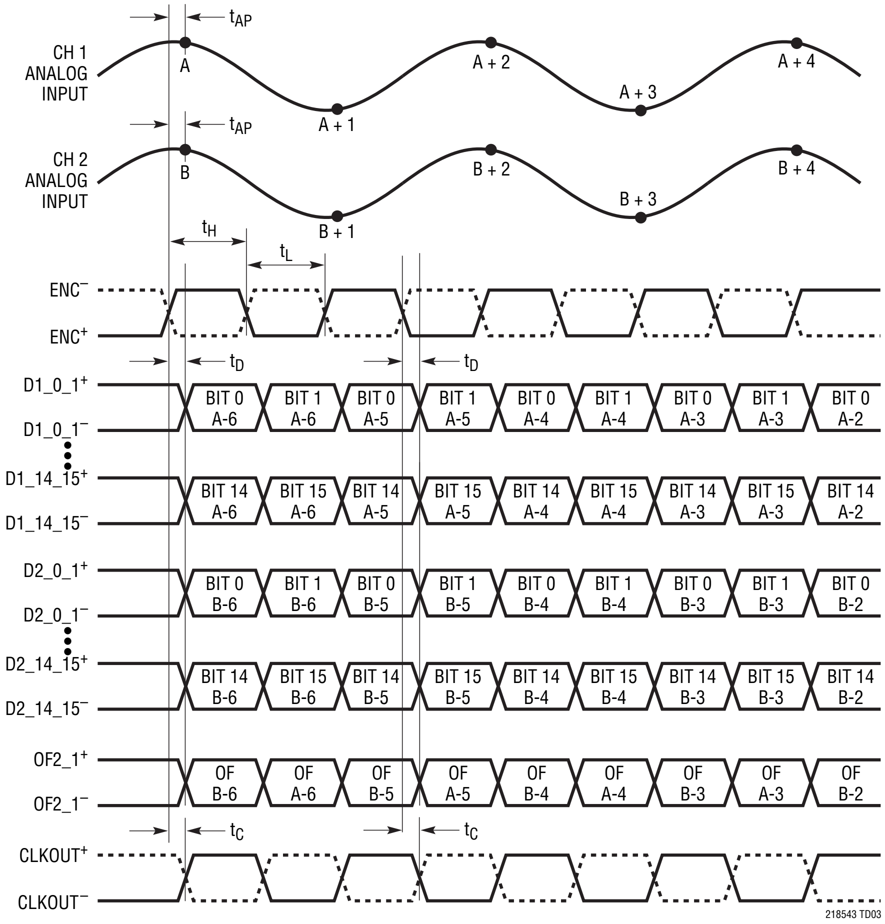


Double Data Rate CMOS Output Mode Timing
All Outputs Are Single-Ended and Have CMOS Levels

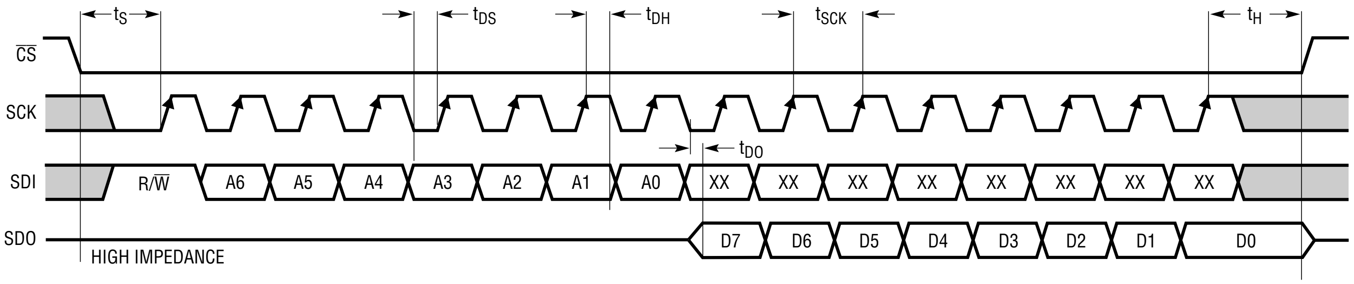


TIMING DIAGRAMS

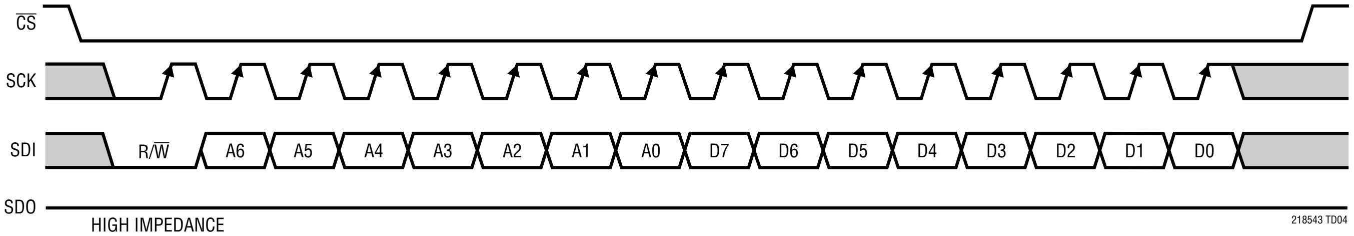
Double Data Rate LVDS Output Mode Timing
All Outputs Are Differential and Have LVDS Levels



SPI Port Timing (Readback Mode)

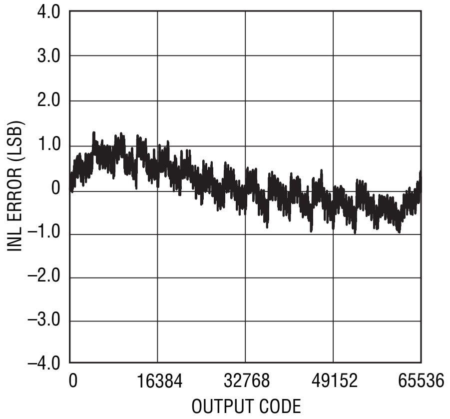


SPI Port Timing (Write Mode)



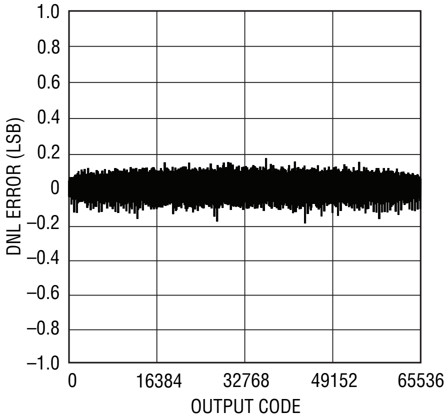
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2185: Integral Non-Linearity (INL)



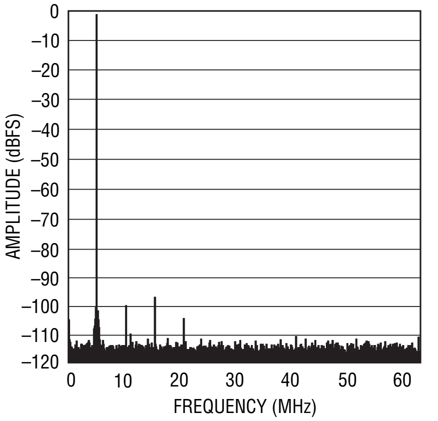
218543 G01

LTC2185: Differential Non-Linearity (DNL)



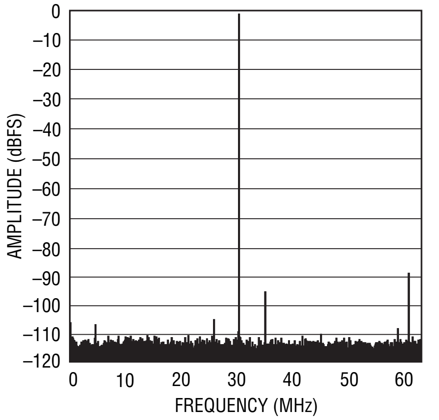
218543 G02

LTC2185: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 125Msps



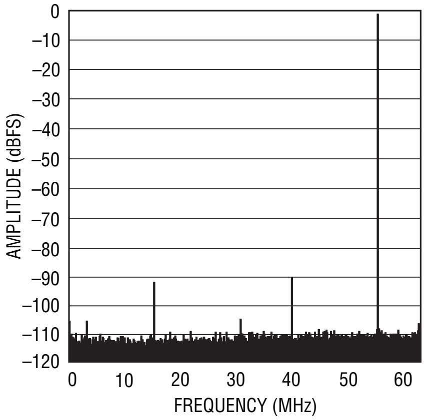
218543 G03

LTC2185: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 125Msps



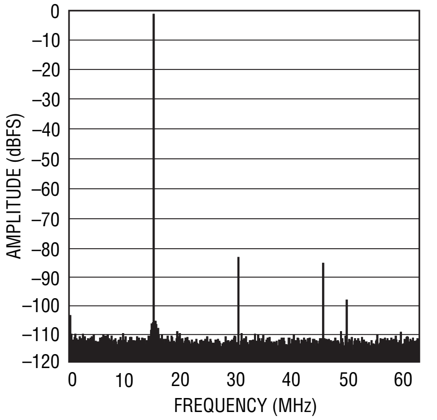
218543 G04

LTC2185: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 125Msps



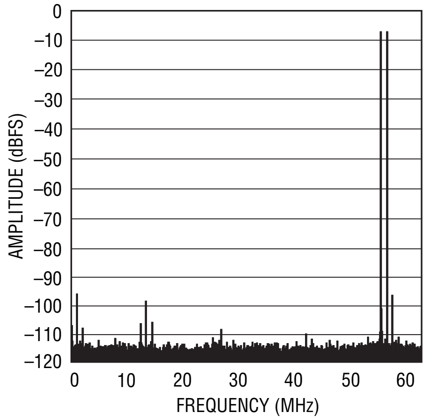
218543 G05

LTC2185: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 125Msps



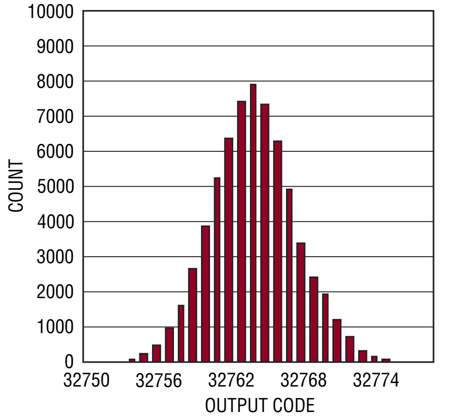
218543 G06

LTC2185: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 125Msps



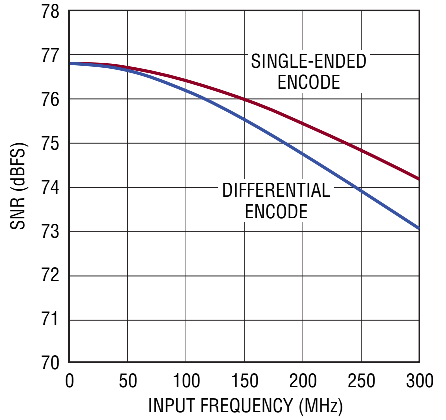
218543 G07

LTC2185: Shorted Input Histogram



218543 G08

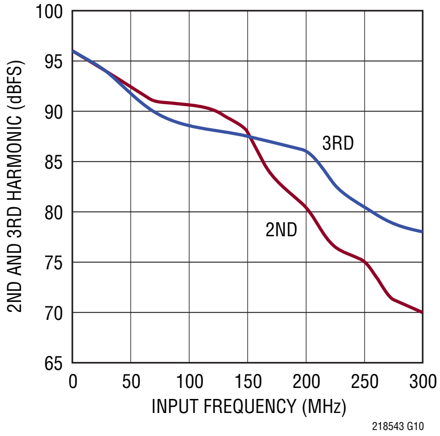
LTC2185: SNR vs Input Frequency, –1dBFS, 125Msps, 2V Range



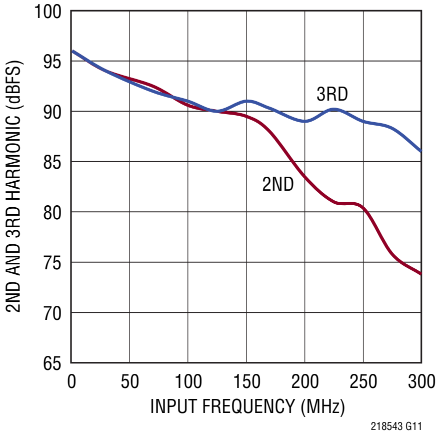
218543 G09

TYPICAL PERFORMANCE CHARACTERISTICS

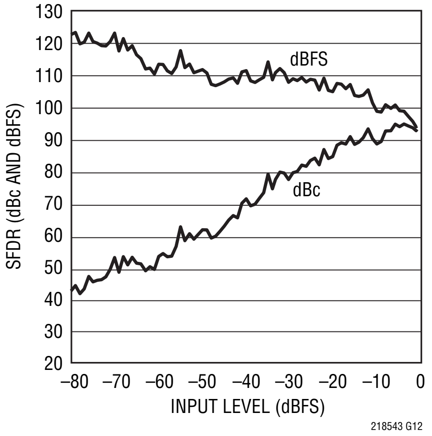
LTC2185: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 125Msps, 2V Range



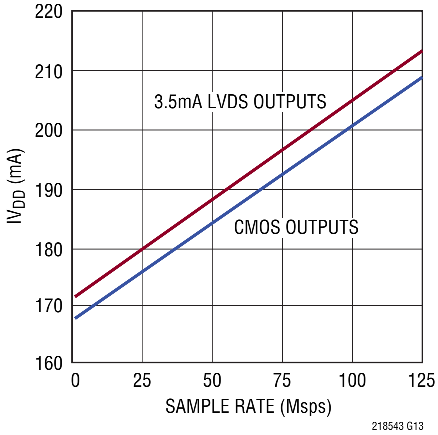
LTC2185: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 125Msps, 1V Range



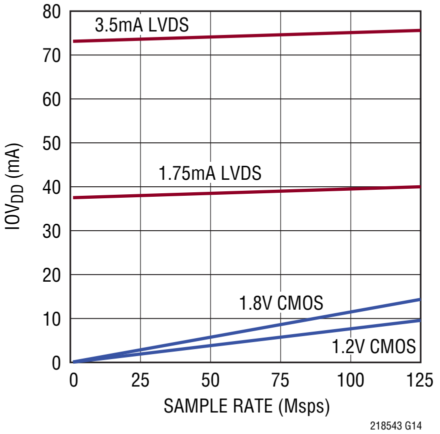
LTC2185: SFDR vs Input Level, f_{IN} = 70MHz, 125Msps, 2V Range



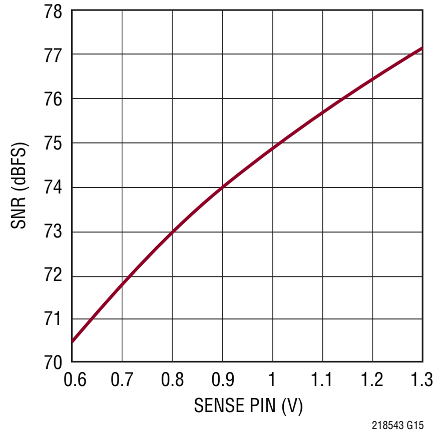
LTC2185: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input on Each Channel



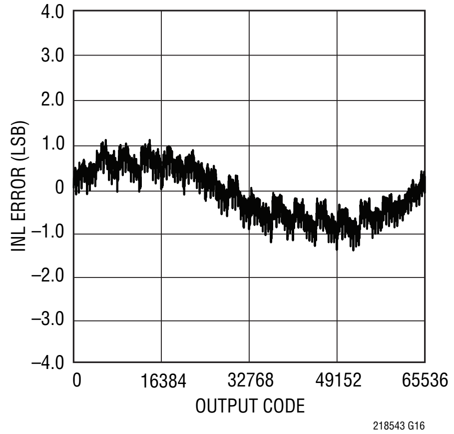
LTC2185: IO_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input on Each Channel



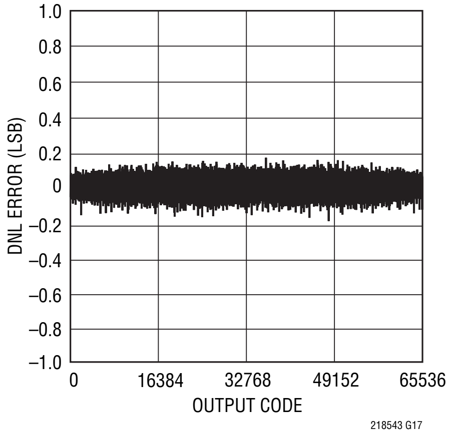
LTC2185: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



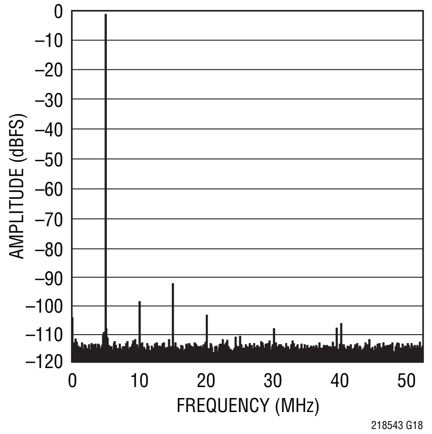
LTC2184: Integral Non-Linearity (INL)



LTC2184: Differential Non-Linearity (DNL)

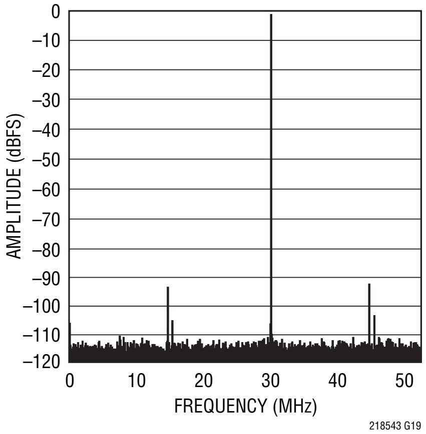


LTC2184: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 105Msps

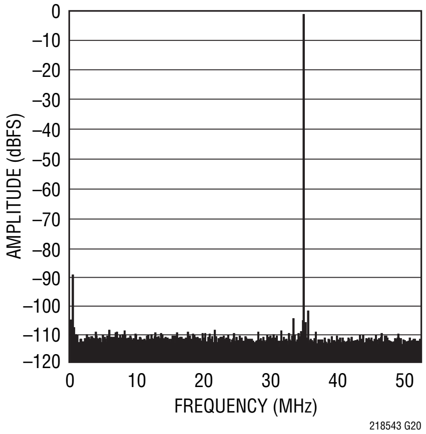


TYPICAL PERFORMANCE CHARACTERISTICS

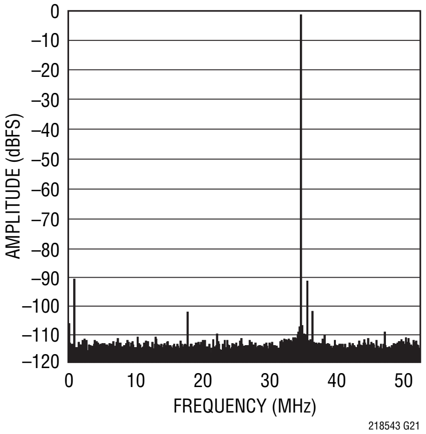
LTC2184: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 105Msps



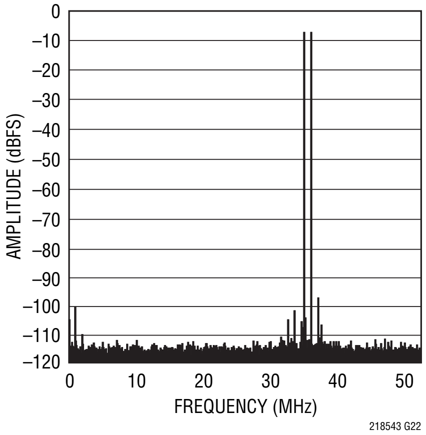
LTC2184: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 105Msps



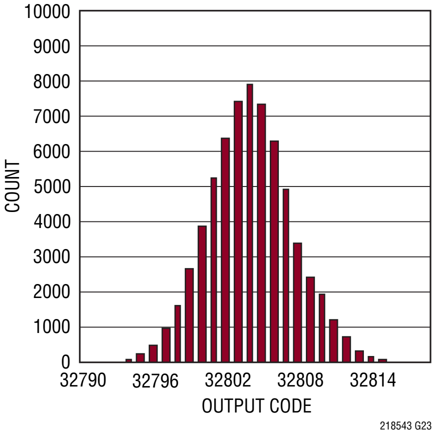
LTC2184: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 105Msps



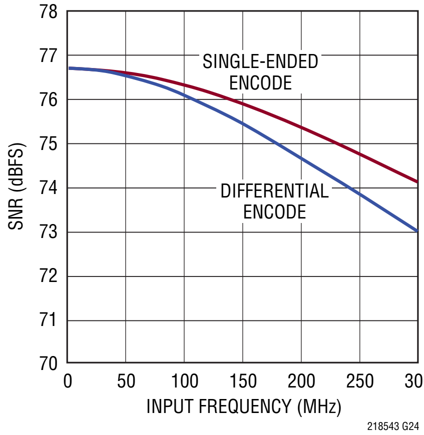
LTC2184: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 105Msps



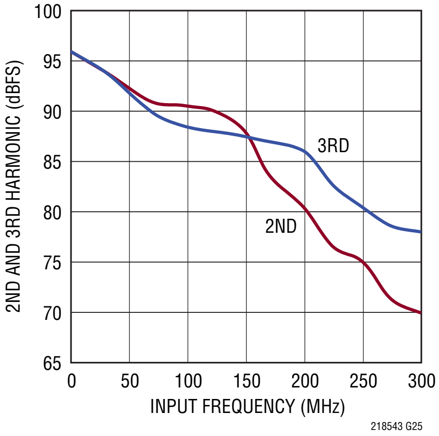
LTC2184: Shorted Input Histogram



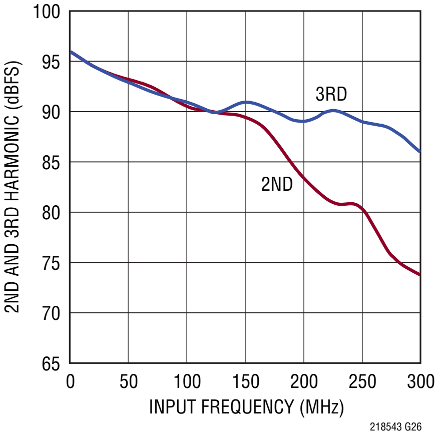
LTC2184: SNR vs Input Frequency, –1dBFS, 105Msps, 2V Range



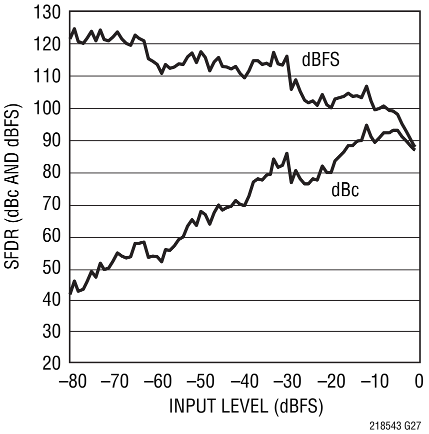
LTC2184: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 105Msps, 2V Range



LTC2184: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 105Msps, 1V Range

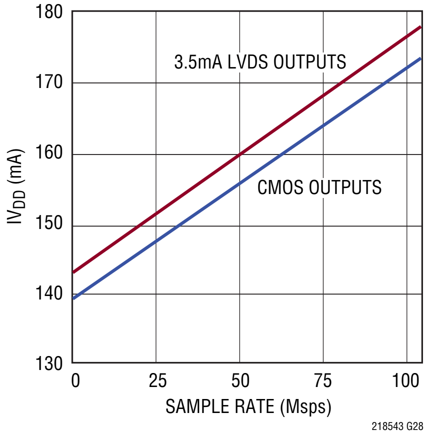


LTC2184: SFDR vs Input Level, f_{IN} = 70MHz, 105Msps, 2V Range

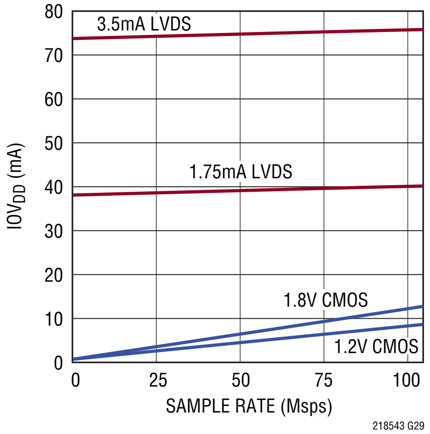


TYPICAL PERFORMANCE CHARACTERISTICS

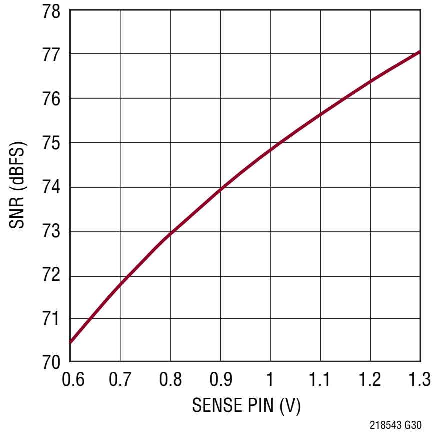
LTC2184: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input on Each Channel



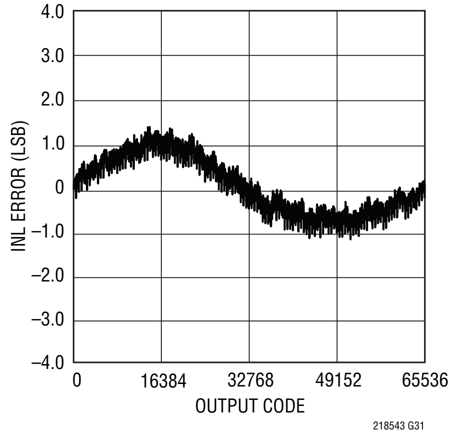
LTC2184: IO_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input on Each Channel



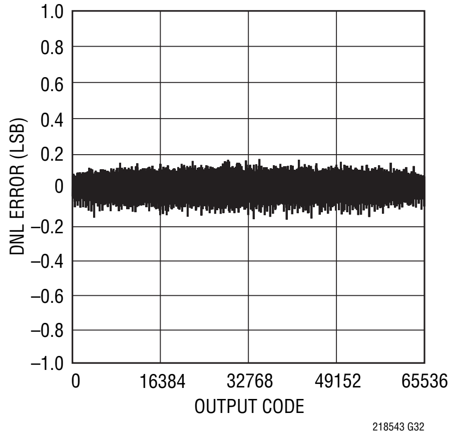
LTC2184: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



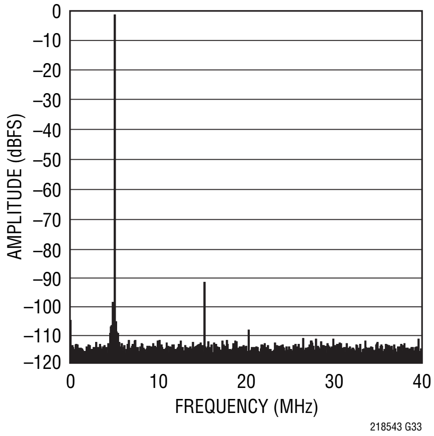
LTC2183: Integral Non-Linearity (INL)



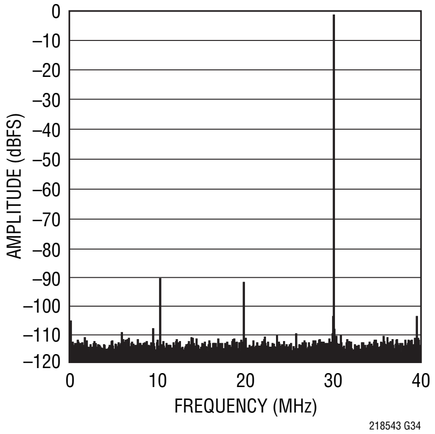
LTC2183: Differential Non-Linearity (DNL)



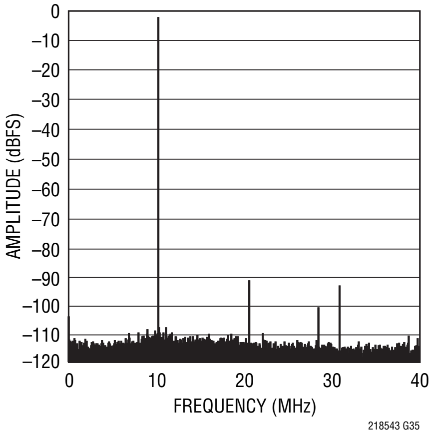
LTC2183: 64k Point FFT, f_{IN} = 5MHz, –1dBFS, 80Msps



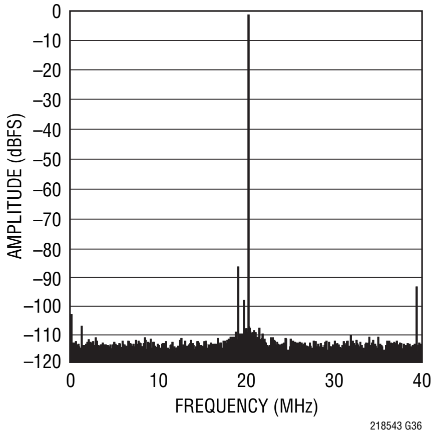
LTC2183: 64k Point FFT, f_{IN} = 30MHz, –1dBFS, 80Msps



LTC2183: 64k Point FFT, f_{IN} = 70MHz, –1dBFS, 80Msps

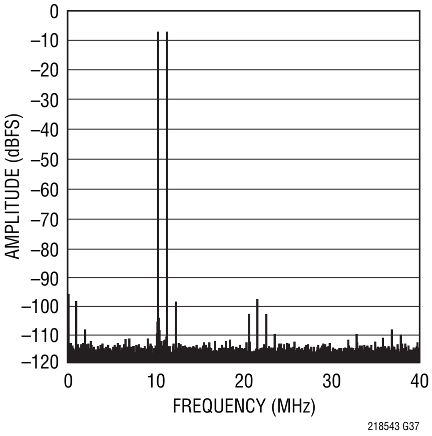


LTC2183: 64k Point FFT, f_{IN} = 140MHz, –1dBFS, 80Msps

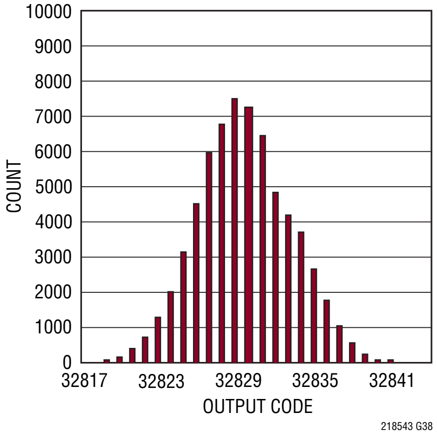


TYPICAL PERFORMANCE CHARACTERISTICS

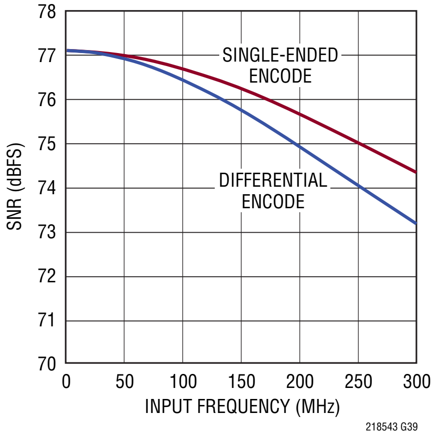
LTC2183: 64k Point 2-Tone FFT, f_{IN} = 69MHz, 70MHz, –7dBFS, 80Msps



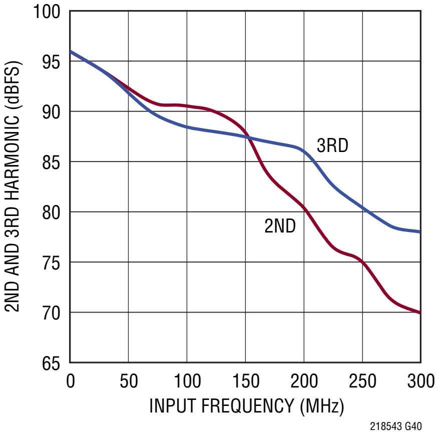
LTC2183: Shorted Input Histogram



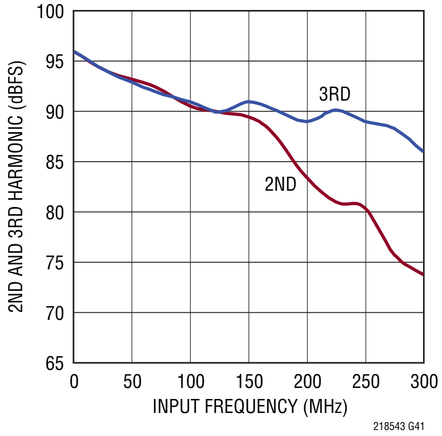
LTC2183: SNR vs Input Frequency, –1dBFS, 80Msps, 2V Range



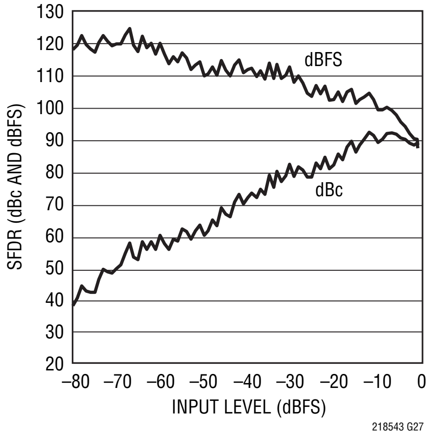
LTC2183: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 80Msps, 2V Range



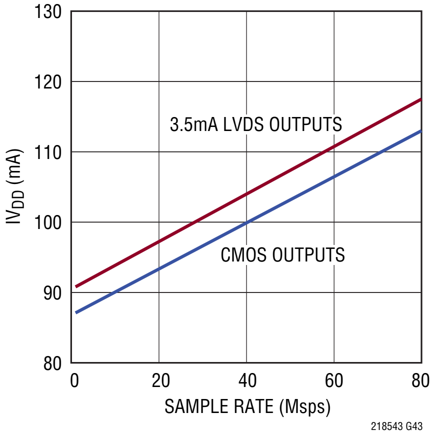
LTC2183: 2nd, 3rd Harmonic vs Input Frequency, –1dBFS, 80Msps, 1V Range



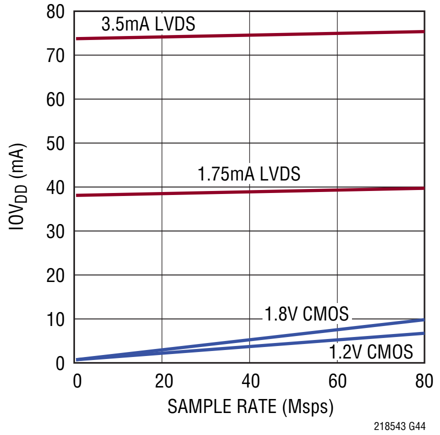
LTC2183: SFDR vs Input Level, f_{IN} = 70MHz, 80Msps, 2V Range



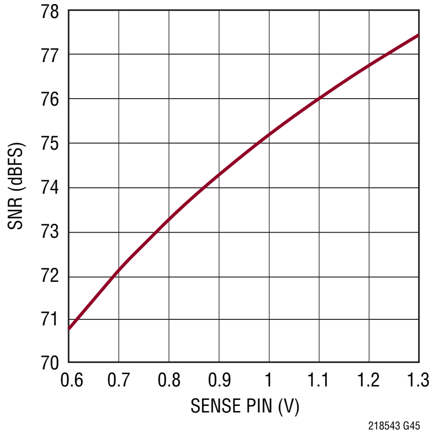
LTC2183: I_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input on Each Channel



LTC2183: IO_{VDD} vs Sample Rate, 5MHz, –1dBFS Sine Wave Input on Each Channel



LTC2183: SNR vs SENSE, f_{IN} = 5MHz, –1dBFS



PIN FUNCTIONS

PINS THAT ARE THE SAME FOR ALL DIGITAL OUTPUT MODES

V_{DD} (Pins 1, 16, 17, 64): Analog Power Supply, 1.7V to 1.9V. Bypass to ground with 0.1µF ceramic capacitors. Adjacent pins can share a bypass capacitor.

V_{CM1} (Pin 2): Common Mode Bias Output, nominally equal to $V_{DD}/2$. V_{CM1} should be used to bias the common mode of the analog inputs to channel 1. Bypass to ground with a 0.1µF ceramic capacitor.

GND (Pins 3, 6, 14): ADC Power Ground.

A_{IN1}^+ (Pin 4): Channel 1 Positive Differential Analog Input.

A_{IN1}^- (Pin 5): Channel 1 Negative Differential Analog Input.

REFH (Pins 7, 9): ADC High Reference. See the Applications Information section for recommended bypassing circuits for REFH and REFL.

REFL (Pins 8, 10): ADC Low Reference. See the Applications Information section for recommended bypassing circuits for REFH and REFL.

PAR/$\overline{\text{SER}}$ (Pin 11): Programming Mode selection pin. Connect to ground to enable the Serial Programming Mode. $\overline{\text{CS}}$, SCK, SDI, SDO become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable the Parallel Programming Mode where $\overline{\text{CS}}$, SCK, SDI, SDO become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{\text{SER}}$ should be connected directly to ground or V_{DD} and not be driven by a logic signal.

A_{IN2}^+ (Pin 12): Channel 2 Positive Differential Analog Input.

A_{IN2}^- (Pin 13): Channel 2 Negative Differential Analog Input.

V_{CM2} (Pin 15): Common Mode Bias Output, nominally equal to $V_{DD}/2$. V_{CM2} should be used to bias the common mode of the analog inputs to channel 2. Bypass to ground with a 0.1µF ceramic capacitor.

ENC^+ (Pin 18): Encode Input. Conversion starts on the rising edge.

ENC^- (Pin 19): Encode Complement Input. Conversion starts on the falling edge. Tie to GND for single-ended encode mode.

$\overline{\text{CS}}$ (Pin 20): In Serial Programming Mode, (PAR/$\overline{\text{SER}}$ = 0V), $\overline{\text{CS}}$ is the Serial Interface Chip Select Input. When $\overline{\text{CS}}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the Parallel Programming Mode (PAR/$\overline{\text{SER}}$ = V_{DD}), $\overline{\text{CS}}$ controls the Clock Duty Cycle Stabilizer (See Table 2). $\overline{\text{CS}}$ can be driven with 1.8V to 3.3V logic.

SCK (Pin 21): In Serial Programming Mode, (PAR/$\overline{\text{SER}}$ = 0V), SCK is the Serial Interface Clock Input. In the Parallel Programming Mode (PAR/$\overline{\text{SER}}$ = V_{DD}), SCK controls the Digital Output Mode (See Table 2). SCK can be driven with 1.8V to 3.3V logic.

SDI (Pin 22): In Serial Programming Mode, (PAR/$\overline{\text{SER}}$ = 0V), SDI is the Serial Interface Data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the Parallel Programming Mode (PAR/$\overline{\text{SER}}$ = V_{DD}), SDI can be used together with SDO to power down the part (see Table 2). SDI can be driven with 1.8V to 3.3V logic.

OGND (Pin 41): Output Driver Ground. Must be shorted to the ground plane by a very low inductance path. Use multiple vias close to the pin.

OV_{DD} (Pin 42): Output Driver Supply. Bypass to ground with a 0.1µF ceramic capacitor.

SDO (Pin 61): In Serial Programming Mode, (PAR/$\overline{\text{SER}}$ = 0V), SDO is the optional Serial Interface Data Output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V – 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the Parallel Programming Mode (PAR/$\overline{\text{SER}}$ = V_{DD}), SDO can be used together with SDI to power down the part (see Table 2). When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

V_{REF} (Pin 62): Reference Voltage Output. Bypass to ground with a 2.2µF ceramic capacitor. The output voltage is nominally 1.25V.

PIN FUNCTIONS

SENSE (Pin 63): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of $\pm 0.8 \bullet V_{SENSE}$.

Ground (Exposed Pad Pin 65): The exposed pad must be soldered to the PCB ground.

FULL-RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels ($OGND$ to OV_{DD})

D2_0 to D2_15 (Pins 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38): Channel 2 Digital Outputs. D2_15 is the MSB.

CLKOUT$^-$ (Pin 39): Inverted version of CLKOUT$^+$.

CLKOUT$^+$ (Pin 40): Data Output Clock. The Digital Outputs normally transition at the same time as the falling edge of CLKOUT$^+$. The phase of CLKOUT$^+$ can also be delayed relative to the Digital Outputs by programming the mode control registers.

D1_0 to D1_15 (Pins 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58): Channel 1 Digital Outputs. D1_15 is the MSB.

OF2 (Pin 59): Channel 2 Over/Under Flow Digital Output. OF2 is high when an overflow or underflow has occurred.

OF1 (Pin 60): Channel 1 Over/Under Flow Digital Output. OF1 is high when an overflow or underflow has occurred.

DOUBLE DATA RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels ($OGND$ to OV_{DD})

D2_0_1 to D2_14_15 (Pins 24, 26, 28, 30, 32, 34, 36, 38): Channel 2 Double Data Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12, D14) appear when CLKOUT$^+$ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13, D15) appear when CLKOUT$^+$ is high.

DNC (Pins 23, 25, 27, 29, 31, 33, 35, 37, 43, 45, 47, 49, 51, 53, 55, 57, 59): Do not connect these pins.

CLKOUT$^-$ (Pin 39): Inverted version of CLKOUT$^+$.

CLKOUT$^+$ (Pin 40): Data Output Clock. The Digital Outputs normally transition at the same time as the falling and rising edges of CLKOUT$^+$. The phase of CLKOUT$^+$ can also be delayed relative to the Digital Outputs by programming the mode control registers.

D1_0_1 to D1_14_15 (Pins 44, 46, 48, 50, 52, 54, 56, 58): Channel 1 Double Data Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12, D14) appear when CLKOUT$^+$ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13, D15) appear when CLKOUT$^+$ is high.

OF2_1 (Pin 60): Over/Under Flow Digital Output. OF2_1 is high when an overflow or underflow has occurred. The over/under flow for both channels are multiplexed onto this pin. Channel 2 appears when CLKOUT$^+$ is low, and Channel 1 appears when CLKOUT$^+$ is high.

DOUBLE DATA RATE LVDS OUTPUT MODE

All Pins Below Have LVDS Output Levels. The Output Current Level Is Programmable. There Is an Optional Internal 100Ω Termination Resistor Between the Pins of Each LVDS Output Pair.

D2_0_1$^-$/D2_0_1$^+$ to D2_14_15$^-$/D2_14_15$^+$ (Pins 23/24, 25/26, 27/28, 29/30, 31/32, 33/34, 35/36, 37/38): Channel 2 Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12, D14) appear when CLKOUT$^+$ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13, D15) appear when CLKOUT$^+$ is high.

CLKOUT$^-$/CLKOUT$^+$ (Pins 39/40): Data Output Clock. The Digital Outputs normally transition at the same time as the falling and rising edges of CLKOUT$^+$. The phase of CLKOUT$^+$ can also be delayed relative to the Digital Outputs by programming the mode control registers.

PIN FUNCTIONS

D1_0_1⁻/D1_0_1⁺ to D1_14_15⁻/D1_14_15⁺ (Pins 43/44, 45/46, 47/48, 49/50, 51/52, 53/54, 55/56, 57/58): Channel 2 Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12, D14) appear when CLKOUT⁺ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13, D15) appear when CLKOUT⁺ is high.

OF2_1⁻/OF2_1⁺ (Pins 59/60): Over/Under Flow Digital Output. OF2_1⁺ is high when an overflow or underflow has occurred. The over/under flow for both channels are multiplexed onto this pin. Channel 2 appears when CLKOUT⁺ is low, and Channel 1 appears when CLKOUT⁺ is high.

FUNCTIONAL BLOCK DIAGRAM

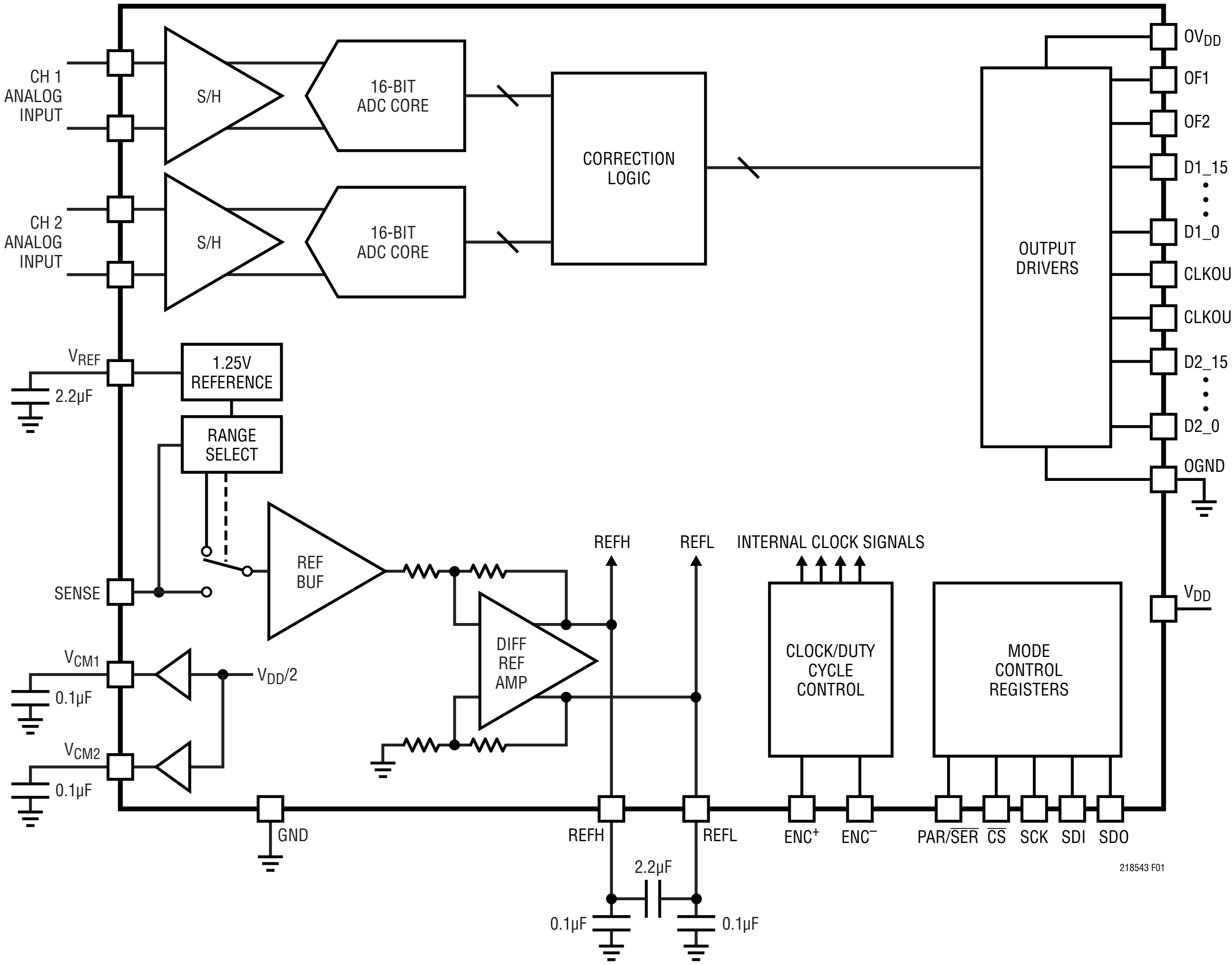


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2185/LTC2184/LTC2183 are low power, two-channel, 16-bit, 125Msps/105Msps/80Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially, or single ended for lower power consumption. The digital outputs can be CMOS, double data rate CMOS (to halve the number of output lines), or double data rate LVDS (to reduce digital noise in the system.) Many additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog inputs are differential CMOS sample-and-hold circuits (Figure 2). The inputs should be driven differentially around a common mode voltage set by the V_{CM1} or V_{CM2} output pins, which are nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from $V_{CM} - 0.5V$ to $V_{CM} + 0.5V$. There should be 180° phase difference between the inputs.

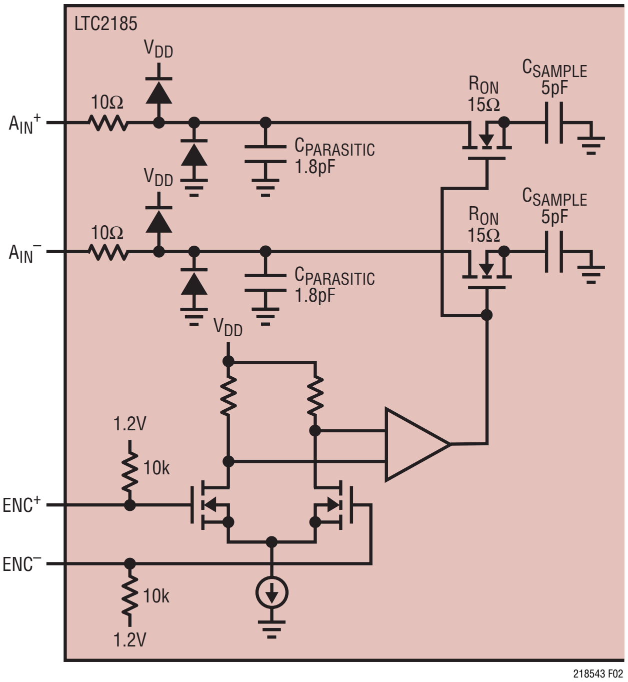


Figure 2. Equivalent Input Circuit. Only One of the Two Analog Channels Is Shown

The two channels are simultaneously sampled by a shared encode circuit (Figure 2).

Single-Ended Input

For applications less sensitive to harmonic distortion, the A_{IN}^+ input can be driven single-ended with a $1V_{P-P}$ signal centered around V_{CM}. The A_{IN}^- input should be connected to V_{CM}. With a single-ended input the harmonic distortion and INL will degrade, but the noise and DNL will remain unchanged.

INPUT DRIVE CIRCUITS

Input filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center tap is biased with V_{CM}, setting the A/D input at its optimal DC level. At higher input frequencies a transmission line balun transformer (Figure 4 to Figure 6) has better balance, resulting in lower A/D distortion.

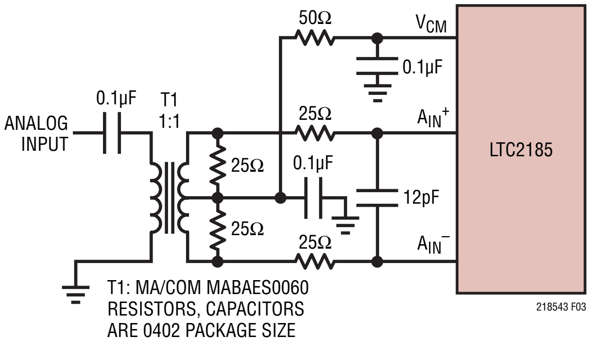


Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

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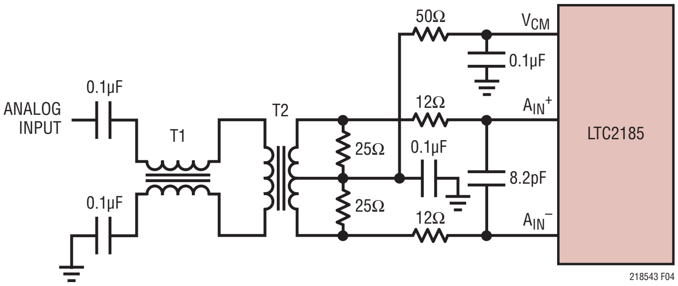
Amplifier Circuits

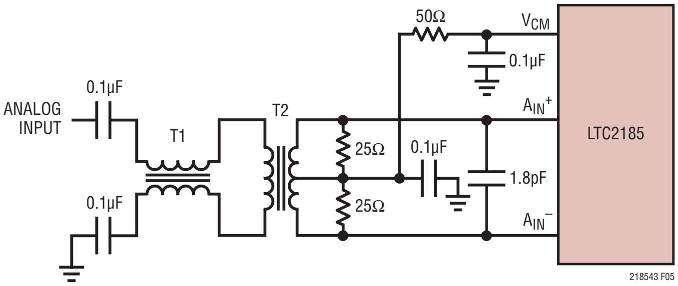
Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC-coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figure 4 to Figure 6) should convert the signal to differential before driving the A/D.



T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1TL
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 4. Recommended Front-End Circuit for Input Frequencies from 5MHz to 150MHz



T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1TL
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

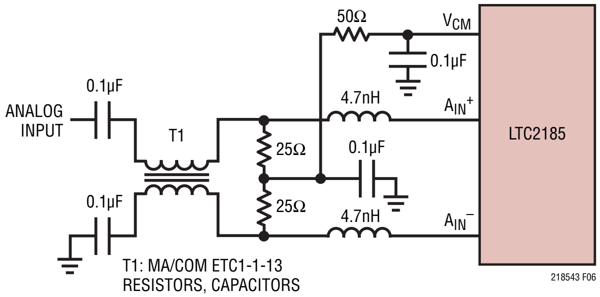
Figure 5. Recommended Front-End Circuit for Input Frequencies from 150MHz to 250MHz

Reference

The LTC2185/LTC2184/LTC2183 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be 1.6 • V_{SENSE}.

The V_{REF}, REFH and REFL pins should be bypassed as shown in Figure 8. A low inductance 2.2µF interdigitated capacitor is recommended for the bypass between REFH and REFL. This type of capacitor is available at a low cost from multiple suppliers.



T1: MA/COM ETC1-1-13
RESISTORS, CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 6. Recommended Front-End Circuit for Input Frequencies Above 250MHz

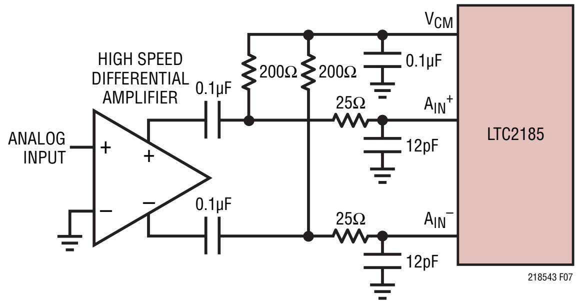


Figure 7. Front-End Circuit Using a High Speed Differential Amplifier

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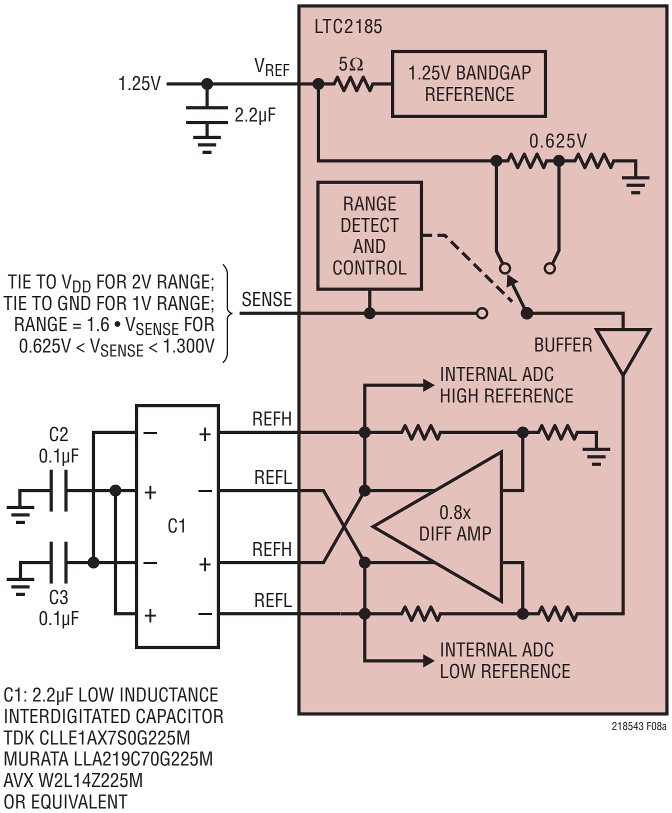

Figure 8a. Reference Circuit

At sample rates below 110Msps an interdigitated capacitor is not necessary for good performance and C1 can be replaced by a standard 2.2µF capacitor between REFH and REFL (see Figure 8b). The capacitors should be as close to the pins as possible (not on the back side of the circuit board).

Figure 8c and Figure 8d show the recommended circuit board layout for the REFH/REFL bypass capacitors. Note that in Figure 8c, every pin of the interdigitated capacitor (C1) is connected since the pins are not internally connected in some vendors' capacitors. In Figure 8d the REFH and REFL pins are connected by short jumpers in an internal layer. To minimize the inductance of these jumpers they can be placed in a small hole in the GND plane on the second board layer.

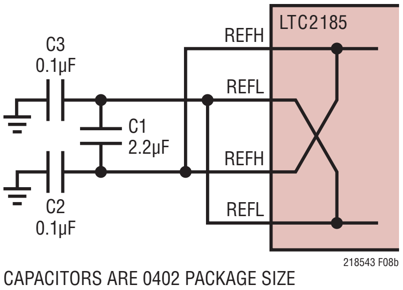

Figure 8b. Alternative REFH/REFL Bypass Circuit

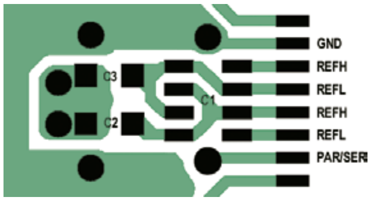

Figure 8c. Recommended Layout for the REFH/REFL Bypass Circuit in Figure 8a

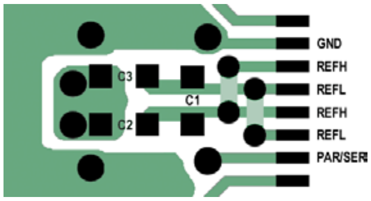

Figure 8d. Recommended Layout for the REFH/REFL Bypass Circuit in Figure 8b.

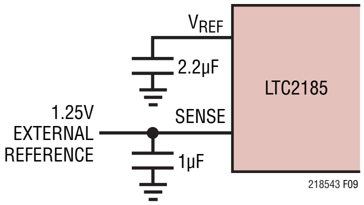

Figure 9. Using an External 1.25V Reference

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals – do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10), and the single-ended encode mode (Figure 11).

The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figure 12 and Figure 13). The encode inputs are internally biased to 1.2V

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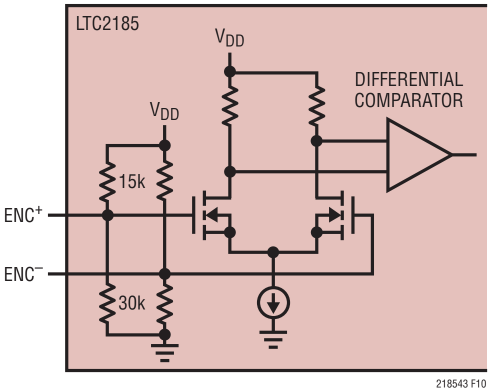


Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode

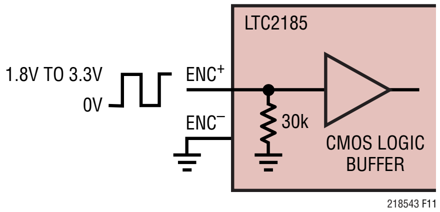
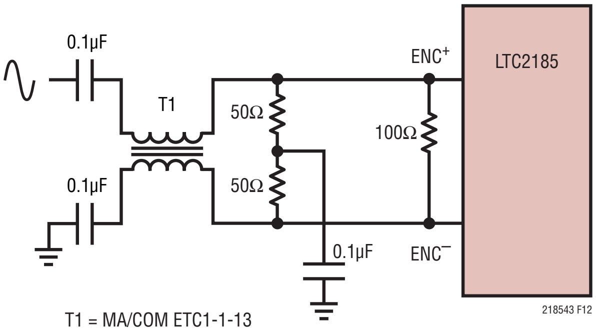


Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode



T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 12. Sinusoidal Encode Drive

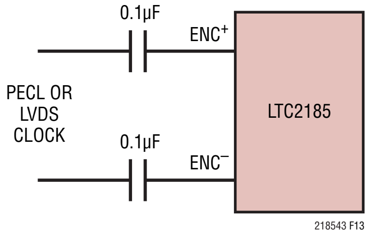


Figure 13. PECL or LVDS Encode Drive

through 10kΩ equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC^- should stay at least 200mV above ground to avoid falsely triggering the single ended encode mode. For good jitter performance ENC^+ and ENC^- should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC^- is connected to ground and ENC^+ is driven with a square wave encode input. ENC^+ can be taken above V_{DD} (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The ENC^+ threshold is 0.9V. For good jitter performance ENC^+ should have fast rise and fall times.

If the encode signal is turned off or drops below approximately 500kHz, the A/D enters nap mode.

Clock Duty Cycle Stabilizer

For good performance the encode signal should have a 50% (±5%) duty cycle. If the optional clock duty cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the encode signal changes frequency, the duty cycle stabilizer circuit requires one hundred clock cycles to lock onto the input clock. The duty cycle stabilizer is enabled by mode control register A2 (Serial Programming Mode), or by $\overline{CS}$ (Parallel Programming Mode).

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50% (±5%) duty cycle. The duty cycle stabilizer should not be used below 5Msps.

DIGITAL OUTPUTS

Digital Output Modes

The LTC2185/LTC2184/LTC2183 can operate in three digital output modes: full rate CMOS, double data rate CMOS (to halve the number of output lines), or double data rate LVDS (to reduce digital noise in the system.) The output mode is set by mode control register A3 (Serial Programming

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Mode), or by SCK (Parallel Programming Mode). Note that double data rate CMOS cannot be selected in the Parallel Programming Mode.

Full Rate CMOS Mode

In Full Rate CMOS Mode the data outputs (D1_0 to D1_15 and D2_0 to D2_15), overflow (OF2, OF1), and the data output clocks ($CLKOUT^+$, $CLKOUT^–$) have CMOS output levels. The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. OV_{DD} can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF a digital buffer should be used.

Double Data Rate CMOS Mode

In Double Data Rate CMOS Mode, two data bits are multiplexed and output on each data pin. This reduces the number of digital lines by seventeen, simplifying board routing and reducing the number of input pins needed to receive the data. The data outputs (D1_0_1, D1_2_3, D1_4_5, D1_6_7, D1_8_9, D1_10_11, D1_12_13, D1_14_15, D2_0_1, D2_2_3, D2_4_5, D2_6_7, D2_8_9, D2_10_11, D2_12_13, D2_14_15), overflow (OF2_1), and the data output clocks ($CLKOUT^+$, $CLKOUT^–$) have CMOS output levels. The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. OV_{DD} can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs. Note that the overflow for both ADC channels is multiplexed onto the OF2_1 pin.

For good performance the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF a digital buffer should be used.

When using Double Data Rate CMOS at sample rates above 100Msps the SNR may degrade slightly, about 0.2dB to 0.5dB depending on load capacitance and board layout.

Double Data Rate LVDS Mode

In Double Data Rate LVDS Mode, two data bits are multiplexed and output on each differential output pair. There are eight LVDS output pairs per ADC channel ($D1\_0\_1^+$/$D1\_0\_1^–$ through $D1\_14\_15^+$/$D1\_14\_15^–$ and $D2\_0\_1^+$/$D2\_0\_1^–$ through $D2\_14\_15^+$/$D2\_14\_15^–$) for the digital output data. Overflow ($OF2\_1^+$/$OF2\_1^–$) and the data output clock ($CLKOUT^+$/$CLKOUT^–$) each have an LVDS output pair. Note that the overflow for both ADC channels is multiplexed onto the $OF2\_1^+$/$OF2\_1^–$ output pair.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. In LVDS mode, OV_{DD} must be 1.8V.

Programmable LVDS Output Current

In LVDS Mode, the default output driver current is 3.5mA. This current can be adjusted by serially programming mode control register A3. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing.

Overflow Bit

The overflow output bit outputs a logic high when the analog input is either over-ranged or under-ranged. The overflow bit has the same pipeline latency as the data bits. In Full-Rate CMOS mode each ADC channel has its own overflow pin (OF1 for channel 1, OF2 for channel 2). In DDR CMOS or DDR LVDS mode the overflow for both ADC channels is multiplexed onto the OF2_1 output.

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Phase Shifting the Output Clock

In Full Rate CMOS mode the data output bits normally change at the same time as the falling edge of CLKOUT$^+$, so the rising edge of CLKOUT$^+$ can be used to latch the output data. In Double Data Rate CMOS and LVDS Modes the data output bits normally change at the same time as the falling and rising edges of CLKOUT$^+$. To allow adequate set-up and hold time when latching the data, the CLKOUT$^+$ signal may need to be phase shifted relative to the data output bits. Most FPGAs have this feature; this is generally the best place to adjust the timing.

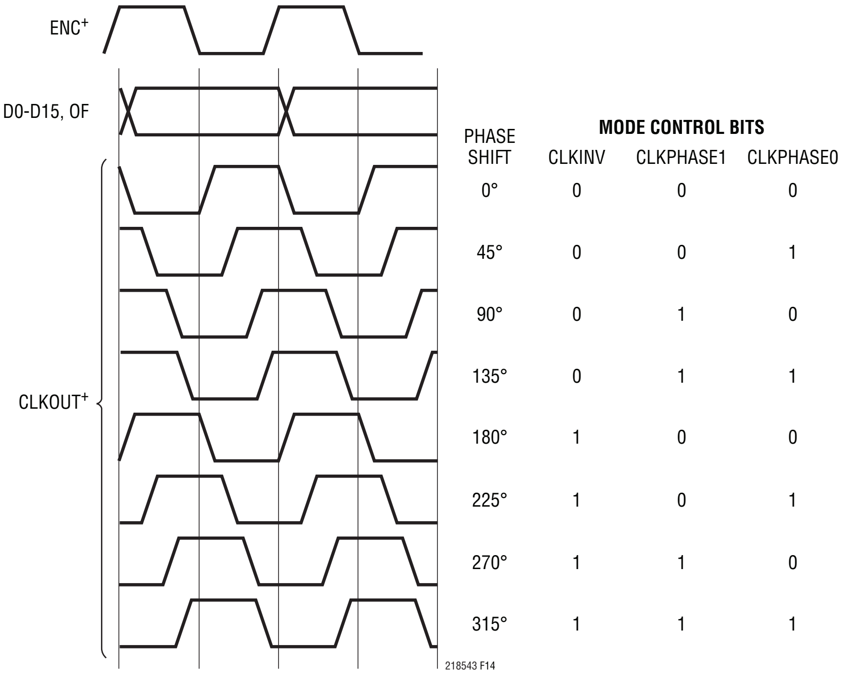
The LTC2185/LTC2184/LTC2183 can also phase shift the CLKOUT$^+$/CLKOUT$^-$ signals by serially programming mode control register A2. The output clock can be shifted by 0°, 45°, 90°, or 135°. To use the phase shifting feature the Clock Duty Cycle Stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT$^+$ and CLKOUT$^-$, independently of the phase shift. The combination of these two features enables phase shifts of 45° up to 315° (Figure 14).

DATA FORMAT

Table 1 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A4.

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ – A_{IN}^-$ (2V Range)	OF	D15-D0 (OFFSET BINARY)	D15-D0 (2's COMPLEMENT)
>1.000000V	1	1111 1111 1111 1111	0111 1111 1111 1111
+0.999970V	0	1111 1111 1111 1111	0111 1111 1111 1111
+0.999939V	0	1111 1111 1111 1110	0111 1111 1111 1110
+0.000030V	0	1000 0000 0000 0001	0000 0000 0000 0001
+0.000000V	0	1000 0000 0000 0000	0000 0000 0000 0000
–0.000030V	0	0111 1111 1111 1111	1111 1111 1111 1111
–0.000061V	0	0111 1111 1111 1110	1111 1111 1111 1110
–0.999939V	0	0000 0000 0000 0001	1000 0000 0000 0001
–1.000000V	0	0000 0000 0000 0000	1000 0000 0000 0000
<–1.000000V	1	0000 0000 0000 0000	1000 0000 0000 0000



PHASE SHIFT	MODE CONTROL BITS CLKINV	CLKPHASE1	CLKPHASE0
0°	0	0	0
45°	0	0	1
90°	0	1	0
135°	0	1	1
180°	1	0	0
225°	1	0	1
270°	1	1	0
315°	1	1	1

Figure 14. Phase Shifting CLKOUT

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Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied – an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output randomizer is enabled by serially programming mode control register A4.

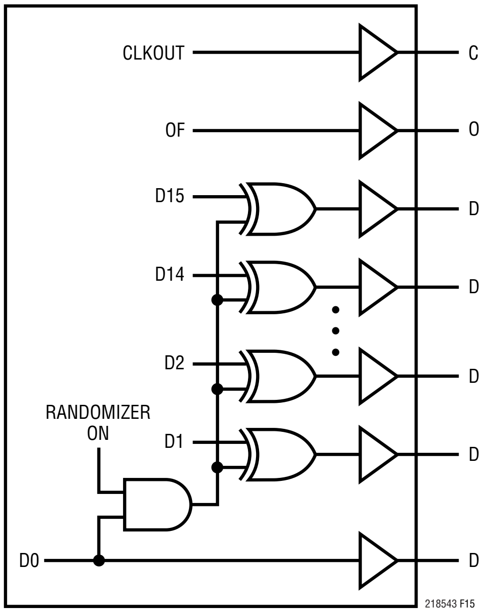

Figure 15. Functional Equivalent of Digital Output Randomizer

Alternate Bit Polarity

Another feature that reduces digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11, D13, D15) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10, D12, D14), OF and CLKOUT are not affected. This can reduce digital currents in the circuit board ground plane and reduce digital noise, particularly for very small analog input signals.

When there is a very small signal at the input of the A/D that is centered around mid-scale, the digital outputs toggle between mostly 1's and mostly 0's. This simultaneous switching of most of the bits will cause large currents in the ground plane. By inverting every other bit, the Alternate Bit Polarity Mode makes half of the bits transition high while half of the bits transition low. This cancels current flow in the ground plane, reducing the digital noise.

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11, D13, D15.) The Alternate Bit Polarity Mode is independent of the Digital Output Randomizer – either, both or neither function can be on at the same time. The Alternate Bit Polarity Mode is enabled by serially programming mode control register A4.

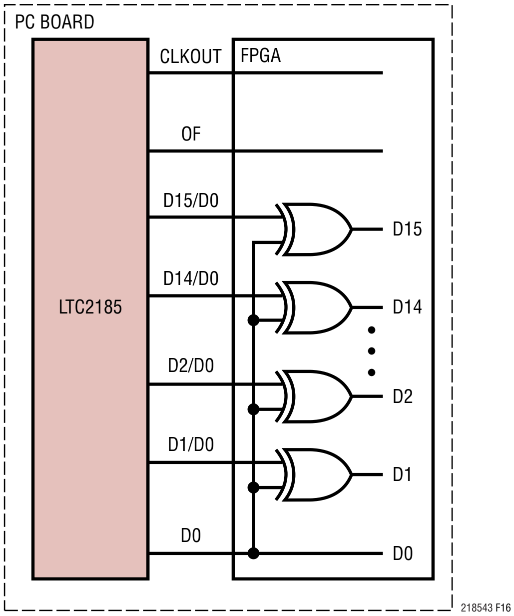

Figure 16. Unrandomizing a Randomized Digital Output Signal

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Digital Output Test Patterns

To allow in-circuit testing of the digital interface to the A/D, there are several test modes that force the A/D data outputs (OF, D15-D0) to known values:

All 1s: All outputs are 1

All 0s: All outputs are 0

Alternating: Outputs change from all 1s to all 0s on alternating samples.

Checkerboard: Outputs change from 1010101010101010 to 0101010101010101 on alternating samples.

The digital output test patterns are enabled by serially programming mode control register A4. When enabled, the Test Patterns override all other formatting modes: 2's complement, randomizer, alternate bit polarity.

Output Disable

The digital outputs may be disabled by serially programming mode control register A3. All digital outputs including OF and CLKOUT are disabled. The high-impedance disabled state is intended for in-circuit testing or long periods of inactivity – it is too slow to multiplex a data bus between multiple converters at full speed. When the outputs are disabled both channels should be put into either sleep or nap mode.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire device is powered down, resulting in 1mW power consumption. The amount of time required to recover from sleep mode depends on the size of the bypass capacitors on V_{REF}, REFH, and REFL. For the suggested values in Fig. 8, the A/D will stabilize after 2ms.

In nap mode the A/D core is powered down while the internal reference circuits stay active, allowing faster wakeup than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50μs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Either channel 2 or both channels can be placed in nap mode; it is not possible to have channel 1 in nap mode and channel 2 operating normally.

Sleep mode and nap mode are enabled by mode control register A1 (serial programming mode), or by SDI and SDO (parallel programming mode).

DEVICE PROGRAMMING MODES

The operating modes of the LTC2185/LTC2184/LTC2183 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{\text{SER}}$ should be tied to V_{DD}. The $\overline{\text{CS}}$, SCK, SDI and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. When used as an input, SDO should be driven through a 1k series resistor. Table 2 shows the modes set by $\overline{\text{CS}}$, SCK, SDI and SDO.

Table 2. Parallel Programming Mode Control Bits (PAR/$\overline{\text{SER}}$ = V_{DD})

PIN	DESCRIPTION
$\overline{\text{CS}}$	**Clock Duty Cycle Stabilizer Control Bit** 0 = Clock Duty Cycle Stabilizer Off 1 = Clock Duty Cycle Stabilizer On
SCK	**Digital Output Mode Control Bit** 0 = Full-Rate CMOS Output Mode 1 = Double Data Rate LVDS Output Mode (3.5mA LVDS Current, Internal Termination Off)
SDI/SDO	**Power Down Control Bit** 00 = Normal Operation 01 = Channel 1 in Normal Operation, Channel 2 in Nap Mode 10 = Channel 1 and Channel 2 in Nap Mode 11 = Sleep Mode (Entire Device Powered Down)

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Serial Programming Mode

To use the serial programming mode, PAR/$\overline{\text{SER}}$ should be tied to ground. The $\overline{\text{CS}}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{\text{CS}}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{\text{CS}}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{\text{W}}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{\text{W}}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{\text{W}}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the timing diagrams). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed, then SDO can be left floating and no pull-up resistor is needed.

Table 3 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset is complete, bit D7 is automatically set back to zero.

GROUNDING AND BYPASSING

The LTC2185/LTC2184/LTC2183 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane in the first layer beneath the ADC is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF}, REFH and REFL pins. Bypass capacitors must be located as close to the pins as possible. Size 0402 ceramic capacitors are recommended. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Of particular importance is the capacitor between REFH and REFL. This capacitor should be on the same side of the circuit board as the A/D, and as close to the device as possible. A low inductance interdigitated capacitor is suggested for REFH/REFL if the sampling frequency is greater than 110Msps.

The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

Most of the heat generated by the LTC2185/LTC2184/LTC2183 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

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Table 3. Serial Programming Mode Register Map (PAR/$\overline{\text{SER}}$ = GND)

REGISTER A0: RESET REGISTER (ADDRESS 00h)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7	**RESET**	Software Reset Bit
	0 = Not Used	
	1 = Software Reset. All Mode Control Registers Are Reset to 00h. The ADC Is Momentarily Placed in SLEEP Mode. This Bit Is Automatically Set Back to Zero After the Reset Is Complete	
Bits 6-0	Unused, Don't Care Bits.	

REGISTER A1: POWER-DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	PWROFF1	PWROFF0

Bits 7-2	Unused, Don't Care Bits.	
Bits 1-0	**PWROFF1:PWROFF0**	Power Down Control Bits
	00 = Normal Operation	
	01 = Channel 1 in Normal Operation, Channel 2 in Nap Mode	
	10 = Channel 1 and Channel 2 in Nap Mode	
	11 = Sleep Mode	

REGISTER A2: TIMING REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	CLKINV	CLKPHASE1	CLKPHASE0	DCS

Bits 7-4	Unused, Don't Care Bits.	
Bit 3	**CLKINV**	Output Clock Invert Bit
	0 = Normal CLKOUT Polarity (As Shown in the Timing Diagrams)	
	1 = Inverted CLKOUT Polarity	
Bits 2-1	**CLKPHASE1:CLKPHASE0**	Output Clock Phase Delay Bits
	00 = No CLKOUT Delay (As Shown in the Timing Diagrams)	
	01 = CLKOUT$^+$/CLKOUT$^-$ Delayed by 45° (Clock Period • 1/8)	
	10 = CLKOUT$^+$/CLKOUT$^-$ Delayed by 90° (Clock Period • 1/4)	
	11 = CLKOUT$^+$/CLKOUT$^-$ Delayed by 135° (Clock Period • 3/8)	
	Note: If the CLKOUT Phase Delay Feature Is Used, the Clock Duty Cycle Stabilizer Must Also Be Turned On	
Bit 0	**DCS**	Clock Duty Cycle Stabilizer Bit
	0 = Clock Duty Cycle Stabilizer Off	
	1 = Clock Duty Cycle Stabilizer On	

APPLICATIONS INFORMATION

REGISTER A3: OUTPUT MODE REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
X	ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE1	OUTMODE0

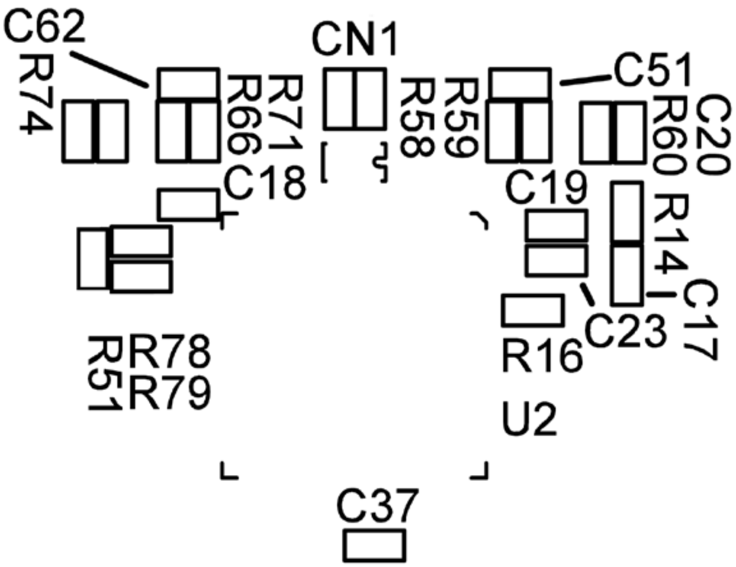
Bit 7	Unused, Don't Care Bit.
Bits 6-4	**ILVDS2:ILVDS0** LVDS Output Current Bits 000 = 3.5mA LVDS Output Driver Current 001 = 4.0mA LVDS Output Driver Current 010 = 4.5mA LVDS Output Driver Current 011 = Not Used 100 = 3.0mA LVDS Output Driver Current 101 = 2.5mA LVDS Output Driver Current 110 = 2.1mA LVDS Output Driver Current 111 = 1.75mA LVDS Output Driver Current
Bit 3	**TERMON** LVDS Internal Termination Bit 0 = Internal Termination Off 1 = Internal Termination On. LVDS Output Driver Current is 2× the Current Set by ILVDS2:ILVDS0
Bit 2	**OUTOFF** Output Disable Bit 0 = Digital Outputs Are Enabled 1 = Digital Outputs Are Disabled and Have High Output Impedance Note: If the Digital Outputs Are Disabled the Part Should Also Be Put in Sleep or Nap Mode (Both Channels).
Bits 1-0	**OUTMODE1:OUTMODE0** Digital Output Mode Control Bits 00 = Full-Rate CMOS Output Mode 01 = Double Data Rate LVDS Output Mode 10 = Double Data Rate CMOS Output Mode 11 = Not Used

REGISTER A4: DATA FORMAT REGISTER (ADDRESS 04h)

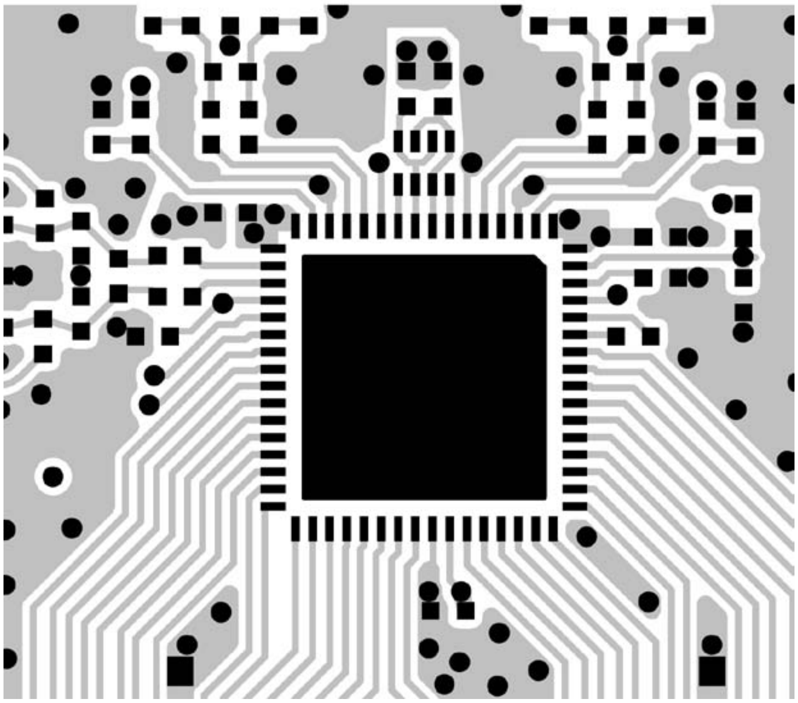
D7	D6	D5	D4	D3	D2	D1	D0
X	X	OUTTEST2	OUTTEST1	OUTTEST0	ABP	RAND	TWOSCOMP

Bit 7-6	Unused, Don't Care Bits.
Bits 5-3	**OUTTEST2:OUTTEST0** Digital Output Test Pattern Bits 000 = Digital Output Test Patterns Off 001 = All Digital Outputs = 0 011 = All Digital Outputs = 1 101 = Checkerboard Output Pattern. OF, D15-D0 Alternate Between 1 0101 0101 0101 0101 and 0 1010 1010 1010 1010 111 = Alternating Output Pattern. OF, D15-D0 Alternate Between 0 0000 0000 0000 0000 and 1 1111 1111 1111 1111 Note: Other Bit Combinations Are not Used
Bit 2	**ABP** Alternate Bit Polarity Mode Control Bit 0 = Alternate Bit Polarity Mode Off 1 = Alternate Bit Polarity Mode On. Forces the Output Format to Be Offset Binary
Bit 1	**RAND** Data Output Randomizer Mode Control Bit 0 = Data Output Randomizer Mode Off 1 = Data Output Randomizer Mode On
Bit 0	**TWOSCOMP** Two's Complement Mode Control Bit 0 = Offset Binary Data Format 1 = Two's Complement Data Format

TYPICAL APPLICATIONS

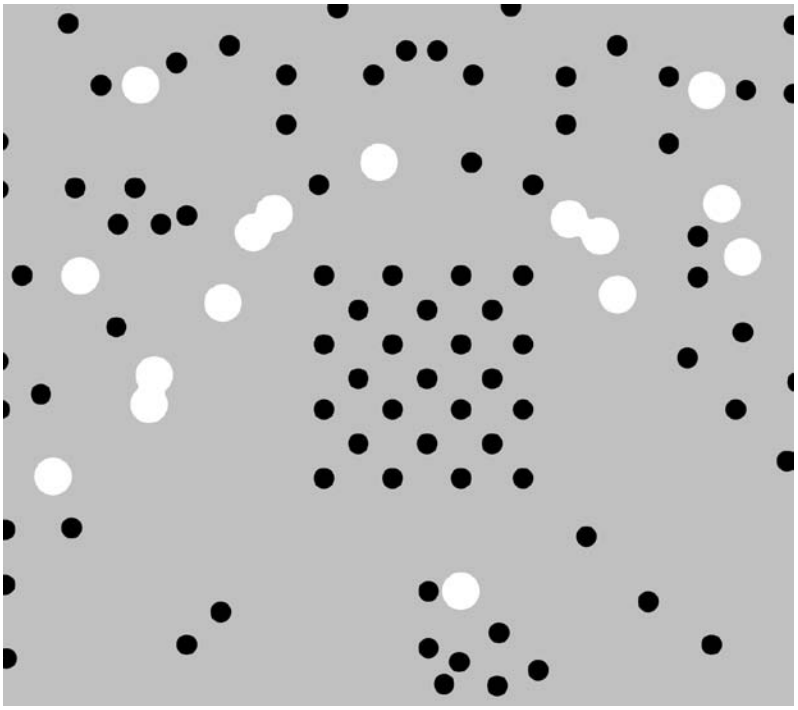


Silkscreen Top

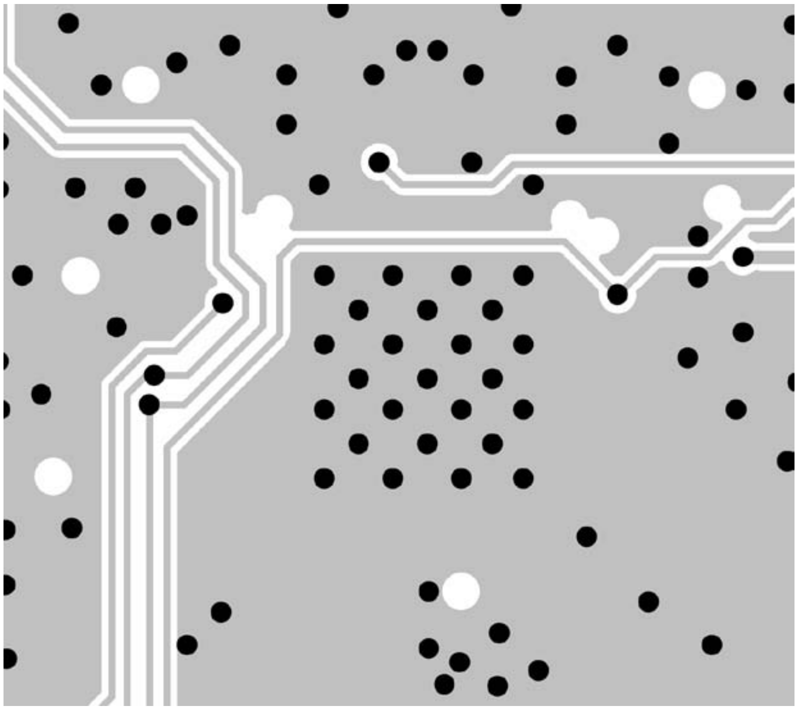


Top Side

TYPICAL APPLICATIONS

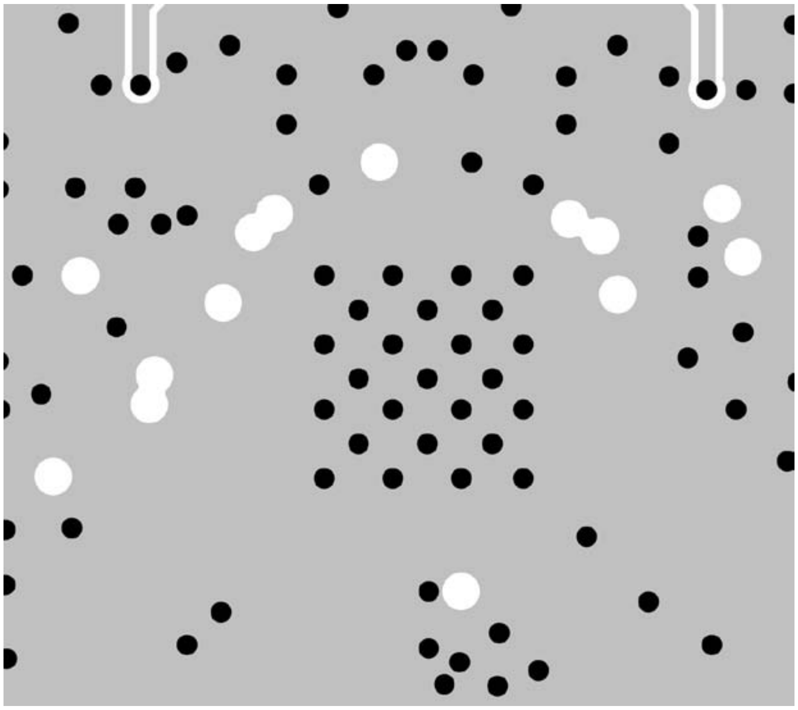


Inner Layer 2 GND

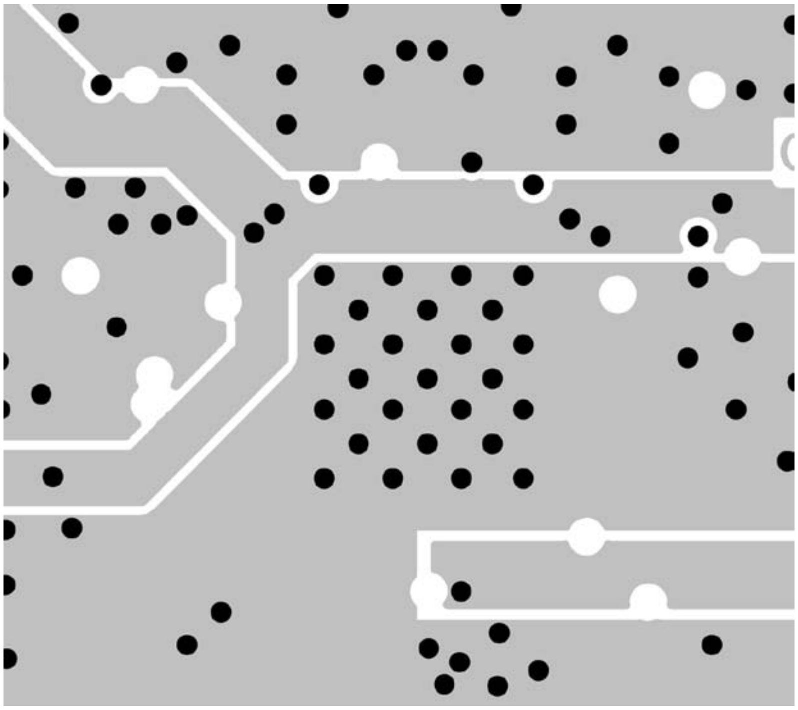


Inner Layer 3

TYPICAL APPLICATIONS

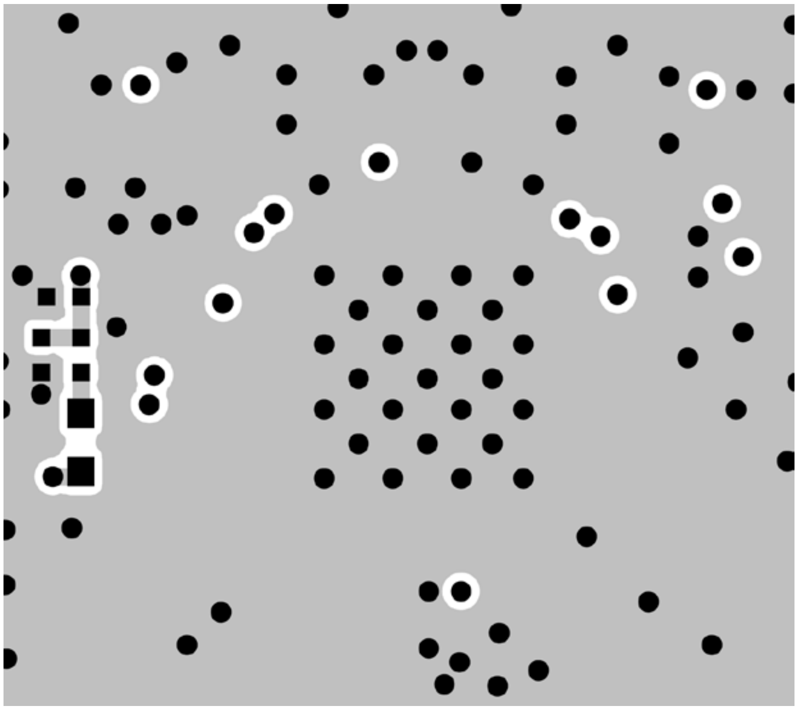


Inner Layer 4



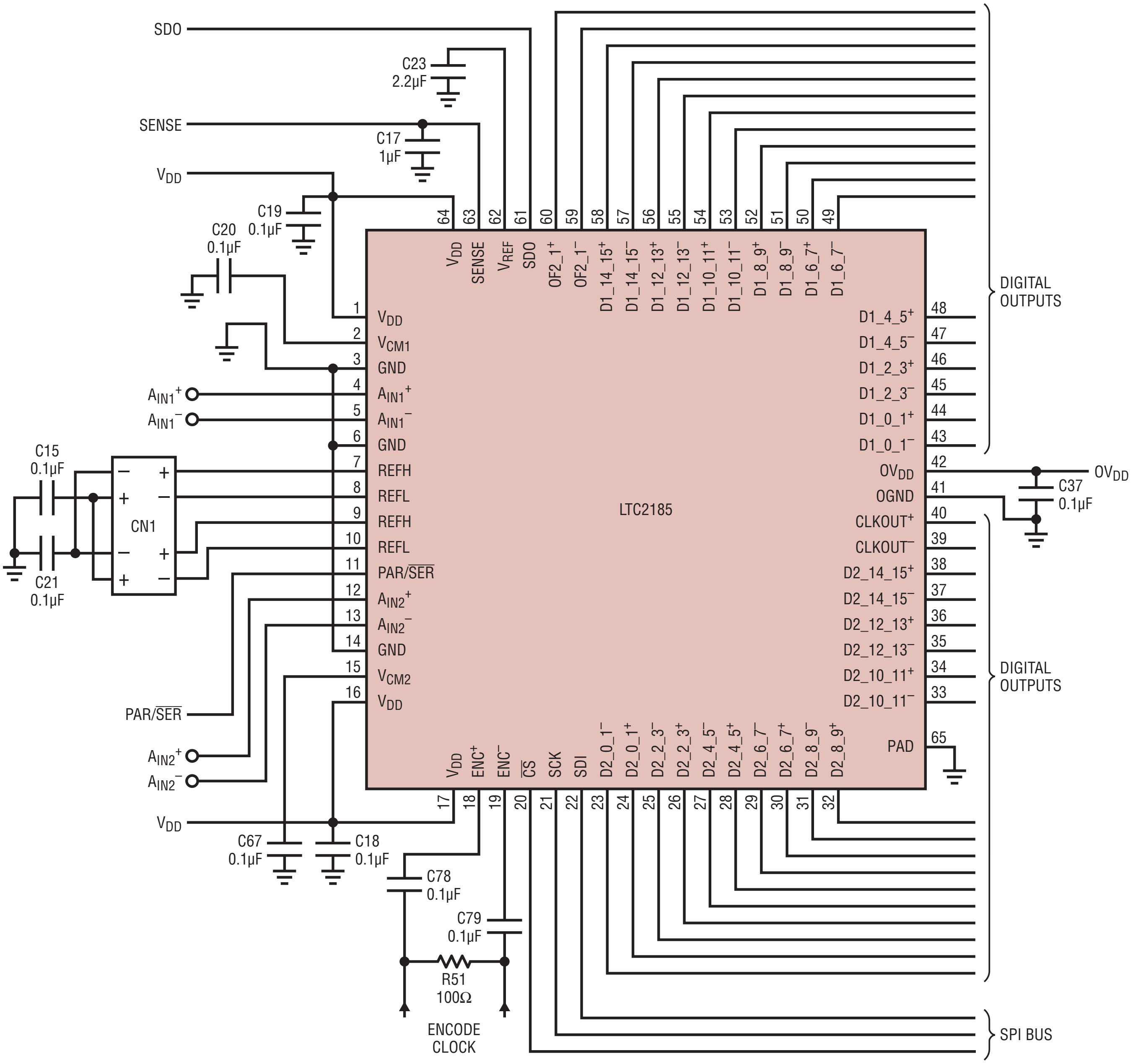
Inner Layer 5 Power

TYPICAL APPLICATIONS



Bottom Side

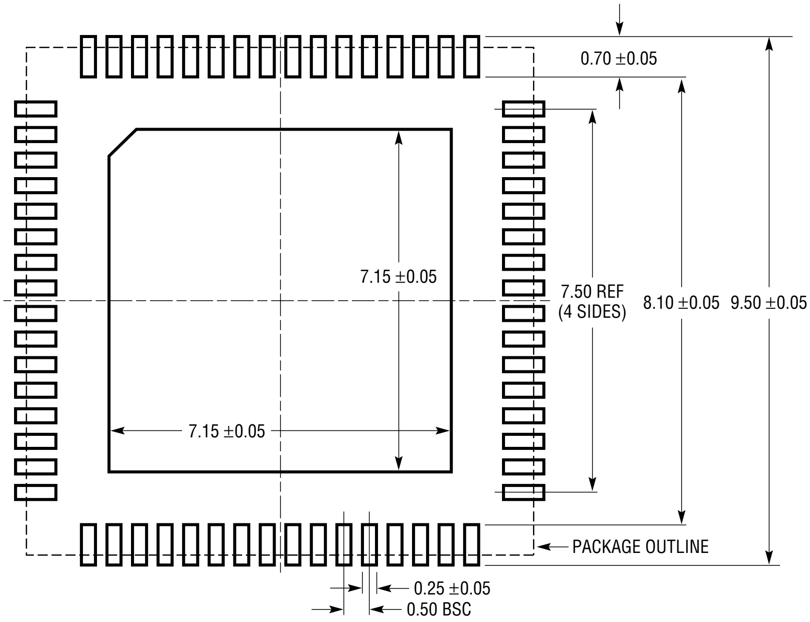
TYPICAL APPLICATIONS



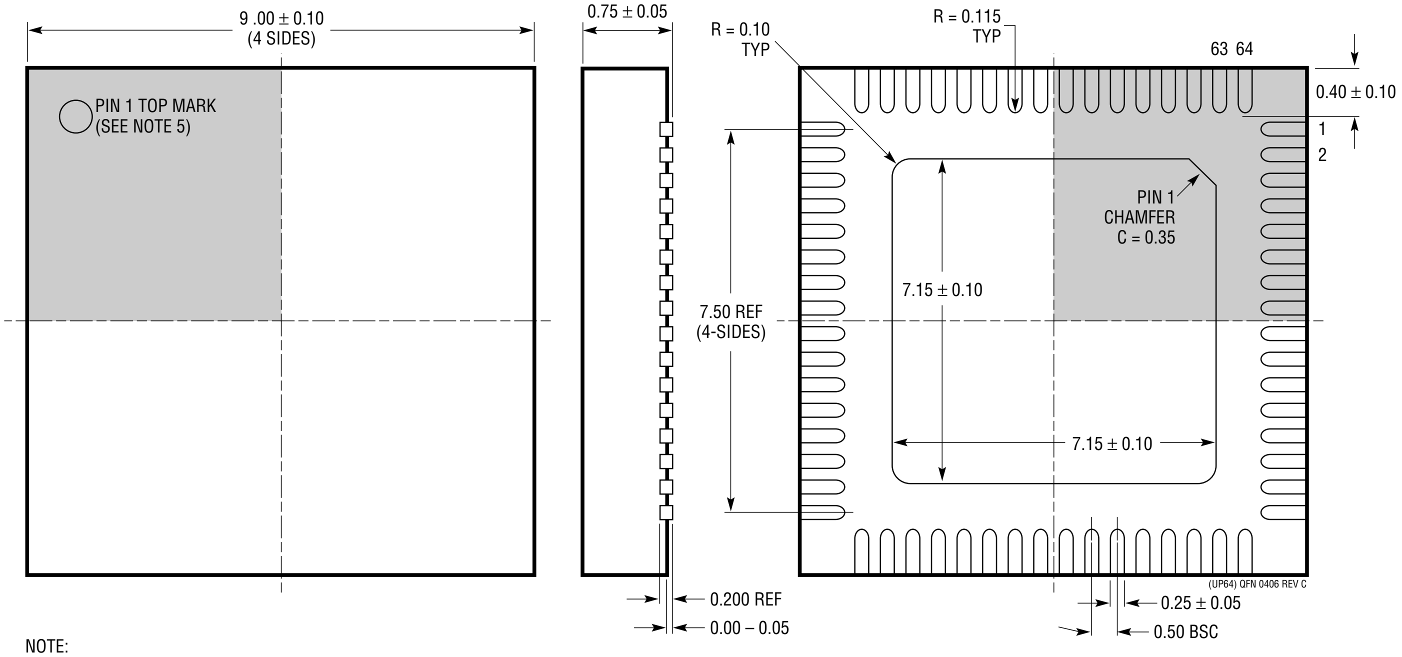
LTC2185 Schematic

PACKAGE DESCRIPTION

UP Package
64-Lead Plastic QFN (9mm × 9mm)
(Reference LTC DWG # 05-08-1705 Rev C)



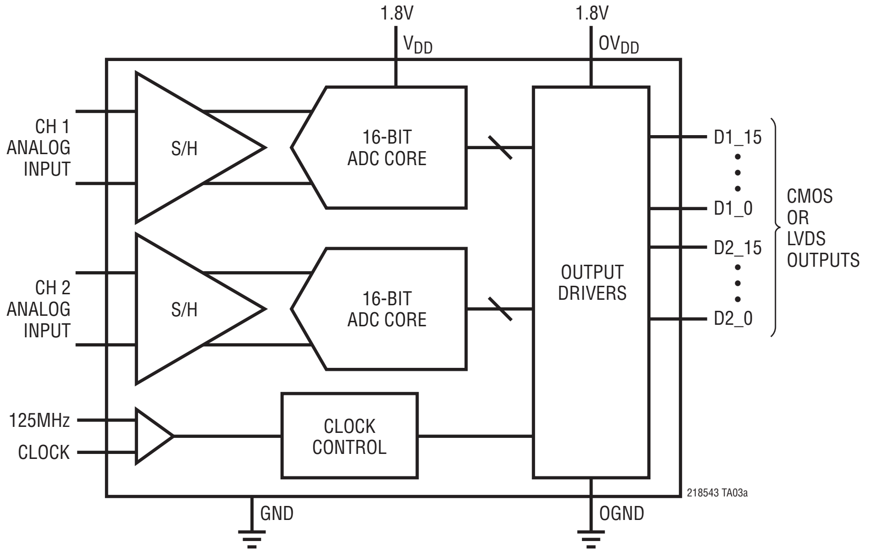
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



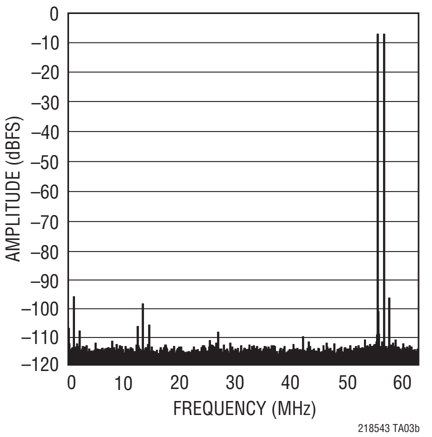
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

TYPICAL APPLICATION



2-Tone FFT, f_{IN} = 70MHz and 69MHz



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2259-14/LTC2260-14/ LTC2261-14	14-Bit, 80Msps/105Msps/125Msps 1.8V ADCs, Ultralow Power	89mW/106mW/127mW, 73.4dB SNR, 85dB SFDR, DDR LVDS/DDR CMOS/CMOS Outputs, 6mm × 6mm QFN-40
LTC2266-14/LTC2267-14/ LTC2268-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
LTC2266-12/LTC2267-12/ LTC2268-12	12-Bit, 80Msps/105Msps/125Msps 1.8V Dual ADCs, Ultralow Power	216mW/250mW/293mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 6mm × 6mm QFN-40
RF Mixers/Demodulators		
LTC5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	High IIP3: 21dBm at 800MHz, Integrated LO Quadrature Generator
LTC5527	400MHz to 3.7GHz High Linearity Downconverting Mixer	24.5dBm IIP3 at 900MHz, 23.5dBm IIP3 at 3.5GHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LTC5557	400MHz to 3.8GHz High Linearity Downconverting Mixer	23.7dBm IIP3 at 2.6GHz, 23.5dBm IIP3 at 3.5GHz, NF = 13.2dB, 3.3V Supply Operation, Integrated Transformer
LTC5575	800MHz to 2.7GHz Direct Conversion Quadrature Demodulator	High IIP3: 28dBm at 900MHz, Integrated LO Quadrature Generator, Integrated RF and LO Transformer
Amplifiers/Filters		
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, 1nV/√Hz Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6421-20	1.3GHz Dual Low Noise, Low Distortion Differential ADC Drivers	Fixed Gain 10V/V, 1nV/√Hz Total Input Noise, 40mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6605-7/LTC6605-10/ LTC6605-14	Dual Matched 7MHz/10MHz/14MHz Filters with ADC Drivers	Dual Matched 2nd Order Lowpass Filters with Differential Drivers, Pin-Programmable Gain, 6mm × 3mm DFN-22
Signal Chain Receivers		
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers

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