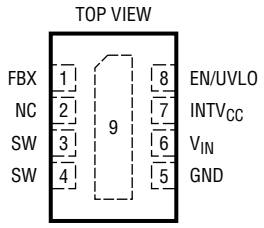
ABSOLUTE MAXIMUM RATINGS (Note 1)

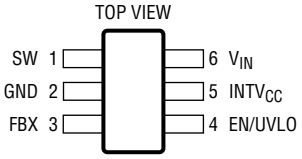
SW 60V
V_{IN}, EN/UVLO 40V
EN/UVLO Pin Above V_{IN} Pin 6V
$INTV_{CC}$ (Note 2) 4V
FBX ..... ±4V

Operating Junction Temperature (Note 3)
LT8330E, LT8330I ..... –40°C to 125°C
LT8330J, LT8330H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
θ_{JA} = 60°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



S6 PACKAGE
6-LEAD PLASTIC TSOT-23
θ_{JA} = 125°C/W, θ_{JC} = 102°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8330ES6#TRMPBF	LT8330ES6#TRPBF	LTGMQ	6-Lead Plastic TSOT-23	–40°C to 125°C
LT8330IS6#TRMPBF	LT8330IS6#TRPBF	LTGMQ	6-Lead Plastic TSOT-23	–40°C to 125°C
LT8330JS6#TRMPBF	LT8330JS6#TRPBF	LTGMQ	6-Lead Plastic TSOT-23	–40°C to 150°C
LT8330HS6#TRMPBF	LT8330HS6#TRPBF	LTGMQ	6-Lead Plastic TSOT-23	–40°C to 150°C
LT8330EDDB#TRMPBF	LT8330EDDB#TRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8330IDDB#TRMPBF	LT8330IDDB#TRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8330JDDB#TRMPBF	LT8330JDDB#TRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
LT8330HDDB#TRMPBF	LT8330HDDB#TRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8330JS6#WTRMPBF	LT8330JS6#WTRPBF	LTGMQ	6-Lead Plastic TSOT-23	–40°C to 150°C
LT8330EDDB#WTRMPBF	LT8330EDDB#WTRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8330IDDB#WTRMPBF	LT8330IDDB#WTRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8330JDDB#WTRMPBF	LT8330JDDB#WTRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
LT8330HDDB#WTRMPBF	LT8330HDDB#WTRPBF	LGRC	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Contact the factory for parts specified with wider operating temperature ranges.
Contact the factory for information on lead based finish parts.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, EN/UVLO = 12V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range		●	3		40	V
V_{IN} Quiescent Current at Shutdown	$V_{EN/UVLO}$ = 0.2V	 ●		0.9 2	2 5	µA µA
	$V_{EN/UVLO}$ = 1.5V	 ●		2 3.6	5 9.5	µA µA
V_{IN} Quiescent Current	Sleep Mode, Not Switching	 ●		5.5 8.5	10 15	µA µA
	Active Mode, Not Switching	 ●		780 840	1100 1200	µA µA
FBX Regulation						
FBX Regulation Voltage	FBX > 0V FBX < 0V	● ●	1.568 –0.820	1.6 –0.80	1.632 –0.780	V V
FBX Line Regulation	FBX > 0V, 3V < V_{IN} < 40V FBX < 0V, 3V < V_{IN} < 40V			0.005 0.005	0.015 0.015	%/V %/V
FBX Pin Current	FBX = 1.6V, –0.8V	●	–10		10	nA
Oscillator						
Switching Frequency (f_{OSC})	V_{IN} = 24V	●	1.85	2.0	2.15	MHz
Minimum On-Time	V_{IN} = 24V			65	105	ns
Minimum Off-Time	V_{IN} = 24V			47	65	ns
Switch						
Maximum Switch Current Limit Threshold		●	1.0	1.2	1.4	A
Switch $R_{DS(ON)}$	I_{SW} = 0.5A			330		mΩ
Switch Leakage Current	V_{SW} = 60V			0.1	1	µA
EN/UVLO Logic						
EN/UVLO Pin Threshold (Rising)	Start Switching	●	1.620	1.68	1.745	V
EN/UVLO Pin Threshold (Falling)	Stop Switching	●	1.556	1.60	1.644	V
EN/UVLO Pin Current	$V_{EN/UVLO}$ = 1.6V	●	–40		100	nA
Soft-Start						
Soft-Start Time	V_{IN} = 24V			1		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: $INTV_{CC}$ cannot be externally driven. No additional components or loading is allowed on this pin.

Note 3: The LT8330E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8330I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8330J and LT8330H are guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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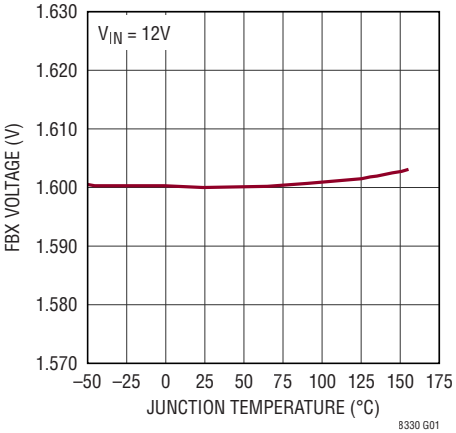
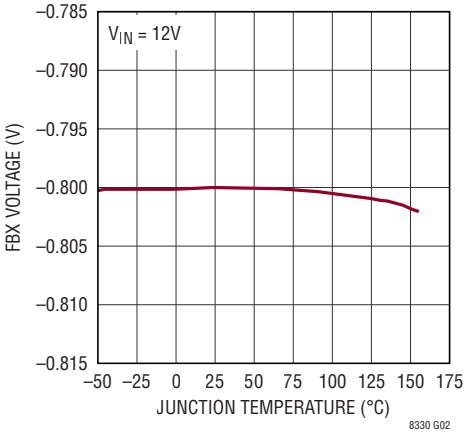
TYPICAL PERFORMANCE CHARACTERISTICS

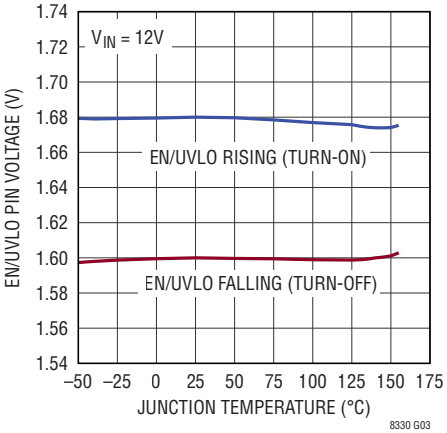
FBX Positive Regulation Voltage vs Temperature



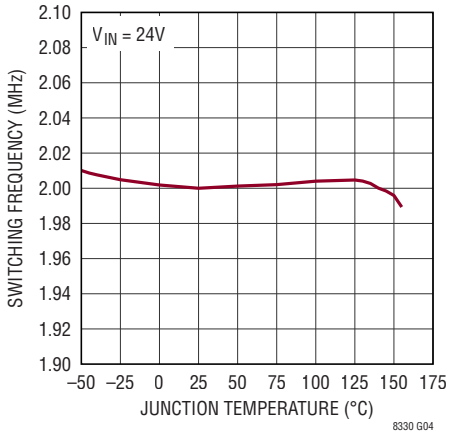
FBX Negative Regulation Voltage vs Temperature



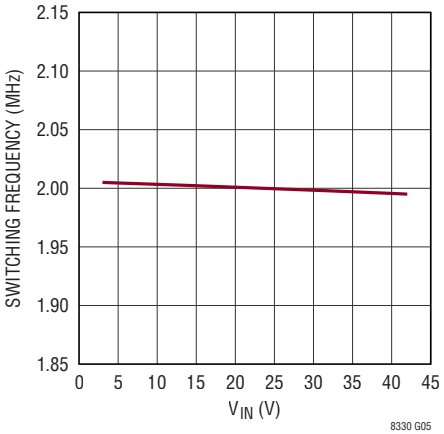
EN/UVLO Pin Thresholds vs Temperature



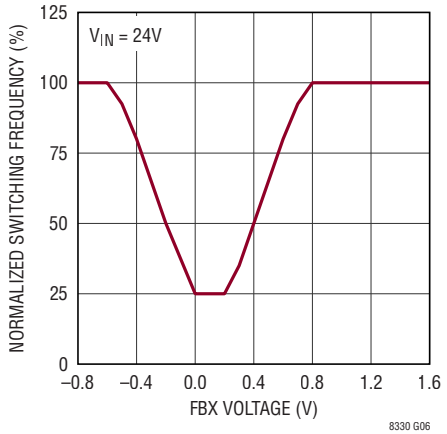
Switching Frequency vs Temperature



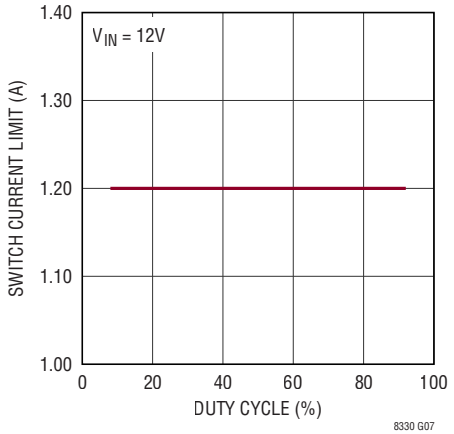
Switching Frequency vs V_{IN}



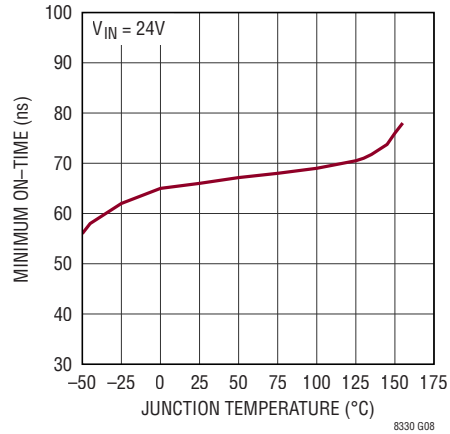
Normalized Switching Frequency vs FBX Voltage



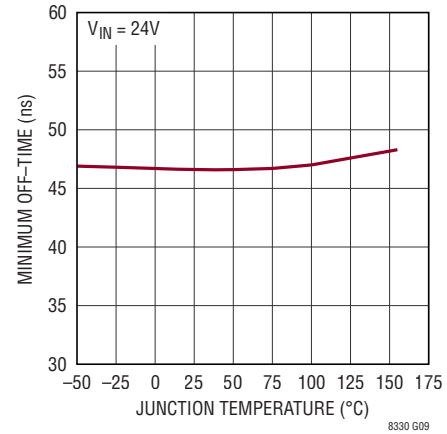
Switch Current Limit vs Duty Cycle



Switch Minimum On-Time vs Temperature



Switch Minimum Off-Time vs Temperature



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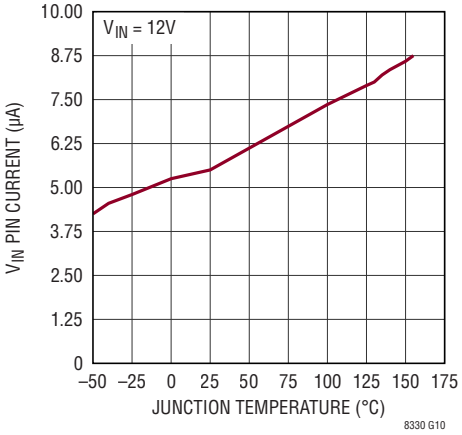
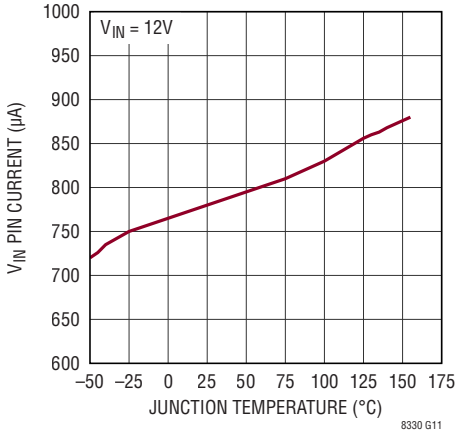
TYPICAL PERFORMANCE CHARACTERISTICS

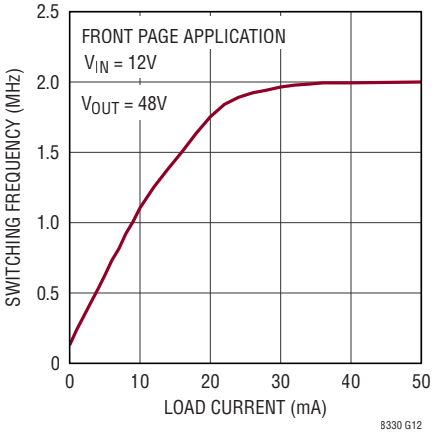
V_{IN} Pin Current (Sleep Mode, Not Switching) vs Temperature



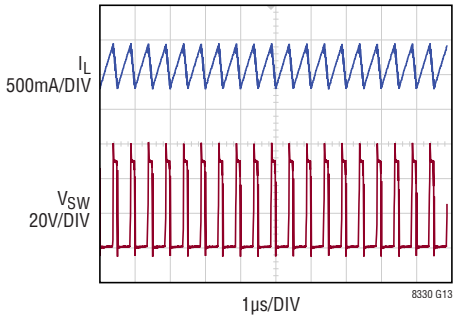
V_{IN} Pin Current (Active Mode, Not Switching) vs Temperature



Burst Frequency vs Load Current

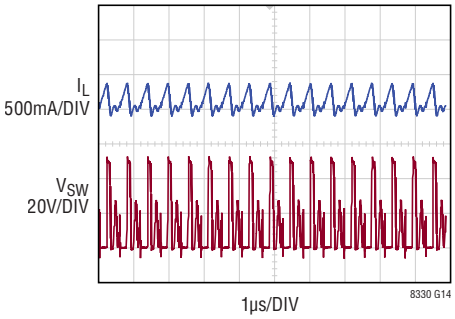


Switching Waveforms (in CCM)



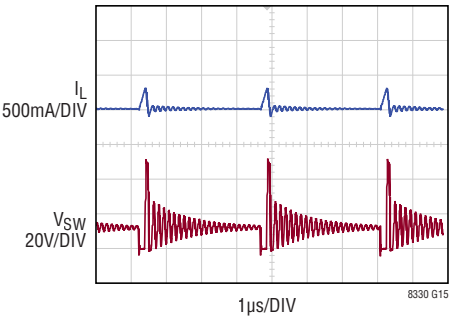
FRONT PAGE APPLICATION
V_{IN} = 12V, V_{OUT} = 48V, I_{LOAD} = 135mA

Switching Waveforms (in DCM/Light Burst Mode)



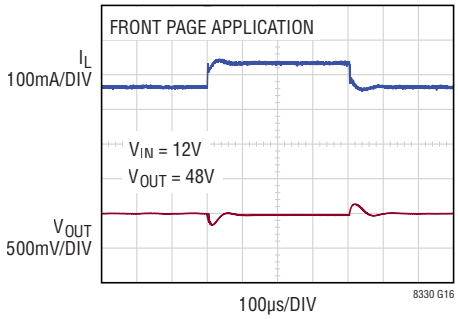
FRONT PAGE APPLICATION
V_{IN} = 12V, V_{OUT} = 48V, I_{LOAD} = 20mA

Switching Waveforms (in Deep Burst Mode)

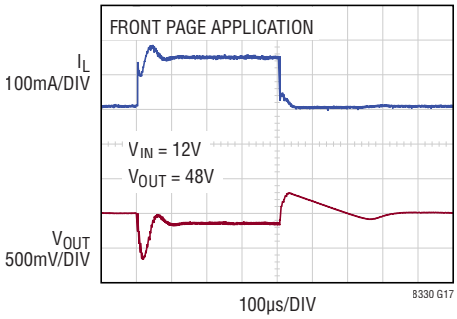


FRONT PAGE APPLICATION
V_{IN} = 12V, V_{OUT} = 48V, I_{LOAD} = 2mA

V_{OUT} Transient Response: Load Current Transients from 67.5mA to 135mA to 67.5mA



V_{OUT} Transient Response: Load Current Transients from 5mA to 135mA to 5mA



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PIN FUNCTIONS

EN/UVLO: Shutdown and Undervoltage Detect Pin. The LT8330 is shut down when this pin is low and active when this pin is high. Below an accurate 1.6V threshold the part enters undervoltage lockout and stops switching. This allows an undervoltage lockout (UVLO) threshold to be programmed for system input voltage by resistively dividing down system input voltage to the EN/UVLO pin. An 80mV pin hysteresis ensures part switching resumes when the pin exceeds 1.68V. EN/UVLO pin voltage below 0.2V reduces V_{IN} current below 1µA. If shutdown and UVLO features are not required, the pin can be tied directly to system input.

FBX: Voltage Regulation Feedback Pin for Positive or Negative Outputs. Connect this pin to a resistor divider between the output and GND. FBX reduces the switching frequency during start-up and fault conditions when FBX is close to GND.

GND: Ground Connection for the LT8330. The DFN package has the best thermal performance due to an exposed pad (Pin 9) on the bottom of the package. This exposed pad must be soldered to a ground plane. Pin 5 of the DFN package (and Pin 2 of the TSOT package) should also be connected to a ground plane. The ground plane should be connected to large copper layers to spread heat dissipated by the LT8330.

$INTV_{CC}$: Regulated 3V Supply for Internal Loads. The $INTV_{CC}$ pin must be bypassed with a minimum 1µF low ESR ceramic capacitor to ground. No additional components or loading is allowed on this pin.

NC: No Internal Connection. Tie directly to local ground.

SW: The Output of Internal Power Switch. Minimize the metal trace area connected to this pin to reduce EMI.

V_{IN}: Input Supply. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pin, and the negative terminal as close as possible to the GND pin.

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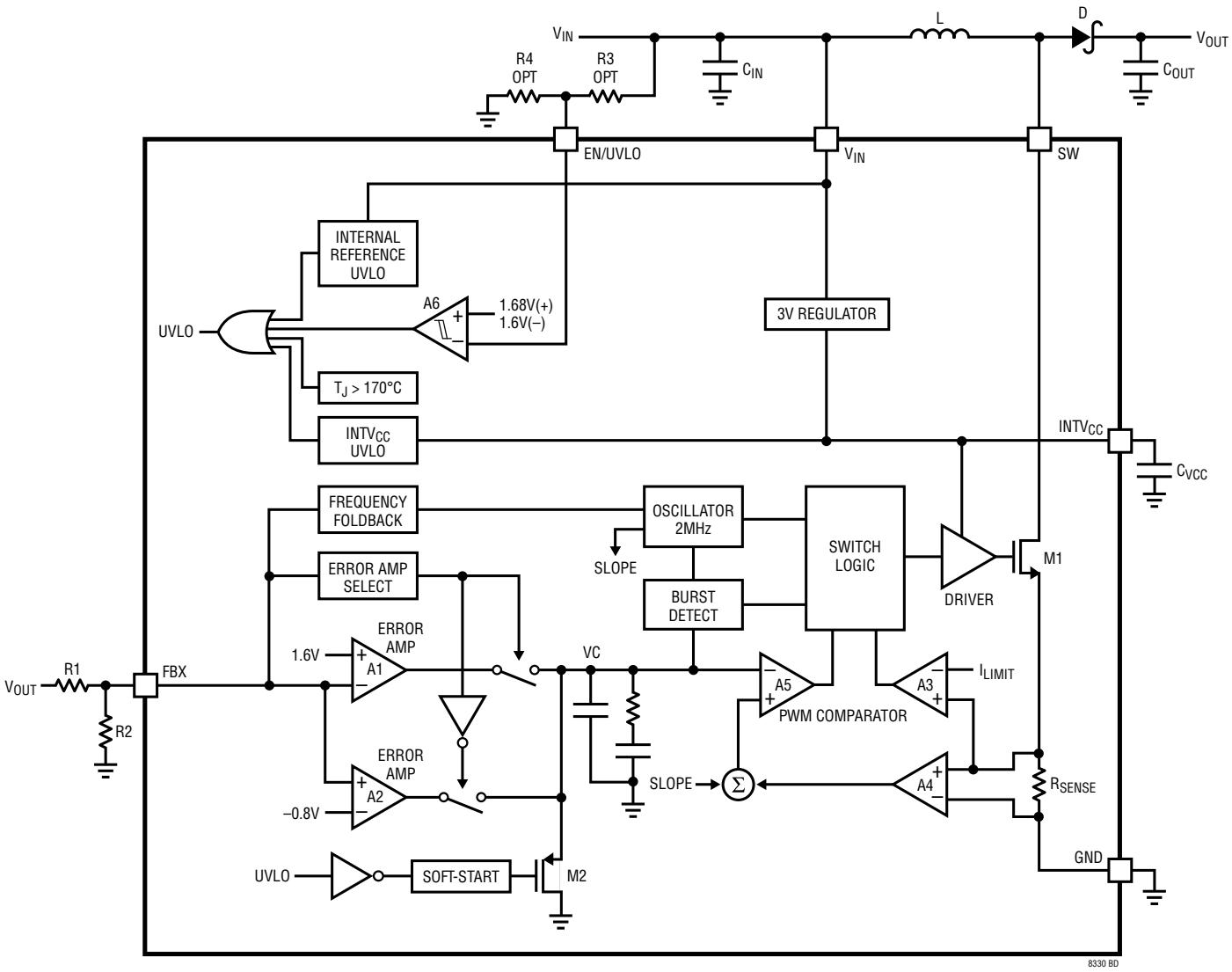
BLOCK DIAGRAM



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OPERATION

The LT8330 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram. An internal 2MHz oscillator turns on the internal power switch at the beginning of each clock cycle. Current in the inductor then increases until the current comparator trips and turns off the power switch. The peak inductor current at which the switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the FBX pin with an internal reference voltage (1.60V or –0.80V, depending on the chosen topology). When the load current increases it causes a reduction in the FBX pin voltage relative to the internal reference. This causes the error amplifier to increase the VC voltage until the new load current is satisfied. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT8330 is capable of generating either a positive or negative output voltage with a single FBX pin. It can be configured as a boost or SEPIC converter to generate a positive output voltage, or as an inverting converter to generate a negative output voltage. When configured as a boost converter, as shown in the Block Diagram, the FBX pin is pulled up to the internal bias voltage of 1.60V by a voltage divider (R1 and R2) connected from V_{OUT} to GND. Amplifier A2 becomes inactive and amplifier A1 performs (inverting) amplification from FBX to VC. When the LT8330 is in an inverting configuration, the FBX pin is pulled down to –0.80V by a voltage divider from V_{OUT} to GND. Amplifier A1 becomes inactive and amplifier A2 performs (non-inverting) amplification from FBX to VC.

If the EN/UVLO pin voltage is below 1.6V, the LT8330 enters undervoltage lockout (UVLO), and stops switching. When the EN/UVLO pin voltage is above 1.68V (typical), the LT8330 resumes switching. If the EN/UVLO pin voltage is below 0.2V, the LT8330 only draws 1µA from V_{IN}.

To optimize efficiency at light loads, the LT8330 operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 6µA.

APPLICATIONS INFORMATION

ACHIEVING ULTRALOW QUIESCENT CURRENT

To enhance efficiency at light loads the LT8330 uses a low ripple Burst Mode architecture. This keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output ripple. In Burst Mode operation the LT8330 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8330 consumes only 6µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8330 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load. The largest contributor to leakage current can be due to the reverse biased leakage of the Schottky diode (see Diode Selection in the Applications Information section).

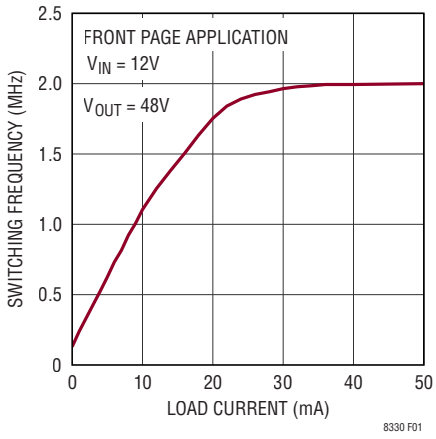

Figure 1. Burst Frequency vs Load Current

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APPLICATIONS INFORMATION

While in Burst Mode operation the current limit of the switch is approximately 240mA resulting in the output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As the output load ramps upward from zero the switching frequency will increase but only up to the fixed 2MHz defined by the internal oscillator as shown in Figure 1. The output load at which the LT8330 reaches the fixed 2MHz frequency varies based on input voltage, output voltage, and inductor choice.

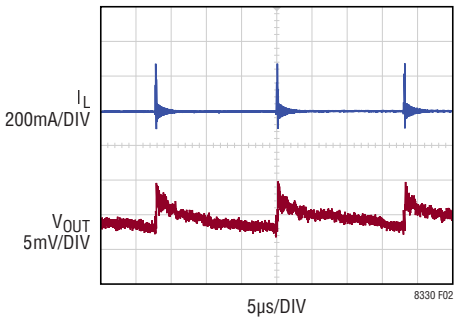

Figure 2. Burst Mode Operation

PROGRAMMING INPUT TURN-ON AND TURN-OFF THRESHOLDS WITH EN/UVLO PIN

The EN/UVLO pin voltage controls whether the LT8330 is enabled or is in a shutdown state. A 1.6V reference and a comparator A6 with built-in hysteresis (typical 80mV) allow the user to accurately program the system input voltage at which the IC turns on and off (see the Block Diagram). The typical input falling and rising threshold voltages can be calculated by the following equations:

$$V_{IN(FALLING,UVLO(-))} = 1.60 \bullet (R3+R4)/R4$$

$$V_{IN(RISING,\ UVLO(+))} = 1.68 \bullet (R3+R4)/R4$$

V_{IN} current is reduced below 1µA when the EN/UVLO pin voltage is less than 0.2V. The EN/UVLO pin can be connected directly to the input supply V_{IN} for always-enabled operation. A logic input can also control the EN/UVLO pin.

When operating in Burst Mode operation for light load currents, the current through the R3 and R4 network can easily be greater than the supply current consumed by the LT8330. Therefore, R3 and R4 should be large enough to minimize their effect on efficiency at light loads.

$INTV_{CC}$ REGULATOR

A low dropout (LDO) linear regulator, supplied from V_{IN}, produces a 3V supply at the $INTV_{CC}$ pin. A minimum 1µF low ESR ceramic capacitor must be used to bypass the $INTV_{CC}$ pin to ground to supply the high transient currents required by the internal power MOSFET gate driver.

No additional components or loading is allowed on this pin. The $INTV_{CC}$ rising threshold (to allow soft start and switching) is typically 2.6V. The $INTV_{CC}$ falling threshold (to stop switching and reset soft start) is typically 2.5V.

DUTY CYCLE CONSIDERATION

The LT8330 minimum on-time, minimum off-time and switching frequency (f_{OSC}) define the allowable minimum and maximum duty cycles of the converter (see Minimum On-Time, Minimum Off-Time, and Switching Frequency in the Electrical Characteristics table).

Minimum Allowable Duty Cycle =
$$\text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

Maximum Allowable Duty Cycle =
$$1 - \text{Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$$

The required switch duty cycle range for a Boost converter operating in continuous conduction mode (CCM) can be calculated as:

$$D_{MIN} = 1 - V_{IN(MAX)}/(V_{OUT} + V_D)$$
$$D_{MAX} = 1 - V_{IN(MIN)}/(V_{OUT} + V_D)$$

where V_D is the diode forward voltage drop. If the above duty cycle calculations for a given application violate the minimum and/or maximum allowed duty cycles for the LT8330, operation in discontinuous conduction mode (DCM) might provide a solution. For the same V_{IN} and V_{OUT} levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid sub-harmonic oscillations and the right half plane zero (RHPZ). While DCM provides these benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

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APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE

The output voltage is programmed with a resistor divider from the output to the FBX pin. Choose the resistor values for a positive output voltage according to:

$$R1 = R2 \bullet (V_{OUT}/1.60V - 1)$$

Choose the resistor values for a negative output voltage according to:

$$R1 = R2 \bullet (|V_{OUT}|/0.80V - 1)$$

The locations of R1 and R2 are shown in the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

Higher-value FBX divider resistors result in the lowest input quiescent current and highest light-load efficiency. FBX divider resistors R1 and R2 are usually in the range from 25k to 1M. Most applications use a phase-lead capacitor from V_{OUT} to FBX in combination with high-value FBX divider resistors (see Compensation in the Applications Information section).

SOFT-START

The LT8330 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT8330 addresses this mechanism with an internal soft-start function. As shown in the Block Diagram, the soft-start function controls the ramp of the power switch current by controlling the ramp of VC through M2. This allows the output capacitor to be charged gradually toward its final value while limiting the start-up peak currents. Figure 3 shows the output voltage and supply current for the first page Typical Application. It can be seen that both the output voltage and supply current come up gradually.

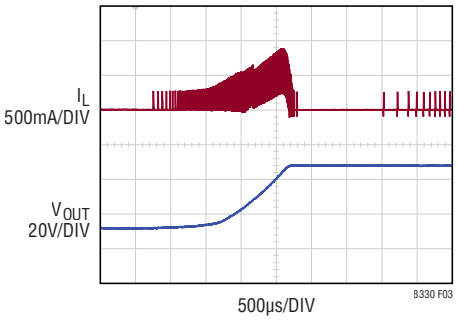

Figure 3. Soft-Start Waveforms

$INTV_{CC}$ undervoltage ($INTV_{CC}$ < 2.5V) and/or thermal lockout (T_J > 170°C) will immediately prevent switching, will reset the internal soft-start function and will pull down VC. Once all faults are removed, the LT8330 will soft-start VC and hence inductor peak current.

FREQUENCY FOLDBACK

During start-up or fault conditions in which V_{OUT} is very low, extremely small duty cycles may be required to maintain control of inductor peak current. The minimum on-time limitation of the power switch might prevent these low duty cycles from being achievable. In this scenario inductor current rise will exceed inductor current fall during each cycle, causing inductor current to 'walk up' beyond the switch current limit. The LT8330 provides protection from this by folding back switching frequency whenever FBX pin is close to GND (low V_{OUT} levels). This frequency foldback provides a larger switch-off time, allowing inductor current to fall enough each cycle (see Normalized Switching Frequency vs FBX Voltage in the Typical Performance Characteristics section).

THERMAL LOCKOUT

If the LT8330 die temperature reaches 170°C (typical), the part will stop switching and go into thermal lockout. When the die temperature has dropped by 5°C (nominal), the part will resume switching with a soft-started inductor peak current.

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APPLICATIONS INFORMATION

SWITCHING FREQUENCY AND INDUCTOR SELECTION

The LT8330 switches at 2MHz, allowing small value inductors to be used. 0.68µH to 10µH will usually suffice. Choose an inductor that can handle at least 1.4A without saturating, and ensure that the inductor has a low DCR (copper-wire resistance) to minimize I^2R power losses. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one-half of the total switch current. For better efficiency, use similar valued inductors with a larger volume. Many different sizes and shapes are available from various manufacturers. Choose a core material that has low losses at 2MHz, such as a ferrite core. The final value chosen for the inductor should not allow peak inductor currents to exceed 1A in steady state at maximum load. Due to tolerances, be sure to account for minimum possible inductance value, switching frequency and converter efficiency.

Table 1. Inductor Manufacturers

Sumida	(847) 956-0666	www.sumida.com
TDK	(847) 803-6100	www.tdk.com
Murata	(714) 852-2001	www.murata.com
Coilcraft	(847) 639-6400	www.coilcraft.com
Würth	(605) 886-4385	www.we-online.com

INPUT CAPACITOR

Bypass the input of the LT8330 circuit with a ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pins. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT8330 and will easily handle the ripple current. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

A precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8330. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8330 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8330's voltage rating. This situation is easily avoided (see Application Note 88).

OUTPUT CAPACITOR AND OUTPUT RIPPLE

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they are small and have extremely low ESR. Use X5R or X7R types. This choice will provide low output ripple and good transient response. A 4.7µF to 15µF output capacitor is sufficient for most applications, but systems with very low output currents may need only a 1µF or 2.2µF output capacitor. Solid tantalum or OS-CON capacitor can be used, but they will occupy more board area than a ceramic and will have a higher ESR. Always use a capacitor with a sufficient voltage rating.

COMPENSATION

The LT8330 is internally compensated. The decision to use either low ESR (ceramic) capacitors or the higher ESR (tantalum or OS-CON) capacitors, for the output capacitor, can affect the stability of the overall system. The ESR of any capacitor, along with the capacitance itself, contributes a zero to the system. For the tantalum and OS-CON capacitors, this zero is located at a lower frequency due to the higher value of the ESR, while the zero of a ceramic capacitor is at a much higher frequency and can generally be ignored.

A phase lead zero can be intentionally introduced by placing a capacitor in parallel with the resistor between V_{OUT} and FBX. By choosing the appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the phase margin of the overall converter. The typical target value for the zero frequency is between 30kHz to 60kHz.

A practical approach to compensation is to start with one of the circuits in this data sheet that is similar to your application. Optimize performance by adjusting the output capacitor and/or the feed forward capacitor (connected across the feedback resistor from output to FBX pin).

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APPLICATIONS INFORMATION

CERAMIC CAPACITORS

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8330 due to their piezoelectric nature. When in Burst Mode operation, the LT8330's switching frequency depends on the load current, and at very light loads the LT8330 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8330 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output. Low noise ceramic capacitors are also available.

Table 2. Ceramic Capacitor Manufacturers

Taiyo Yuden	(408) 573-4150	www.t-yuden.com
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com

DIODE SELECTION

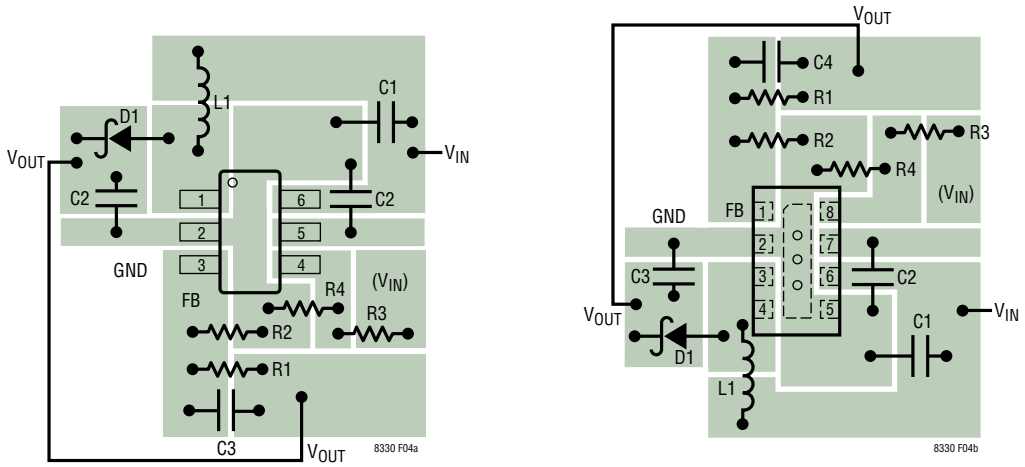
A Schottky diode is recommended for use with the LT8330. Low leakage Schottky diodes are necessary when low quiescent current is desired at low loads. The diode leakage appears as an equivalent load at the output and should be minimized. Choose Schottky diodes with sufficient reverse voltage ratings for the target applications.

Table 3. Recommended Schottky Diodes

PART NUMBER	AVERAGE FORWARD CURRENT (mA)	REVERSE VOLTAGE (V)	REVERSE CURRENT (µA)	MANUFACTURER
PMEG6010CEJ	≤1000	≤60	50	NXP
PMEG6030EP	≤3000	≤60	200	NXP

LAYOUT HINTS

The high speed operation of the LT8330 demands careful attention to board layout. Careless layout will result in performance degradation. Figure 4a shows the recommended component placement for the ThinSOT package. Figure 4b shows the recommended component placement for the DFN package. Note the vias under the exposed pad. These should connect to a local ground plane for better thermal performance.



(a) (b)

Figure 4. Suggested Layout – (a) ThinSOT, (b) DFN

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APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8330. The DFN package has the best thermal performance due to an exposed pad (Pin 9) on the bottom of the package. This exposed pad must be soldered to a ground plane. Pin 5 of the DFN package (and Pin 2 of the TSOT package) should also be connected to a ground plane. The ground plane should be connected to large copper layers to spread heat dissipated by the LT8330 and to further reduce the thermal resistance (θ_{JA}) values listed in the Pin Configuration section. Power dissipation within the LT8330 (P_{DISS_LT8330}) can be estimated by subtracting the inductor and Schottky diode power losses from the total power losses calculated in an efficiency measurement. The junction temperature of LT8330 can then be estimated by,

$$T_J\ (LT8330) = T_A + \theta_{JA} \bullet P_{DISS_LT8330}$$

ADDITIONAL TOPOLOGIES : SEPIC AND INVERTING

In addition to the Boost topology, the LT8330 can be configured in a SEPIC or Inverting topology. SEPIC and Inverting converters are analyzed below.

SEPIC CONVERTER APPLICATIONS

The LT8330 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 5. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1 - D}$$

in continuous conduction mode (CCM).

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter operates at the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_{OUT} + V_D}$$

Be sure to check that D_{MAX} and D_{MIN} obey:

$D_{MAX} < 1\text{-Minimum Off-Time}_{(MAX)} \bullet f_{OSC(MAX)}$

and

$D_{MIN} > \text{Minimum On-Time}_{(MAX)} \bullet f_{OSC(MAX)}$

where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in the Electrical Characteristics table.

SEPIC Converter: The Maximum Output Current Capability and Inductor Selection

As shown in Figure 5, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can

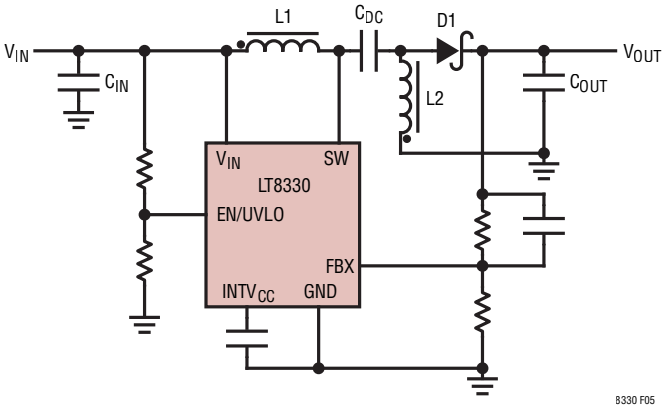

Figure 5. LT8330 Configured in a SEPIC Topology

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APPLICATIONS INFORMATION

also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)(AVE)} = I_{IN(MAX)(AVE)} = I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

$$I_{L2(MAX)(AVE)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to I_{L1} + I_{L2} when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)(AVE)} = I_{L1(MAX)(AVE)} + I_{L2(MAX)(AVE)}$$

$$= I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to $I_{SW(MAX)(AVE)}$, as shown in Figure 6. Then, the switch ripple current ΔI_{SW} can be calculated by:

$$\Delta I_{SW} = \chi \bullet I_{SW(MAX)(AVE)}$$

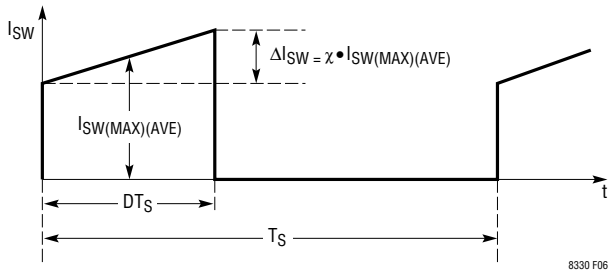

Figure 6. The Switch Current Waveform of the SEPIC Converter

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \bullet \Delta I_{SW}$$

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.2 to 0.6.

Due to the current limit of its internal power switch, the LT8330 should be used in a SEPIC converter whose maximum output current ($I_{O(MAX)}$) is less than the output current capability by a sufficient margin (10% or higher is recommended):

$$I_{O(MAX)} < (1 - D_{MAX}) \bullet (1A - 0.5 \bullet \Delta I_{SW}) \bullet (0.9)$$

Given an operating input voltage range, and having chosen ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \bullet \Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1µH to 47µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{OSC}} \bullet D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \bullet \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \bullet \Delta I_{L2}$$

The maximum RMS inductor currents are approximately equal to the maximum average inductor currents.

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APPLICATIONS INFORMATION

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current.

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

where V_D is diode's forward voltage drop, and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 5) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

INVERTING CONVERTER APPLICATIONS

The LT8330 can be configured as a dual-inductor inverting topology, as shown in Figure 7. The V_{OUT} to V_{IN} ratio is:

$$\frac{V_{OUT} - V_D}{V_{IN}} = -\frac{D}{1-D}$$

in continuous conduction mode (CCM).

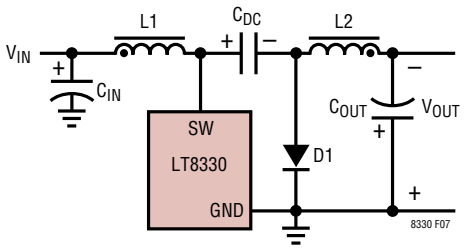

Figure 7. A Simplified Inverting Converter

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MIN)}}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage :

$$D_{MIN} = \frac{|V_{OUT}| + V_D}{|V_{OUT}| + V_D + V_{IN(MAX)}}$$

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APPLICATIONS INFORMATION

Be sure to check that D_{MAX} and D_{MIN} obey :

D_{MAX} < 1-Minimum Off-Time$_{(MAX)}$ • $f_{OSC(MAX)}$

and

D_{MIN} > Minimum On-Time$_{(MAX)}$ • $f_{OSC(MAX)}$

where Minimum Off-Time, Minimum On-Time and f_{OSC} are specified in the Electrical Characteristics table.

Inverting Converter: Inductor, Output Diode and Input Capacitor Selections

The selections of the inductor, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 7) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

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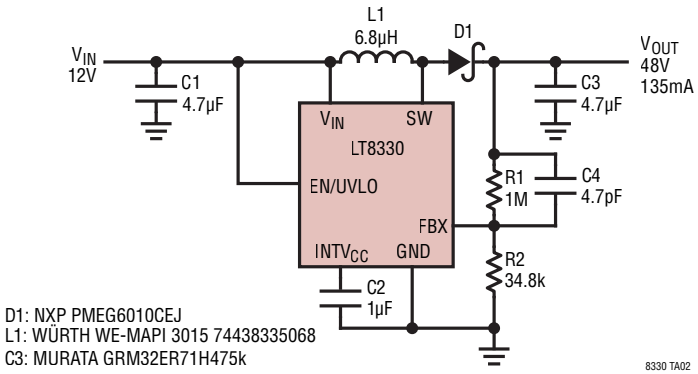
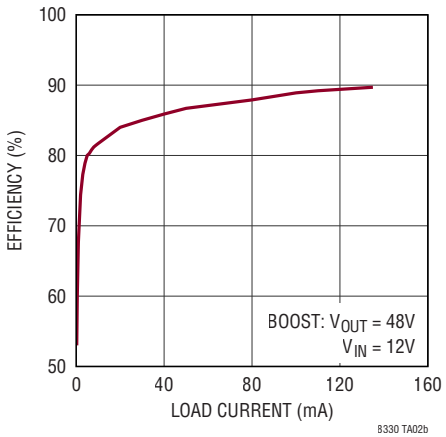
TYPICAL APPLICATIONS

48V Boost Converter

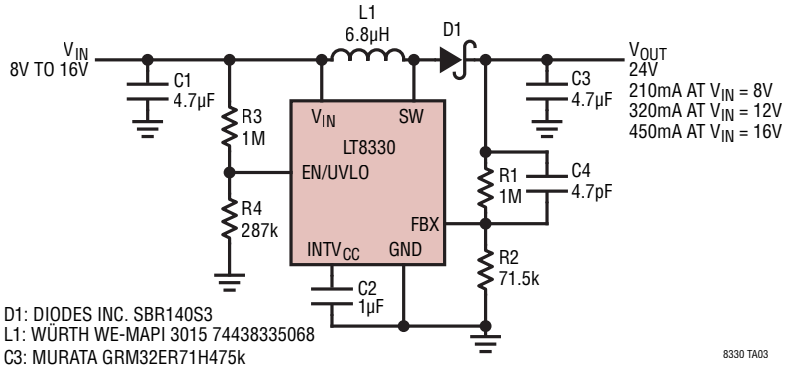


D1: NXP PMEG6010CEJ
L1: WÜRTH WE-MAPI 3015 74438335068
C3: MURATA GRM32ER71H475k

Efficiency

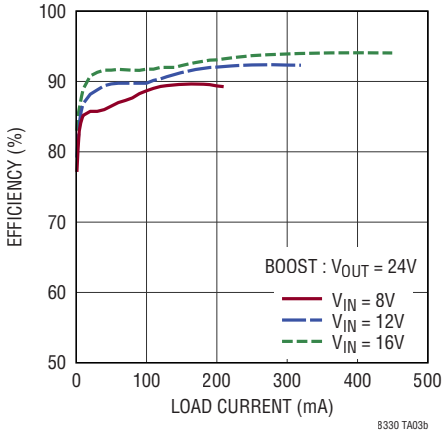


8V to 16V Input, 24V Boost Converter

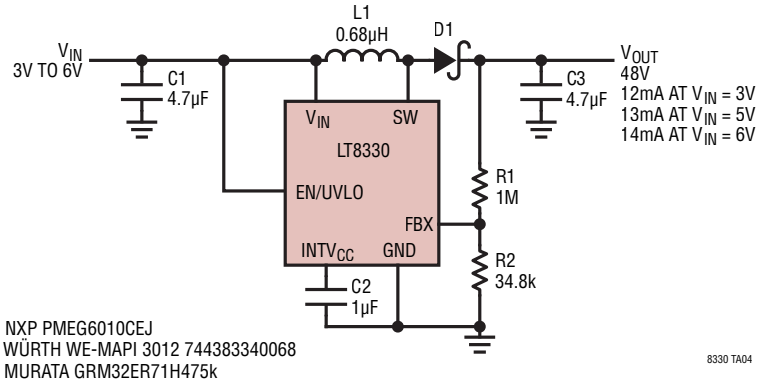


D1: DIODES INC. SBR140S3
L1: WÜRTH WE-MAPI 3015 74438335068
C3: MURATA GRM32ER71H475k

Efficiency

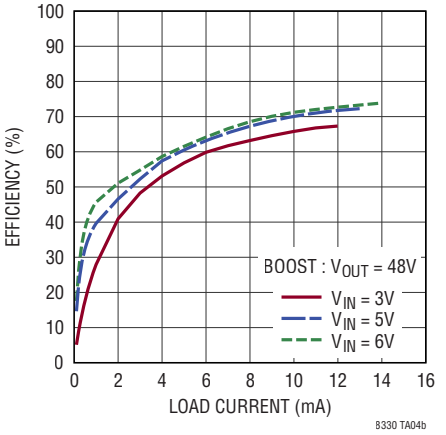


3V to 6V Input, 48V Boost Converter



D1: NXP PMEG6010CEJ
L1: WÜRTH WE-MAPI 3012 744383340068
C3: MURATA GRM32ER71H475k

Efficiency



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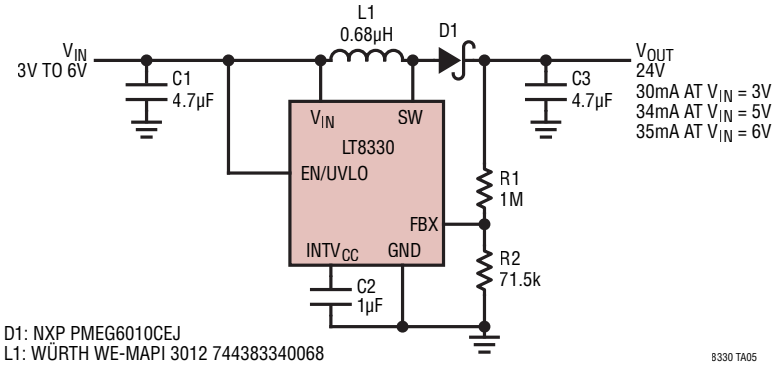
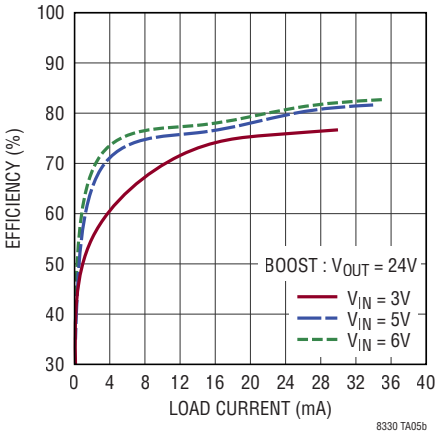
TYPICAL APPLICATIONS

3V to 6V Input, 24V Boost Converter

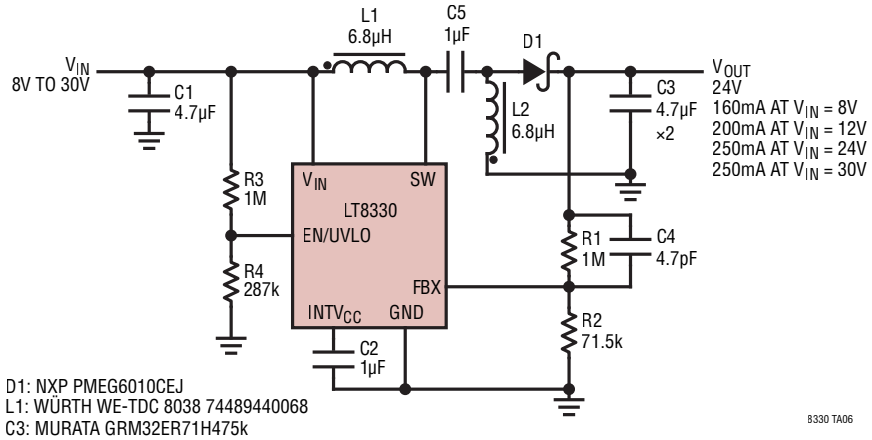


D1: NXP PMEG6010CEJ
L1: WÜRTH WE-MAPI 3012 744383340068
C3: MURATA GRM32ER71H475k

Efficiency

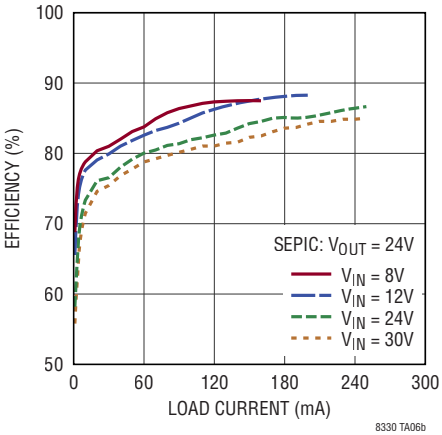


8V to 30V Input, 24V SEPIC Converter



D1: NXP PMEG6010CEJ
L1: WÜRTH WE-TDC 8038 74489440068
C3: MURATA GRM32ER71H475k

Efficiency



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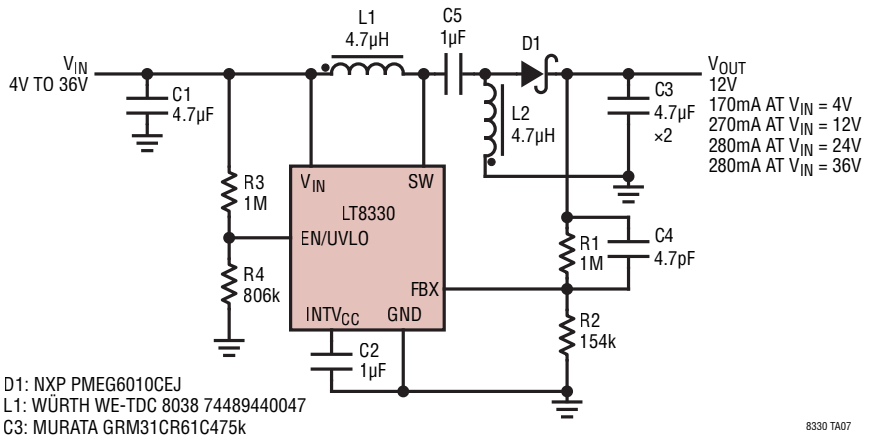
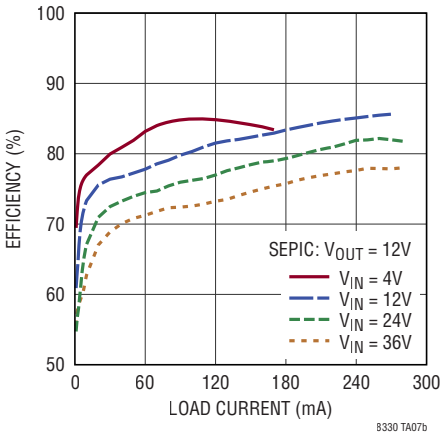
TYPICAL APPLICATIONS

4V to 36V Input, 12V SEPIC Converter

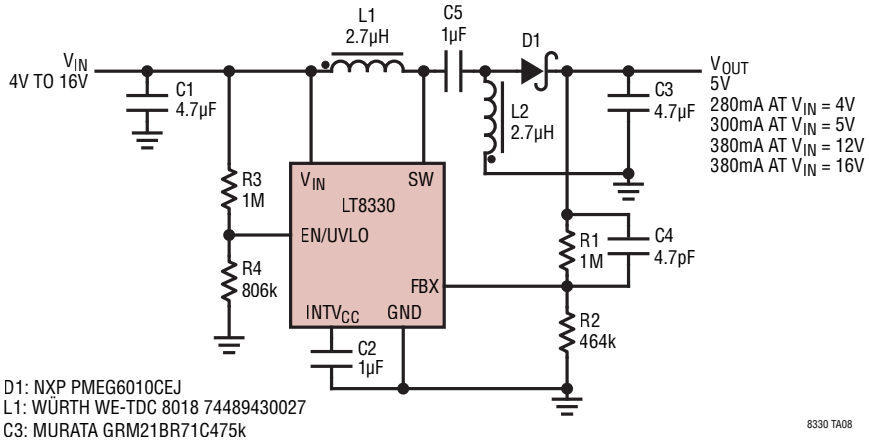


D1: NXP PMEG6010CEJ
L1: WÜRTH WE-TDC 8038 74489440047
C3: MURATA GRM31CR61C475k

Efficiency

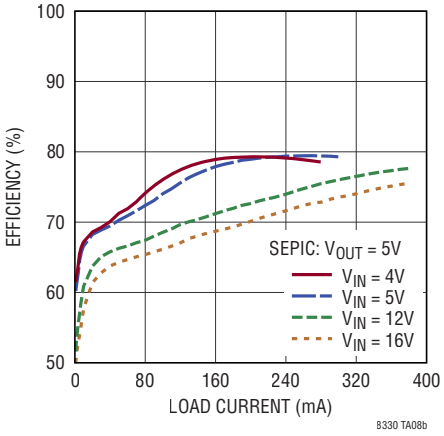


4V to 16V Input, 5V SEPIC Converter



D1: NXP PMEG6010CEJ
L1: WÜRTH WE-TDC 8018 74489430027
C3: MURATA GRM21BR71C475k

Efficiency



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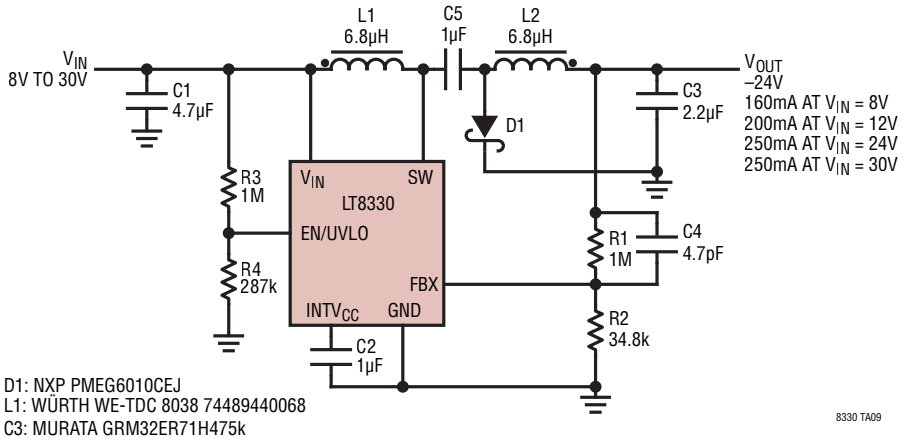
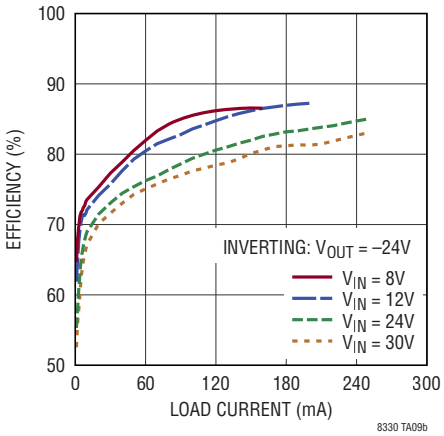
TYPICAL APPLICATIONS

8V to 30V Input, –24V Inverting Converter

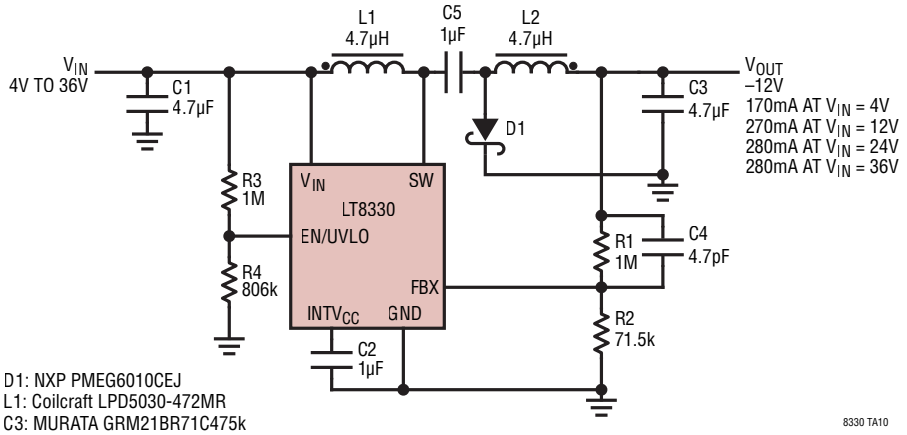


D1: NXP PMEG6010CEJ
L1: WÜRTH WE-TDC 8038 74489440068
C3: MURATA GRM32ER71H475k

Efficiency

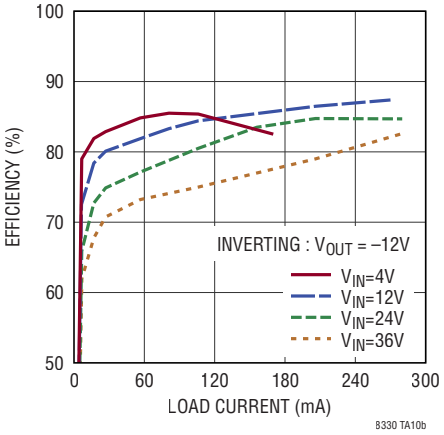


4V to 36V Input, –12V Inverting Converter

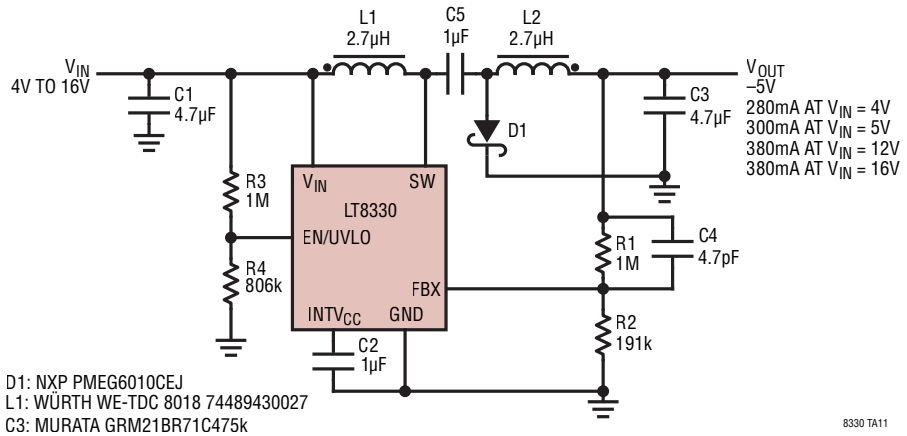


D1: NXP PMEG6010CEJ
L1: Coilcraft LPD5030-472MR
C3: MURATA GRM21BR71C475k

Efficiency

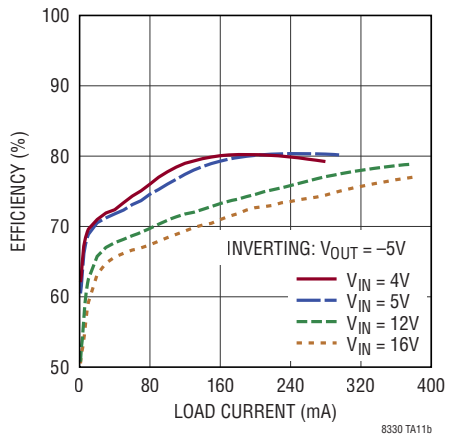


4V to 16V Input, –5V Inverting Converter



D1: NXP PMEG6010CEJ
L1: WÜRTH WE-TDC 8018 74489430027
C3: MURATA GRM21BR71C475k

Efficiency



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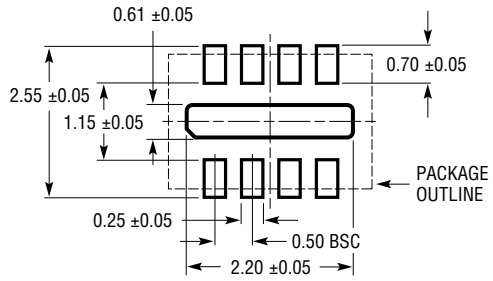
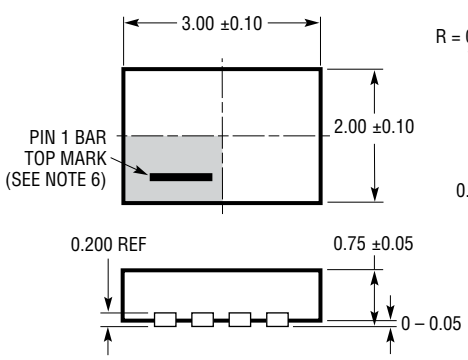
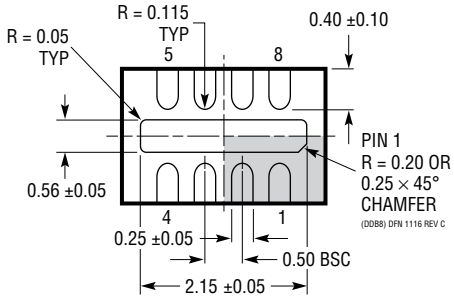
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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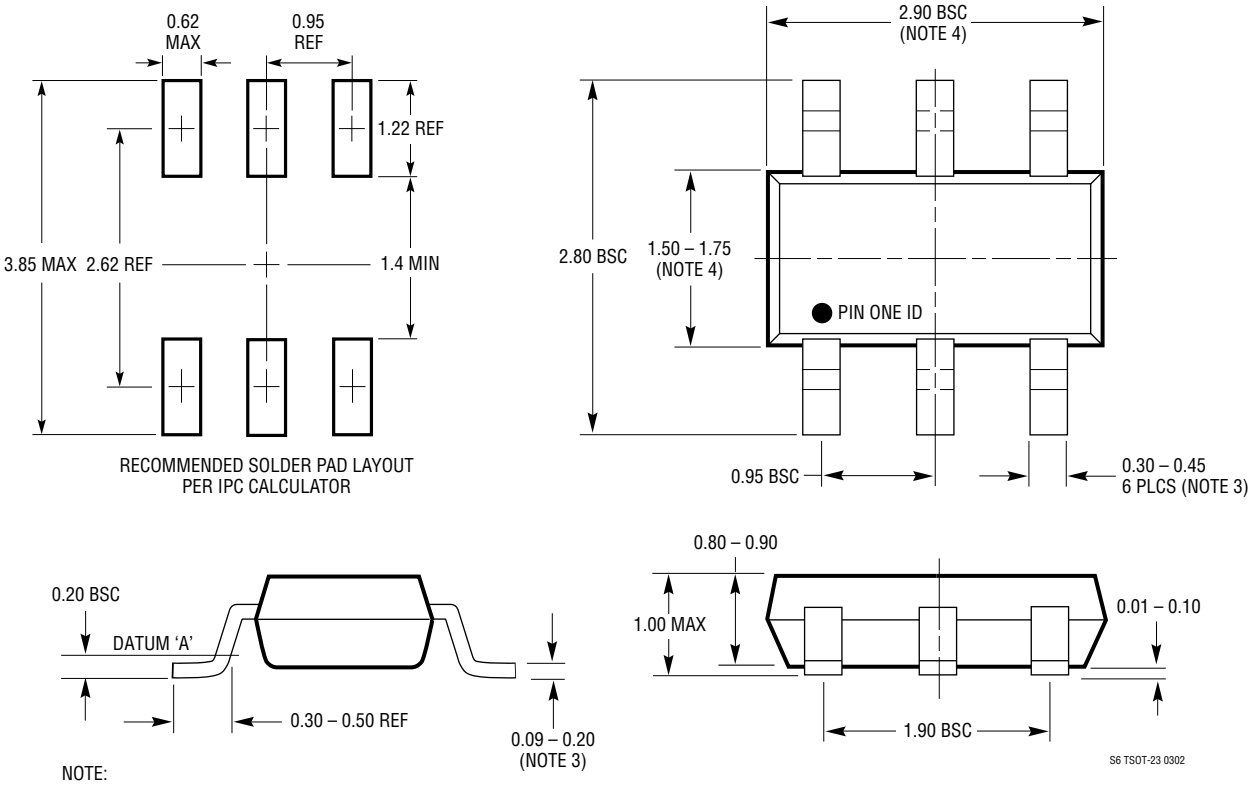
PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/16	Corrected V_{IN} Quiescent Current.	3
		Corrected Typographic Errors.	2, 22, 23
B	09/19	Added automotive models.	2
		Updated Equations in Inverting Converter Applications.	15
C	04/21	Updated description.	1
		Added J-Grade.	2, 3
		Changed EN/UVLO Pin Current spec from 40nA to 100nA.	3

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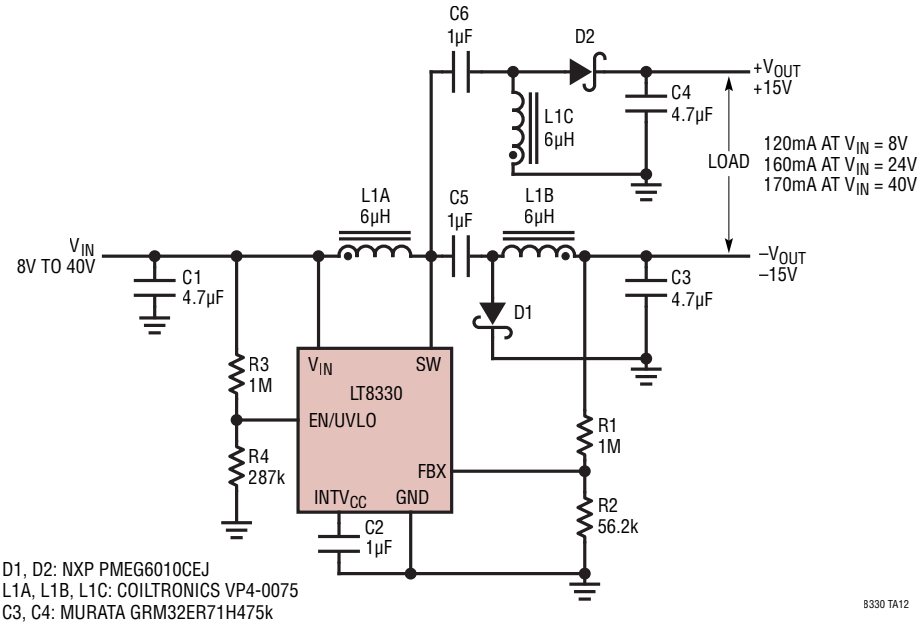
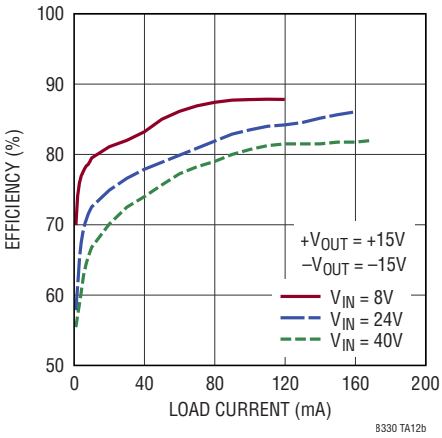
TYPICAL APPLICATION

8V to 40V Input, ±15V Converter



D1, D2: NXP PMEG6010CEJ
L1A, L1B, L1C: COILTRONICS VP4-0075
C3, C4: MURATA GRM32ER71H475k

Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1935	2A (I_{SW}), 40V, 1.2MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.3V to 16V, $V_{OUT(MAX)}$ = 38V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT Package
LT3467	1.1A (I_{SW}), 1.3MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.4V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} < 1µA, ThinSOT, 2mm × 3mm DFN Packages
LT3580	2A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN} = 2.5V to 32V, $V_{OUT(MAX)}$ = 42V, I_Q = 1mA, I_{SD} = <1µA, 3mm × 3mm DFN-8, MSOP-8E
LT8494	70V, 2A Boost/SEPIC 1.5MHz High Efficiency Step-Up DC/DC Converter	V_{IN} = 1V to 60V (2.5V to 32V Start-Up), $V_{OUT(MAX)}$ = 70V, I_Q = 3µA (Burst Mode operation), I_{SD} = <1µA, 20-Lead TSSOP
LT8570/LT8570-1	65V, 500mA/250mA Boost/Inverting DC/DC Converter	$V_{IN(MIN)}$ = 2.55V, $V_{IN(MAX)}$ = 40V, $V_{OUT(MAX)}$ = ±60V, I_Q = 1.2mA, I_{SD} = <1mA, 3mm × 3mm DFN-8, MSOP-8E
LT8580	1A (I_{SW}), 65V 1.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.55V to 40V, $V_{OUT(MAX)}$ = 65V, I_Q = 1.2mA, I_{SD} = <1µA, 3mm × 3mm DFN-8, MSOP-8E

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