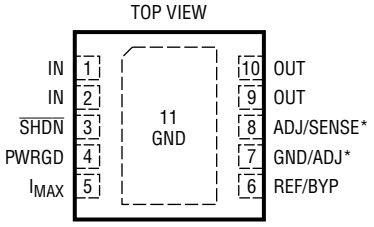
ABSOLUTE MAXIMUM RATINGS (Note 1)

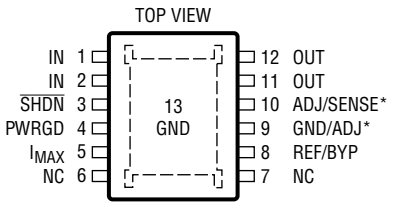
IN Pin Voltage ..... ±50V
OUT Pin Voltage ..... +40V, –50V
Input-to-Output Differential Voltage (Note 2) .. +50V, –40V
ADJ Pin Voltage ..... ±50V
SENSE Pin Voltage ..... ±50V
$\overline{SHDN}$ Pin Voltage ..... ±50V
PWRGD Pin Voltage ..... –0.3V, 50V
I_{MAX} Pin Voltage ..... –0.3V, 7V
REF/BYP Pin Voltage 1V

Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Notes 3, 5, 14)
E-, I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 150°C
H-Grade ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP Package Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 31°C/W, θ_{JC} = 9°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 28°C/W, θ_{JC} = 6°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

*Pin 7: GND for LT3065, ADJ for LT3065-1.2, LT3065-1.5, LT3065-1.8, LT3065-2.5, LT3065-3.3, LT3065-5

*Pin 8: ADJ for LT3065, SENSE for LT3065-1.2, LT3065-1.5, LT3065-1.8, LT3065-2.5, LT3065-3.3, LT3065-5

*Pin 9: GND for LT3065, ADJ for LT3065-1.2, LT3065-1.5, LT3065-1.8, LT3065-2.5, LT3065-3.3, LT3065-5

*Pin 10: ADJ for LT3065, SENSE for LT3065-1.2, LT3065-1.5, LT3065-1.8, LT3065-2.5, LT3065-3.3, LT3065-5

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3065EDD#PBF	LT3065EDD#TRPBF	LGKS	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD#PBF	LT3065IDD#TRPBF	LGKS	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065HDD#PBF	LT3065HDD#TRPBF	LGKS	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD#PBF	LT3065MPDD#TRPBF	LGKS	10-Lead (3mm x 3mm) Plastic DFN	–55°c to 150°C
LT3065EDD-1.2#PBF	LT3065EDD-1.2#TRPBF	LGQV	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD-1.2#PBF	LT3065IDD-1.2#TRPBF	LGQV	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065HDD-1.2#PBF	LT3065HDD-1.2#TRPBF	LGQV	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD-1.2#PBF	LT3065MPDD-1.2#TRPBF	LGQV	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3065EDD-1.5#PBF	LT3065EDD-1.5#TRPBF	LGQW	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD-1.5#PBF	LT3065IDD-1.5#TRPBF	LGQW	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065HDD-1.5#PBF	LT3065HDD-1.5#TRPBF	LGQW	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD-1.5#PBF	LT3065MPDD-1.5#TRPBF	LGQW	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3065EDD-1.8#PBF	LT3065EDD-1.8#TRPBF	LGQX	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD-1.8#PBF	LT3065IDD-1.8#TRPBF	LGQX	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C

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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3065HDD-1.8#PBF	LT3065HDD-1.8#TRPBF	LGQX	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD-1.8#PBF	LT3065MPDD-1.8#TRPBF	LGQX	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3065EDD-2.5#PBF	LT3065EDD-2.5#TRPBF	LGQY	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD-2.5#PBF	LT3065IDD-2.5#TRPBF	LGQY	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065HDD-2.5#PBF	LT3065HDD-2.5#TRPBF	LGQY	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD-2.5#PBF	LT3065MPDD-2.5#TRPBF	LGQY	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3065EDD-3.3#PBF	LT3065EDD-3.3#TRPBF	LGQZ	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD-3.3#PBF	LT3065IDD-3.3#TRPBF	LGQZ	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065HDD-3.3#PBF	LT3065HDD-3.3#TRPBF	LGQZ	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD-3.3#PBF	LT3065MPDD-3.3#TRPBF	LGQZ	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3065EDD-5#PBF	LT3065EDD-5#TRPBF	LGRB	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065IDD-5#PBF	LT3065IDD-5#TRPBF	LGRB	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3065HDD-5#PBF	LT3065HDD-5#TRPBF	LGRB	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3065MPDD-5#PBF	LT3065MPDD-5#TRPBF	LGRB	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3065EMSE#PBF	LT3065EMSE#TRPBF	3065	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE#PBF	LT3065IMSE#TRPBF	3065	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE#PBF	LT3065HMSE#TRPBF	3065	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE#PBF	LT3065MPMSE#TRPBF	3065	12-Lead Plastic MSOP	–55°C to 150°C
LT3065EMSE-1.2#PBF	LT3065EMSE-1.2#TRPBF	306512	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE-1.2#PBF	LT3065IMSE-1.2#TRPBF	306512	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE-1.2#PBF	LT3065HMSE-1.2#TRPBF	306512	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE-1.2#PBF	LT3065MPMSE-1.2#TRPBF	306512	12-Lead Plastic MSOP	–55°C to 150°C
LT3065EMSE-1.5#PBF	LT3065EMSE-1.5#TRPBF	306515	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE-1.5#PBF	LT3065IMSE-1.5#TRPBF	306515	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE-1.5#PBF	LT3065HMSE-1.5#TRPBF	306515	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE-1.5#PBF	LT3065MPMSE-1.5#TRPBF	306515	12-Lead Plastic MSOP	–55°C to 150°C
LT3065EMSE-1.8#PBF	LT3065EMSE-1.8#TRPBF	306518	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE-1.8#PBF	LT3065IMSE-1.8#TRPBF	306518	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE-1.8#PBF	LT3065HMSE-1.8#TRPBF	306518	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE-1.8#PBF	LT3065MPMSE-1.8#TRPBF	306518	12-Lead Plastic MSOP	–55°C to 150°C
LT3065EMSE-2.5#PBF	LT3065EMSE-2.5#TRPBF	306525	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE-2.5#PBF	LT3065IMSE-2.5#TRPBF	306525	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE-2.5#PBF	LT3065HMSE-2.5#TRPBF	306525	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE-2.5#PBF	LT3065MPMSE-2.5#TRPBF	306525	12-Lead Plastic MSOP	–55°C to 150°C
LT3065EMSE-3.3#PBF	LT3065EMSE-3.3#TRPBF	306533	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE-3.3#PBF	LT3065IMSE-3.3#TRPBF	306533	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE-3.3#PBF	LT3065HMSE-3.3#TRPBF	306533	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE-3.3#PBF	LT3065MPMSE-3.3#TRPBF	306533	12-Lead Plastic MSOP	–55°C to 150°C
LT3065EMSE-5#PBF	LT3065EMSE-5#TRPBF	30655	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE-5#PBF	LT3065IMSE-5#TRPBF	30655	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE-5#PBF	LT3065HMSE-5#TRPBF	30655	12-Lead Plastic MSOP	–40°C to 150°C
LT3065MPMSE-5#PBF	LT3065MPMSE-5#TRPBF	30655	12-Lead Plastic MSOP	–55°C to 150°C

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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**				
LT3065EMSE#WPBF	LT3065EMSE#WTRPBF	3065	12-Lead Plastic MSOP	–40°C to 125°C
LT3065IMSE#WPBF	LT3065IMSE#WTRPBF	3065	12-Lead Plastic MSOP	–40°C to 125°C
LT3065HMSE#WPBF	LT3065HMSE#WTRPBF	3065	12-Lead Plastic MSOP	–40°C to 150°C
LT3065IMSE-5#WPBF	LT3065IMSE-5#WTRPBF	30655	12-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 4, 9)	I_{LOAD} = 500mA	●		1.6	2.2	V
Regulated Output Voltage	LT3065-1.2: V_{IN} = 2.2V, I_{LOAD} = 1mA		1.188	1.2	1.212	V
	2.2V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	1.176		1.224	V
	LT3065-1.5: V_{IN} = 2.2V, I_{LOAD} = 1mA		1.485	1.5	1.515	V
	2.2V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	1.470		1.530	V
	LT3065-1.8: V_{IN} = 2.4V, I_{LOAD} = 1mA		1.782	1.8	1.818	V
	2.4V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	1.764		1.836	V
	LT3065-2.5: V_{IN} = 3.1V, I_{LOAD} = 1mA		2.475	2.5	2.525	V
	3.1V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	2.450		2.550	V
	LT3065-3.3: V_{IN} = 3.9V, I_{LOAD} = 1mA		3.267	3.3	3.333	V
	3.9V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	3.234		3.366	V
	LT3065-5: V_{IN} = 5.6V, I_{LOAD} = 1mA		4.950	5	5.050	V
	5.6V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	4.900		5.100	V
ADJ Pin Voltage (Notes 4, 5)	LT3065: V_{IN} = 2.2V, I_{LOAD} = 1mA		594	600	606	mV
	2.2V < V_{IN} < 45V, 1mA < I_{LOAD} < 500mA	●	588		612	mV
Line Regulation I_{LOAD} = 1mA	LT3065-1.2: ΔV_{IN} = 2.2V to 45V	●		0.7	7	mV
	LT3065-1.5: ΔV_{IN} = 2.2V to 45V	●		0.9	8.8	mV
	LT3065-1.8: ΔV_{IN} = 2.4V to 45V	●		1.1	10.5	mV
	LT3065-2.5: ΔV_{IN} = 3.1V to 45V	●		1.6	14.6	mV
	LT3065-3.3: ΔV_{IN} = 3.9V to 45V	●		2.0	19.3	mV
	LT3065-5: ΔV_{IN} = 5.6V to 45V	●		3.1	29.2	mV
	LT3065: ΔV_{IN} = 2.2V to 45V (Note 4)	●		0.1	3	mV
Load Regulation ΔI_{LOAD} = 1mA to 500mA	LT3065-1.2, V_{IN} = 2.2V	●		0.5	8	mV
	LT3065-1.5, V_{IN} = 2.2V	●		0.7	10	mV
	LT3065-1.8, V_{IN} = 2.4V	●		0.9	12	mV
	LT3065-2.5 V_{IN} = 3.1V	●		1.2	16.7	mV
	LT3065-3.3, V_{IN} = 3.9V	●		1.6	11	mV
	LT3065-5, V_{IN} = 5.6V	●		2.4	33.4	mV
	LT3065, V_{IN} = 2.2V (Note 4)	●		0.1	4	mV
Dropout Voltage, V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 6, 7)	I_{LOAD} = 10mA			110	150	mV
		●			210	mV
	I_{LOAD} = 50mA			145	200	mV
		●			310	mV
	I_{LOAD} = 100mA			175	220	mV
		●			330	mV
	I_{LOAD} = 500mA			300	350	mV
		●			510	mV
GND Pin Current, V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V (Notes 7, 8)	I_{LOAD} = 0mA	●		55	110	µA
	I_{LOAD} = 1mA	●		100	200	µA
	I_{LOAD} = 10mA	●		270	550	µA
	I_{LOAD} = 100mA	●		1.8	4.5	mA
	I_{LOAD} = 500mA	●		11	25	mA
Quiescent Current in Shutdown	V_{IN} = 45V, $V_{\overline{SHDN}}$ = 0V			0.2	1	µA
ADJ Pin Bias Current (Notes 4, 10)	V_{IN} = 2.2V	●		16	60	nA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 500mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			90		μV_{RMS}
	C_{OUT} = 10µF, C_{BYP} = 10nF, I_{LOAD} = 500mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			25		μV_{RMS}
Shutdown Threshold	V_{OUT} = Off to On	●		1. 3	1.42	V
	V_{OUT} = On to Off	●	0.9	1.1		V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 3).

$\overline{SHDN}$ Pin Current (Note 11)	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 45V $V_{\overline{SHDN}}$ = 45V, V_{IN} = 45V	● ●		 0.5	±1 3	µA µA
Ripple Rejection $V_{IN} - V_{OUT}$ = 2V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA	LT3065-1.2 LT3065-1.5 LT3065-1.8 LT3065-2.5 LT3065-3.3 LT3065-5 LT3065		63 63 59 57 56 55 70	78 78 74 72 71 70 85		dB dB dB dB dB dB dB
Input Reverse Leakage Current	V_{IN} = –45V, V_{OUT} = 0	●			300	µA
Reverse Output Current (Note 12)	V_{OUT} = 1.2V, V_{IN} = $V_{\overline{SHDN}}$ = 0			0	10	µA
Internal Current Limit (Note 4)	V_{IN} = 2.2V, V_{OUT} = 0, V_{IMAX} = 0 V_{IN} = 2.2V, ΔV_{OUT} = –5%	 ●	 520	900		mA mA
External Programmed Current Limit (Notes 7, 13)	5.6V < V_{IN} < 10V, V_{OUT} = 95% of V_{OUT} (Nominal), R_{IMAX} = 1.5k 5.6V < V_{IN} < 7V, V_{OUT} = 95% of V_{OUT} (Nominal), R_{IMAX} = 604Ω	● ●	180 445	200 495	220 545	mA mA
PWRGD Logic Low Voltage	Pull-Up Current = 50µA	●		0.07	0.25	V
PWRGD Leakage Current	V_{PWRGD} = 45V			0.01	1	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	86	90	94	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1.6		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With IN at 50V, do not pull OUT below 0V. The total differential voltage from IN to OUT must not exceed +50V, –40V. If OUT is pulled above IN and GND, the OUT to IN differential voltage must not exceed 40V.

Note 3: The LT3065 regulator is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3065E regulators are 100% tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance at –40°C to 125°C is assured by design, characterization and correlation with statistical process controls. The LT3065I regulators are guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3065MP regulators are 100% tested over the –55°C to 150°C operating junction temperature range. The LT3065H regulators are 100% tested at the 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The LT3065 adjustable version is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 5: Maximum junction temperature limits operating conditions. Regulated output voltage specifications do not apply for all possible combinations of input voltage and output current. If operating at the maximum input voltage, limit the output current range. If operating at the maximum output current, limit the input voltage range. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit vs $V_{IN} - V_{OUT}$ in the Typical Performance Characteristics section.

Note 6: Dropout voltage is the minimum IN-to-OUT differential voltage needed to maintain regulation at a specified output current. In dropout, the output voltage equals ($V_{IN} - V_{DROPOUT}$). For some output voltages, minimum input voltage requirements limit dropout voltage.

Note 7: To satisfy minimum input voltage requirements, the LT3065 is tested and specified for these conditions with an external resistor divider (60.4k bottom, 442k top) which sets V_{OUT} to 5V. The divider adds 10uA of output DC load. This external current is not factored into GND pin current.

Note 8: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)} + 0.6V$ and a current source load. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 9: To satisfy requirements for minimum input voltage, current limit is tested at $V_{IN} = V_{OUT(NOMINAL)} + 1V$ or V_{IN} = 2.2V, whichever is greater.

Note 10: ADJ pin bias current flows out of the ADJ pin.

Note 11: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 12: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the specified voltage. This current flows into the OUT pin and out of the GND pin.

Note 13: Current limit varies inversely with the external resistor value tied from the IMAX pin to GND. For detailed information on selecting the IMAX resistor value, see the Applications Information section. If the externally programmed current limit feature is unused, tie the IMAX pin to GND. The internal current limit circuitry implements short-circuit protection as specified.

Note 14: This IC includes over temperature protection that protects the device during overload conditions. Junction temperature exceeds 125°C (LT3065E, LT3065I) or 150°C (LT3065MP, LT3065H) when the over temperature circuitry is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

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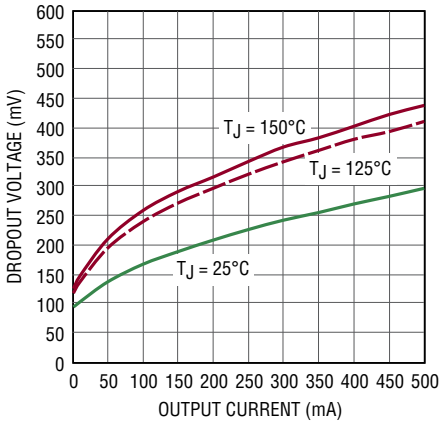
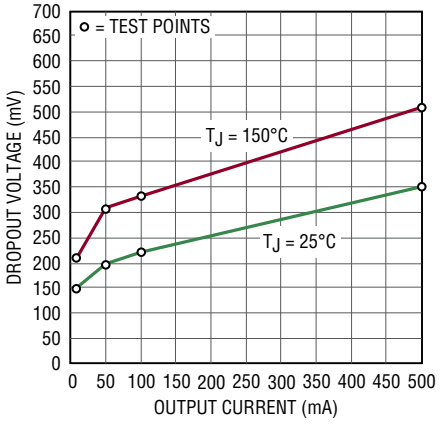
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

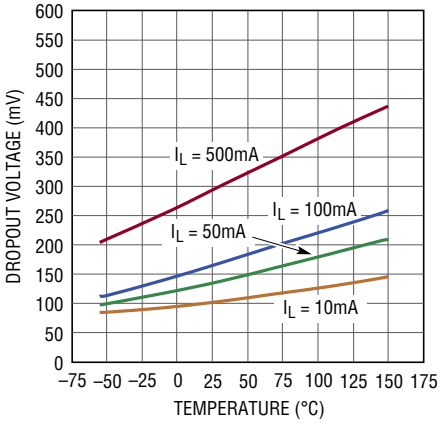
Typical Dropout Voltage



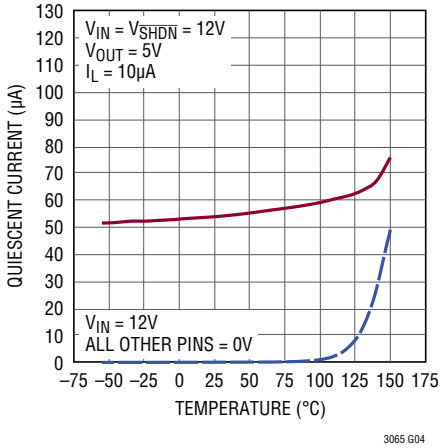
Guaranteed Dropout Voltage



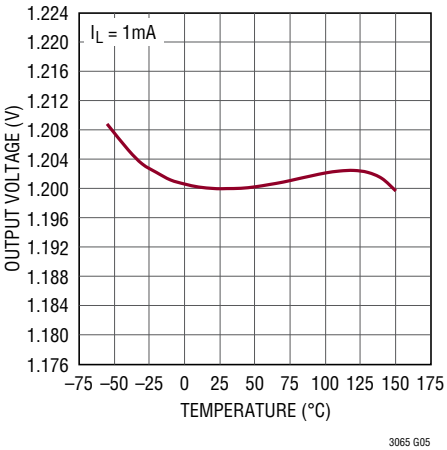
Dropout Voltage



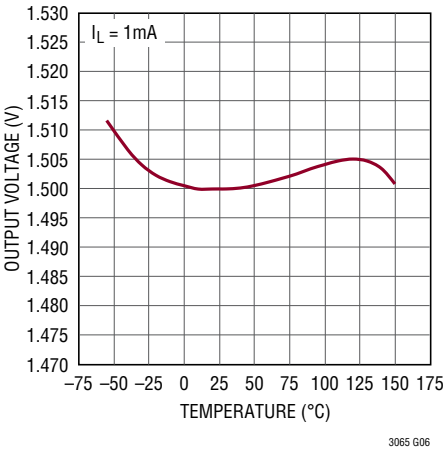
Quiescent Current



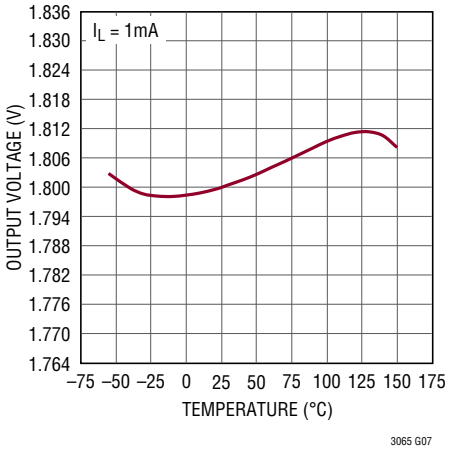
LT3065-1.2 Output Voltage



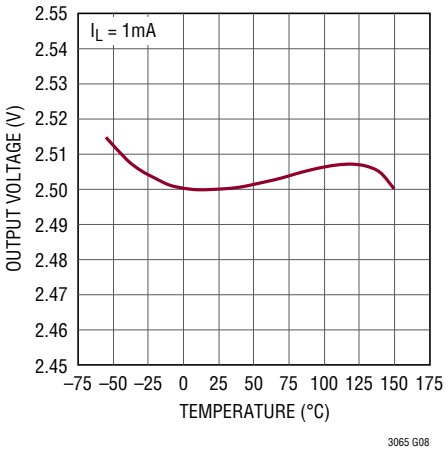
LT3065-1.5 Output Voltage



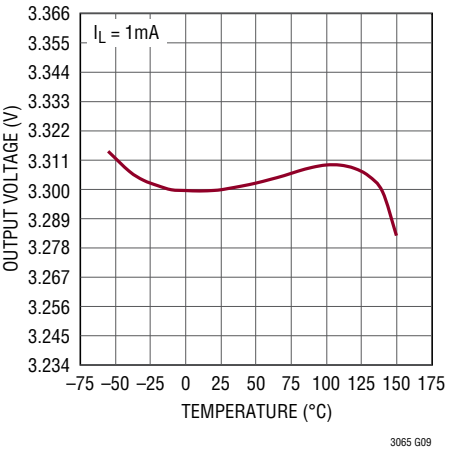
LT3065-1.8 Output Voltage



LT3065-2.5 Output Voltage



LT3065-3.3 Output Voltage



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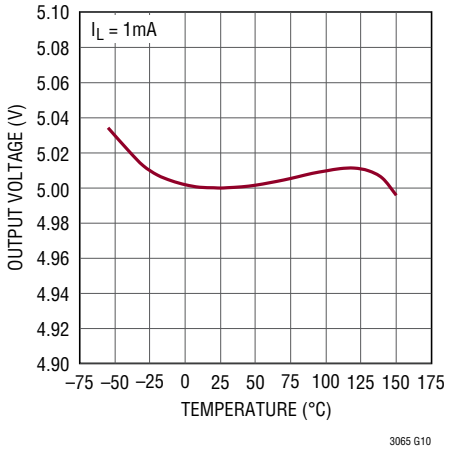
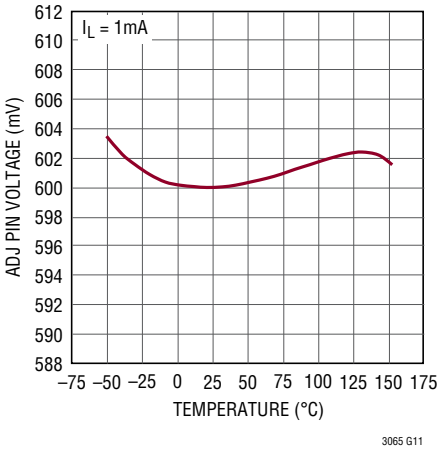
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

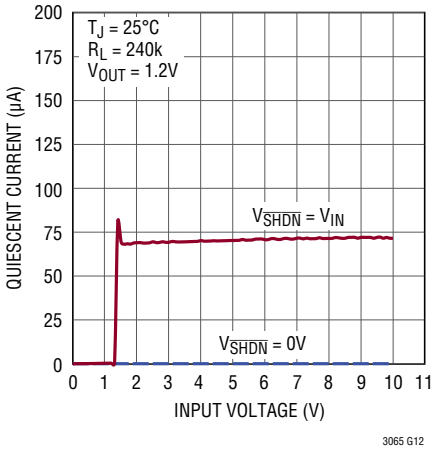
LT3065-5 Output Voltage



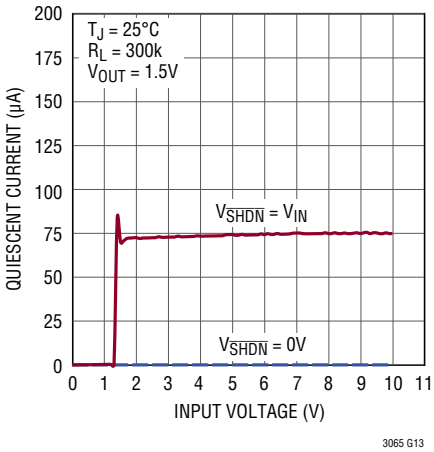
ADJ Pin Voltage



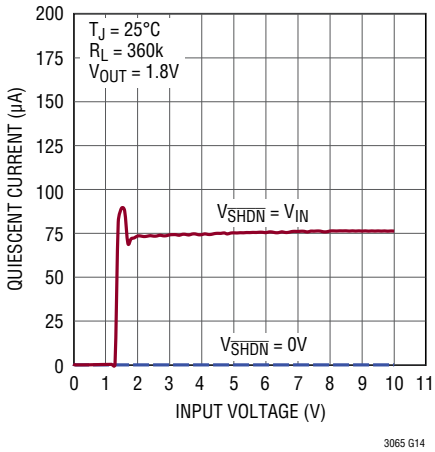
LT3065-1.2 Quiescent Current



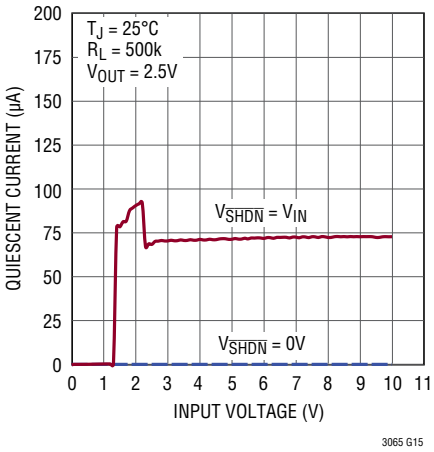
LT3065-1.5 Quiescent Current



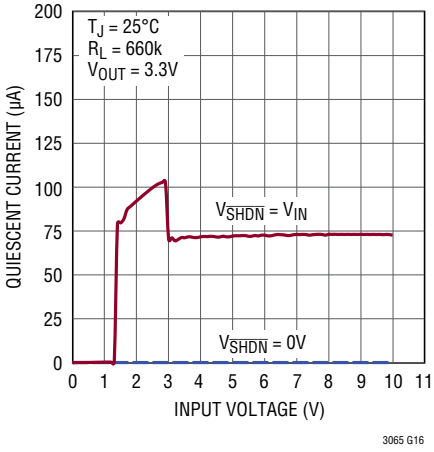
LT3065-1.8 Quiescent Current



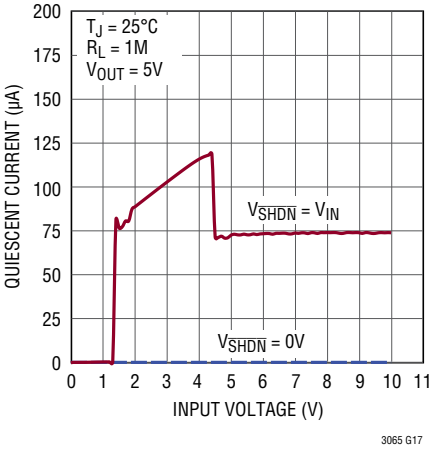
LT3065-2.5 Quiescent Current



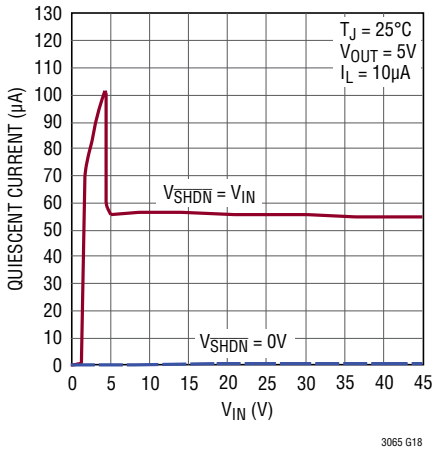
LT3065-3.3 Quiescent Current



LT3065-5 Quiescent Current



Quiescent Current



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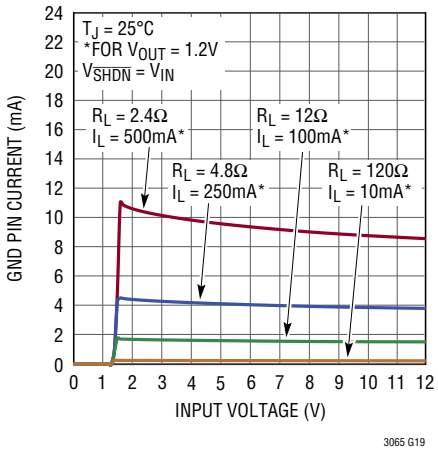
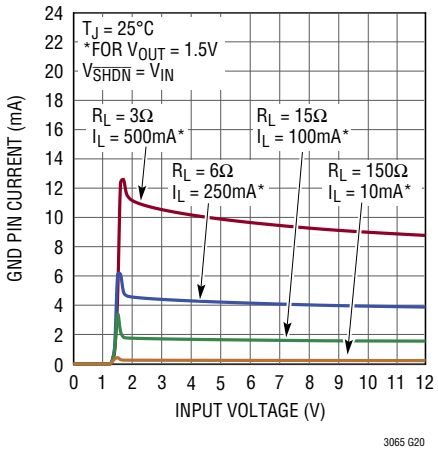
TYPICAL PERFORMANCE CHARACTERISTICS

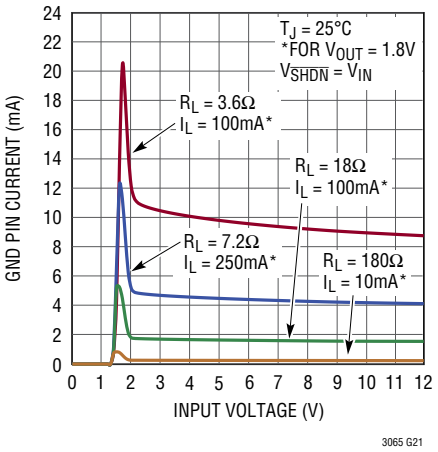
LT3065-1.2 GND Pin Current



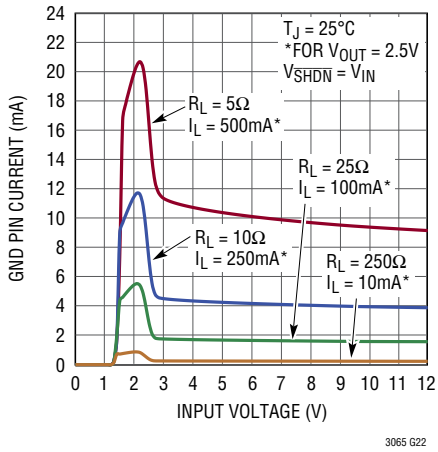
LT3065-1.5 GND Pin Current



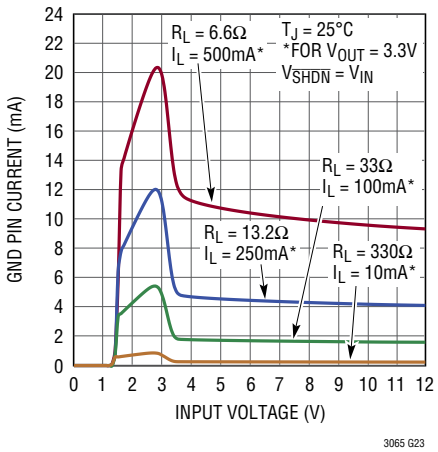
LT3065-1.8 GND Pin Current



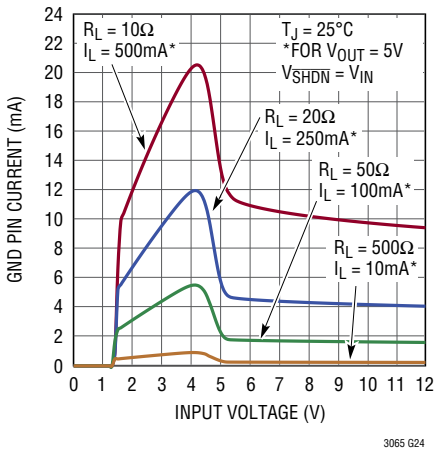
LT3065-2.5 GND Pin Current



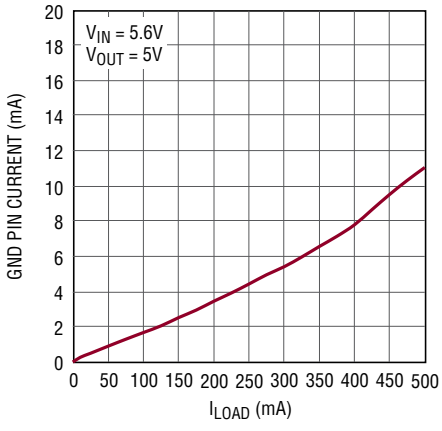
LT3065-3.3 GND Pin Current



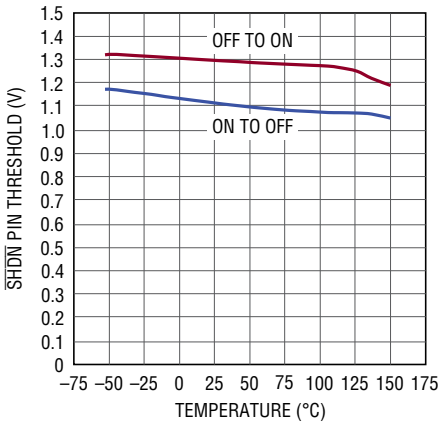
LT3065-5 GND Pin Current



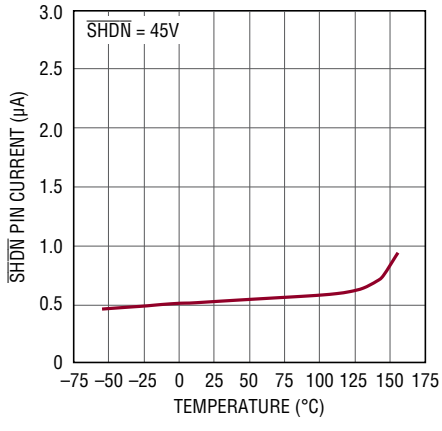
GND Pin Current vs I_{LOAD}



$\overline{SHDN}$ Pin Threshold



$\overline{SHDN}$ Pin Current



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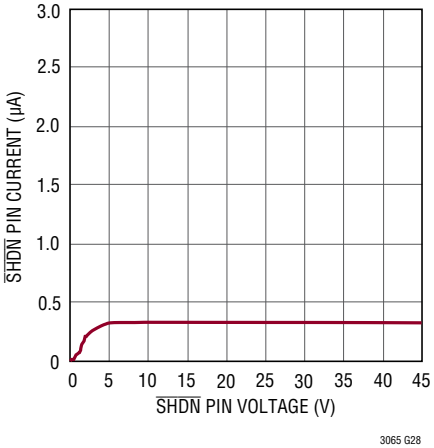
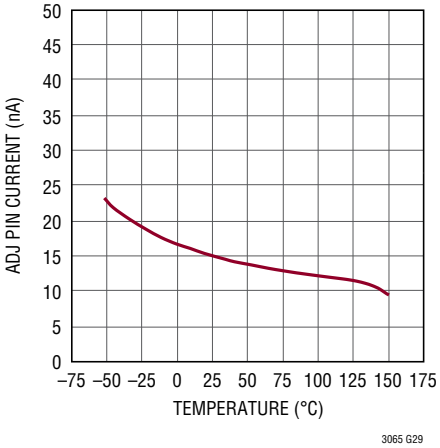
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

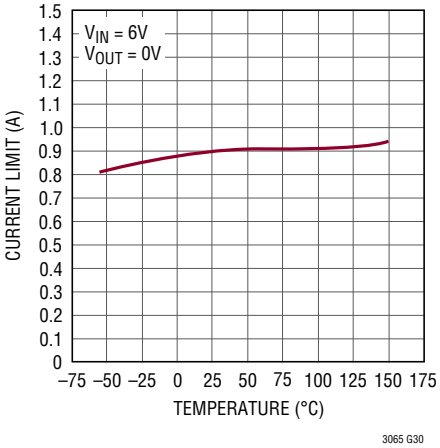
$\overline{SHDN}$ Pin Input Current



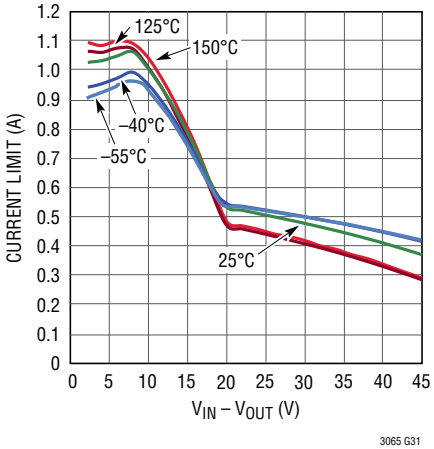
ADJ Pin Bias Current



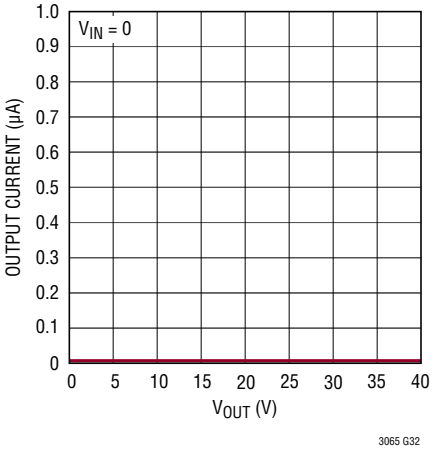
Internal Current Limit



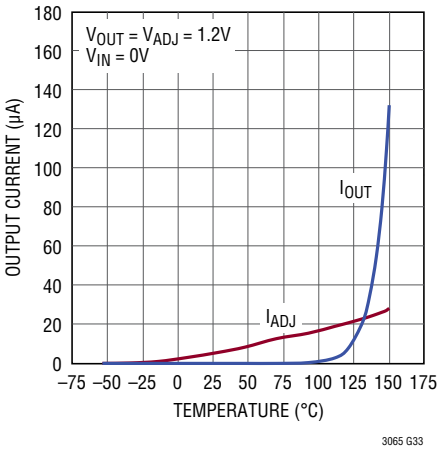
Internal Current Limit



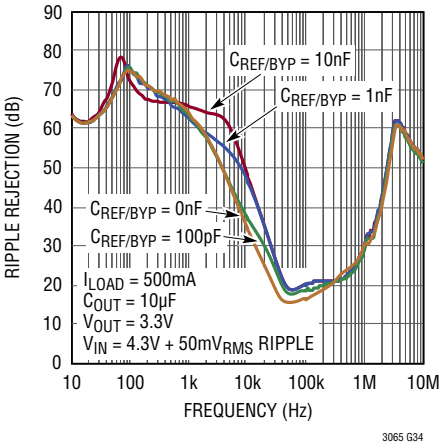
Reverse Output Current



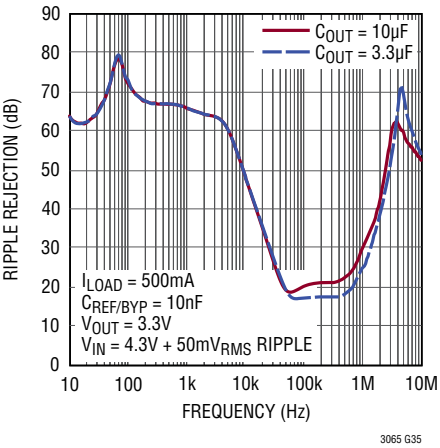
Reverse Output Current



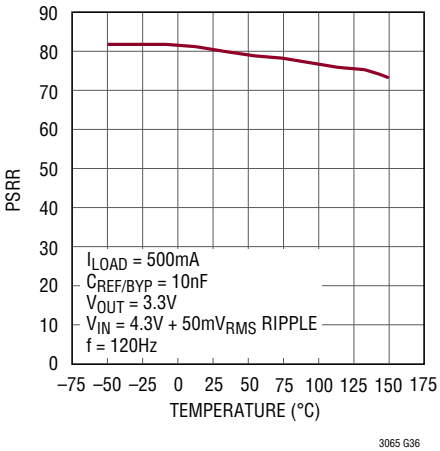
Input Ripple Rejection



Input Ripple Rejection



Input Ripple Rejection



Rev. F

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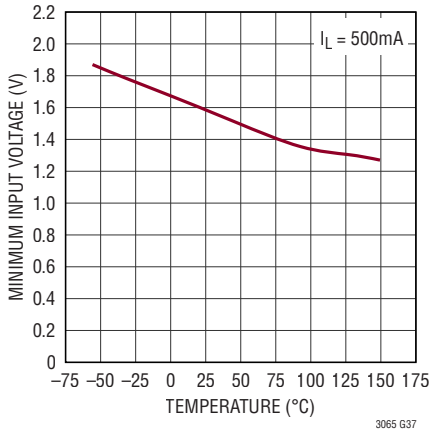
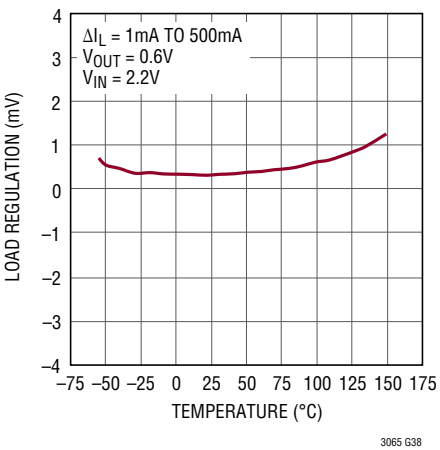
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

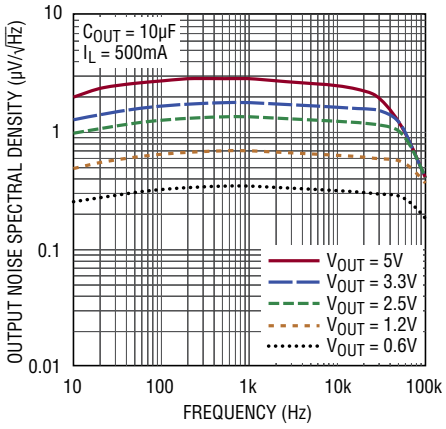
Minimum Input Voltage



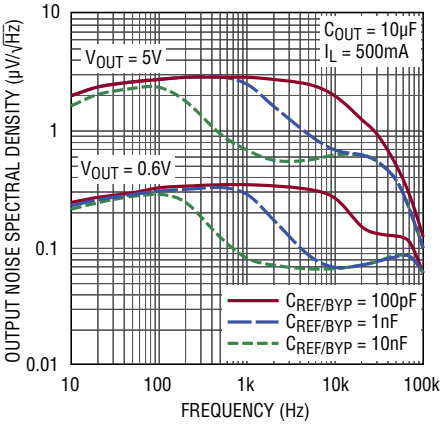
Load Regulation



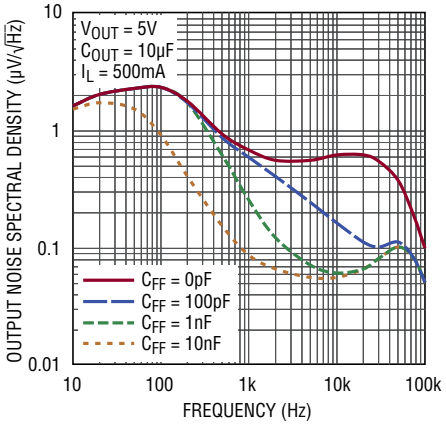
Output Noise Spectral Density $C_{REF/BYP}$ = 0, C_{FF} = 0



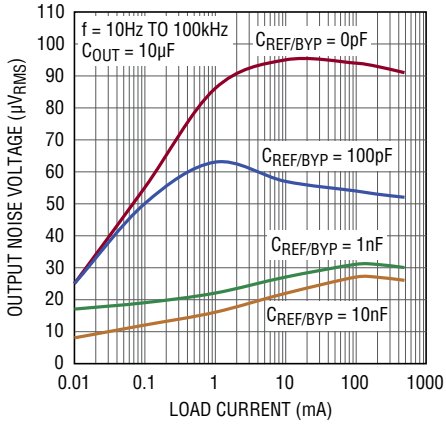
Output Noise Spectral Density vs $C_{REF/BYP}$, C_{FF} = 0



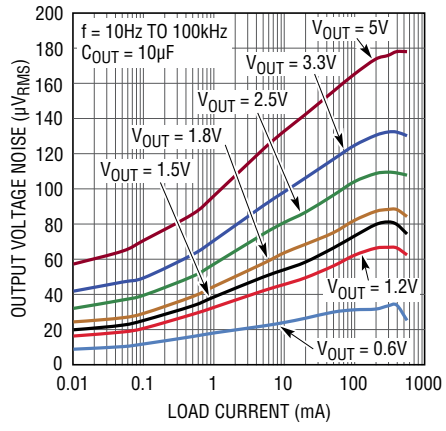
Output Noise Spectral Density vs C_{FF}, $C_{REF/BYP}$ = 10nF



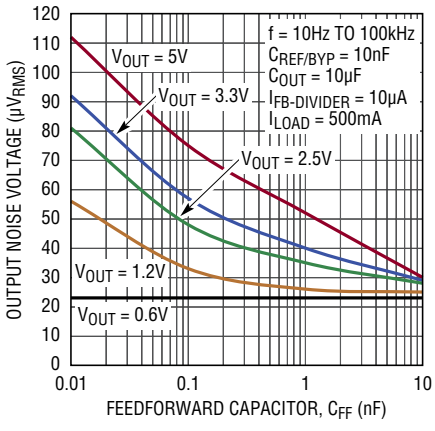
RMS Output Noise, V_{OUT} = 0.6V, C_{FF} = 0



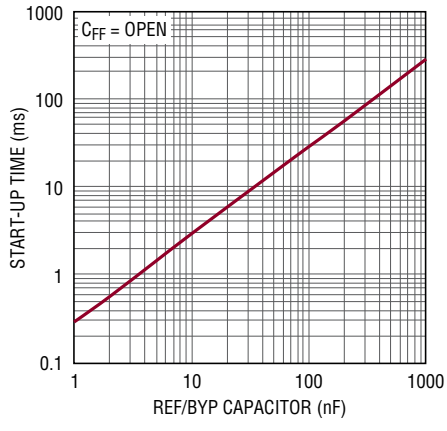
RMS Output Noise vs Load Current vs $C_{REF/BYP}$ = 10nF, C_{FF} = 0



RMS Output Noise, vs Feedforward Capacitor (C_{FF})



Start-Up Time vs REF/BYP Capacitor



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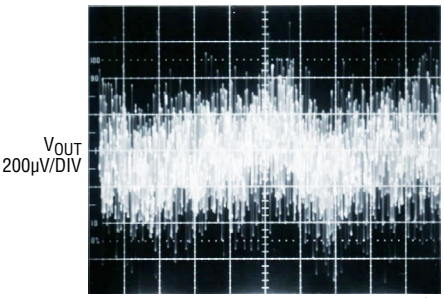
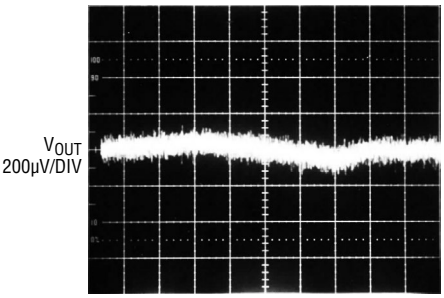
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

10Hz to 100kHz Output Noise
$C_{REF/BYP}$ = 10nF, C_{FF} = 0



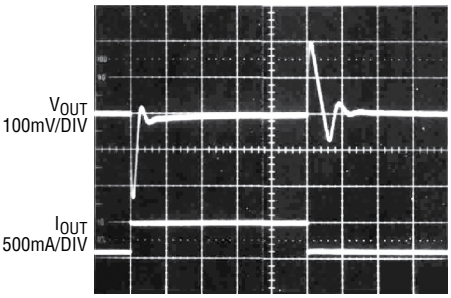
C_{OUT} = 10µF
I_{LOAD} = 500mA
V_{OUT} = 5V
2ms/DIV

10Hz to 100kHz Output Noise
$C_{REF/BYP}$ = 10nF, C_{FF} = 10nF



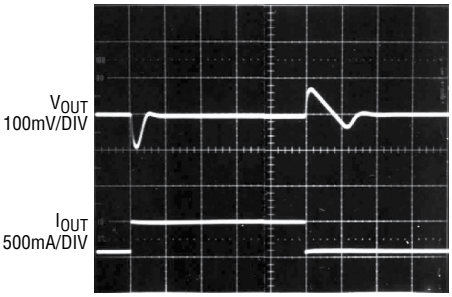
C_{OUT} = 10µF
I_{LOAD} = 500mA
V_{OUT} = 5V
2ms/DIV

5V Transient Response
C_{FF} = 0, I_{OUT} = 50mA to 500mA



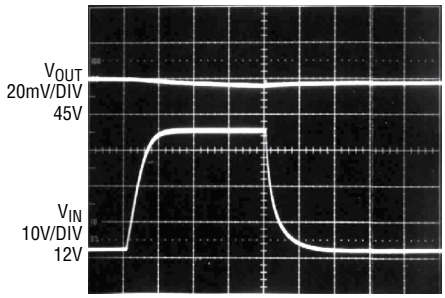
V_{IN} = 6V
C_{OUT} = 10µF
$I_{FB-DIVIDER}$ = 10µA
V_{OUT} = 5V
100µs/DIV

5V Transient Response
C_{FF} = 10nF, I_{OUT} = 50mA to 500mA



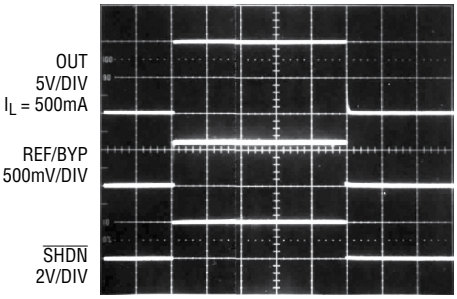
V_{IN} = 6V
C_{OUT} = 10µF
$I_{FB-DIVIDER}$ = 10µA
V_{OUT} = 5V
20µs/DIV

Transient Response (Load Dump)



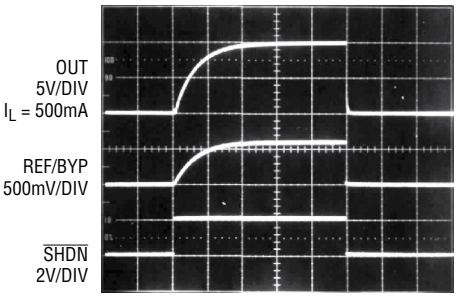
V_{OUT} = 5V
I_{OUT} = 100mA
C_{OUT} = 10µF
1ms/DIV

$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 0



2ms/DIV

$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 10nF



2ms/DIV

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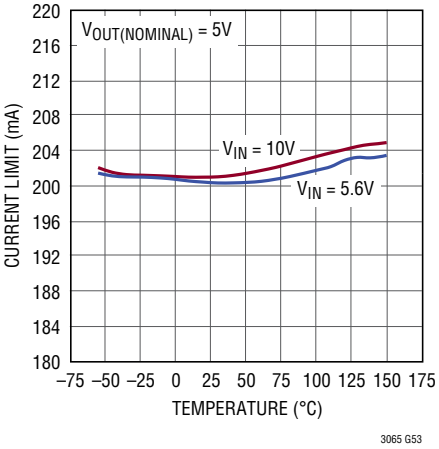
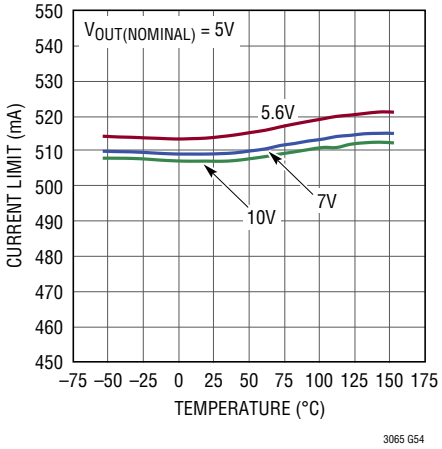
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

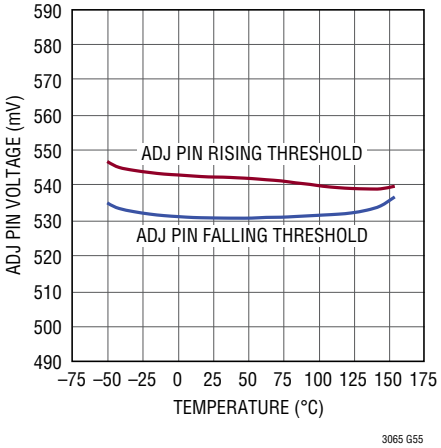
Precision Current Limit, R_{IMAX} = 1.5k



Precision Current Limit, R_{IMAX} = 604Ω



PWRGD Threshold Voltage



PIN FUNCTIONS (DFN/MSOP)

IN (Pins 1, 2/Pins 1, 2): Input. These pin(s) supply power to the device. The LT3065 requires a local IN bypass capacitor if it is located more than six inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery-powered circuits is advisable. An input bypass capacitor in the range of 1µF to 10µF generally suffices. See Input Capacitance and Stability in the Applications Information section for more information.

The LT3065 withstands reverse voltages on the IN pin with respect to its GND and OUT pins. In such case, such as a battery plugged in backwards, the LT3065 behaves as if a diode is in series with its input. No reverse current flows into the LT3065 and no reverse voltage appears at the load. The device protects itself and the load.

$\overline{\text{SHDN}}$ (Pin 3/Pin 3): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3065 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 2µA. If unused, connect the $\overline{\text{SHDN}}$ pin to IN. The LT3065 does not function if the $\overline{\text{SHDN}}$ pin is not connected.

PWRGD (Pin 4/Pin 4): Power Good. The PWRGD pin is an open-drain output that actively pulls low if the output is less than 90% of the nominal output value. The PWRGD pin is capable of sinking 50µA. There is no internal pull-up resistor; an external pull-up resistor must be used.

I_{MAX} (Pin 5/Pin 5): Precision Current Limit Programming. This pin is the collector of a current mirror PNP that is 1/500th the size of the output power PNP. This pin is also the input to the current limit amplifier. The current limit threshold is set by connecting a resistor between the I_{MAX} pin and GND.

For detailed information on how to set the I_{MAX} pin resistor value, see the Applications Information section. The I_{MAX} pin requires a 22nF de-coupling capacitor to ground. If not used, tie I_{MAX} to GND.

NC (Pins 6, 7, MSE Package Only): No Connect. These pins have no connection to internal circuitry. These pins may be floated or connected to GND.

REF/BYP (Pin 6/Pin 8): Bypass/Soft Start. Connecting a capacitor from this pin to GND bypasses the LT3065's reference noise and soft-starts the reference. A 10nF bypass capacitor typically reduces output voltage noise to 25μV_{RMS} in a 10Hz to 100kHz bandwidth. Soft-start time is directly

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PIN FUNCTIONS (DFN/MSOP)

proportional to the BYP capacitor value. If the LT3065 is placed in shutdown, BYP is actively pulled low by an internal device to reset soft-start. If low noise or soft-start performance is not required, this pin must be left floating (unconnected). Do not drive this pin with any active circuitry.

Because the REF/BYP pin is the reference input to the error amplifier, stray capacitance at this point should be minimized. Special attention should be given to any stray capacitances that can couple external signals onto the REF/BYP pin producing undesirable output transients or ripple. A minimum capacitance of 100pF from REF/BYP to GND is recommended.

OUTPUT (Pins 9,10/Pins 11,12): Output. These pins supply power to the load. Stability requirements demand a minimum 3.3µF ceramic output capacitor with an ESR < 1Ω to prevent oscillations. Applications with output voltages less than 1.2V require a minimum 4.7µF ceramic output capacitor. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for details on transient response and reverse output characteristics. Permissible output voltage range is 600mV to 40V.

Adjustable Version Only

GND (Pin 7, Exposed Pad Pin 11/Pin 9, Exposed Pad Pin 13): Ground. The exposed pad of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 11/Pin 13 to the PCB GND and tie it directly to Pin 7/Pin 9. For the adjustable LT3065, connect the bottom of the external resistor divider that sets output voltage directly to GND (Pin 7/Pin 9)for optimum load regulation.

ADJ (Pin 8/Pin 10): Adjust. This pin is the error amplifier's inverting terminal. It's typical bias current of 16nA flows out of the pin (see curve of ADJ Pin Bias Current vs Temperature in the Typical Performance Characteristics section). The ADJ pin voltage is 600mV referenced to GND.

Connecting a capacitor from OUT to ADJ reduces output noise and improves transient response for output voltages greater than 600mV. See the Applications Information section for calculating the value of the feedforward capacitor.

At output voltages above 0.6V, the resistor divider connected to the ADJ pin is used to regulate voltage at the load. Parasitic resistances of PCB traces or cables can therefore result in load regulation errors at high output currents. To eliminate these, connect the resistor divider directly to the load for a Kelvin sense connection, as shown in Figure 1.

Fixed Voltage Version Only

GND (Exposed Pad Pin 11, Exposed Pad Pin 13): Ground. The exposed pad of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 11/Pin 13 to the PCB ground.

SENSE (Pin 8/Pin 10): Sense. This pin is the top of the internal resistor divider network, and should be connected directly to the load, as a Kelvin sense, for optimum load regulation and transient performance. Connecting this pin to the output pin at the package, rather than directly to the load, can result in load regulation errors due to the current across the parasitic resistance of the PCB trace.

ADJ (Pin 7/Pin 9): Adjust. This pin is the midpoint of the internal resistor divider network and the inverting input to the error amplifier. Connecting a capacitor from the OUT to ADJ reduces output noise and improves transient response. See the Applications Information section for calculating the value of the feedforward capacitor; the internal divider current is 5µA. This pin should not be used for any other purpose.

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PIN FUNCTIONS

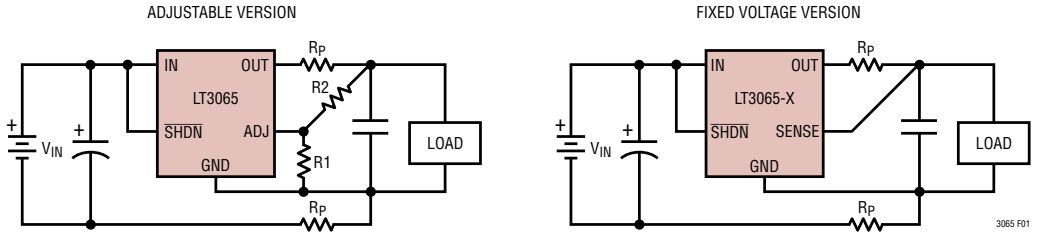
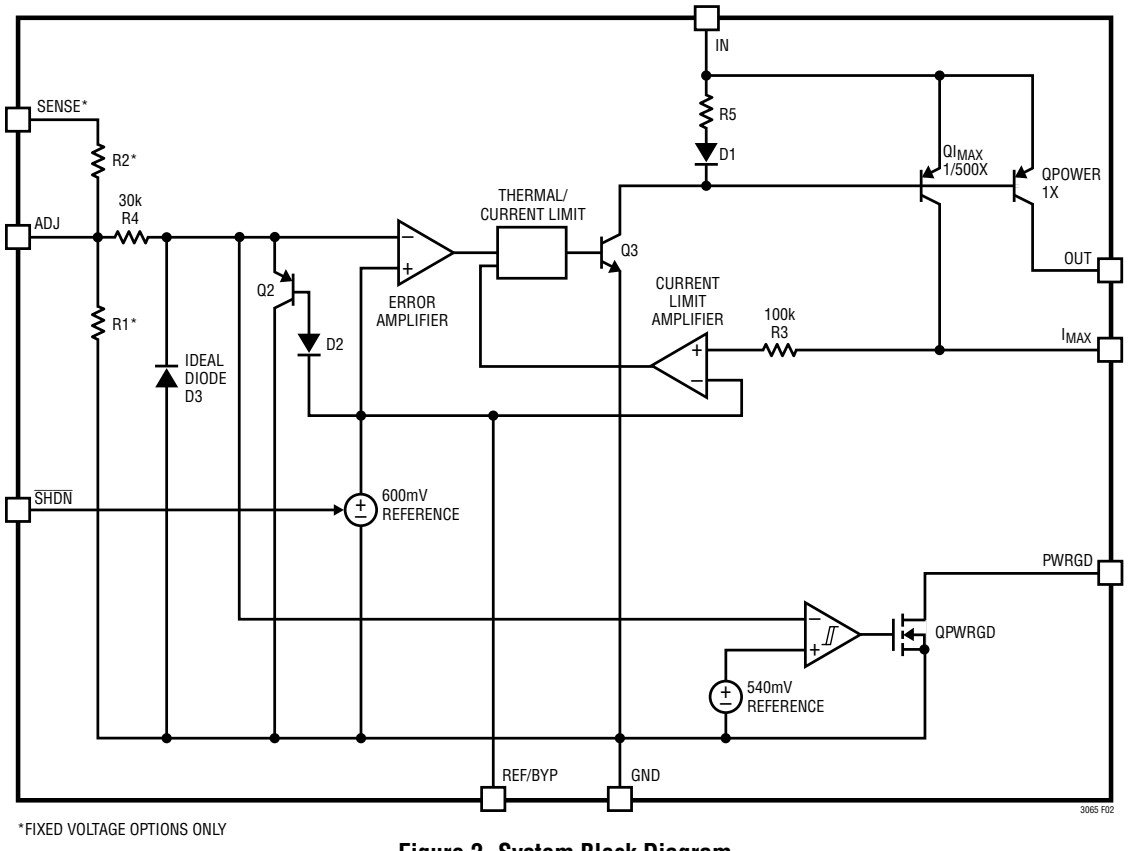


Figure 1. Kelvin Sense Connection

BLOCK DIAGRAM

Table 1. Fixed Voltage Option Resistor Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
5	120	880
3.3	120	540
2.5	120	380
1.8	120	240
1.5	120	180
1.2	120	120



*FIXED VOLTAGE OPTIONS ONLY

Figure 2. System Block Diagram

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APPLICATIONS INFORMATION

The LT3065 are micropower, low noise and low drop-out voltage, 500mA linear regulators with micropower shutdown, programmable current limit, and a Power-good flag. The devices supply up to 500mA at a typical dropout voltage of 300mV and operate over a 1.6V to 45V input range.

A single external capacitor provides low noise reference performance and output soft-start functionality. For example, connecting a 10nF capacitor from the REF/BYP pin to GND lowers output noise to 25μV_{RMS} over a 10Hz to 100kHz bandwidth. This capacitor also soft starts the reference and prevents output voltage overshoot at turn-on.

The LT3065's quiescent current is merely 55μA but provides fast transient response with a low ESR, minimum value 3.3μF ceramic output capacitor. In shutdown, quiescent current is less than 1μA and the reference soft-start capacitor is reset.

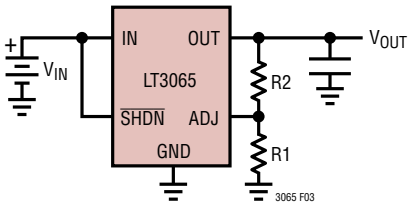
The LT3065 optimizes stability and transient response with low ESR, ceramic output capacitors. The regulator does not require the addition of ESR as is common with other regulators. The LT3065 typically provides better than 0.1% line regulation and 0.1% load regulation. Internal protection circuitry includes reverse battery protection, reverse output protection, reverse current protection, current limit with foldback and thermal shutdown.

This "bullet-proof" protection set makes it ideal for use in battery-powered, automotive and industrial systems.In battery backup applications where the output is held up by a backup battery and the input is pulled to ground, the LT3065 acts like it has a diode in series with its output and prevents reverse current.

Adjustable Operation

The adjustable LT3065 has an output voltage range of 0.6V to 40V. Output voltage is set by the ratio of two external resistors, as shown in Figure 3. The device regulates the output to maintain the ADJ pin voltage at 0.6V referenced to ground. The current in R1 equals 0.6V/R1, and R2's current is R1's current minus the ADJ pin bias current.

The ADJ pin bias current, 16nA at 25°C, flows from the ADJ pin through R1 to GND. Calculate the output voltage using the formula in Figure 3. R1's value should not be greater than 62k to provide a minimum 10μA load current so that output voltage errors, caused by the ADJ pin bias current, are minimized. Note that in shutdown, the output is turned off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.



$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)-(I_{ADJ}\bullet R2)$$

$V_{ADJ} = 0.6V$

I_{ADJ} = 16nA AT 25°C

OUTPUT RANGE = 0.6V TO 40V

Figure 3. Adjustable Operation

The LT3065 is tested and specified with the ADJ pin tied to the OUT pin, yielding V_{OUT} = 0.6V. Specifications for output voltages greater than 0.6V are proportional to the ratio of the desired output voltage to 0.6V: V_{OUT}/0.6V. For example, load regulation for an output current change of 1mA to 500mA is 0.1mV (typical) at V_{OUT} = 0.6V. At V_{OUT} = 12V, load regulation is:

$$\frac{12V}{0.6V}\bullet(0.1mV)=2mV$$

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APPLICATIONS INFORMATION

Table 2 shows 1% resistor divider values for some common output voltages with a resistor divider current of 10µA.

Table 2. Output Voltage Resistor Divider Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.2	60.4	60.4
1.5	59	88.7
1.8	59	118
2.5	60.4	191
3	59	237
3.3	61.9	280
5	59	432

Bypass Capacitance and Output Voltage Noise

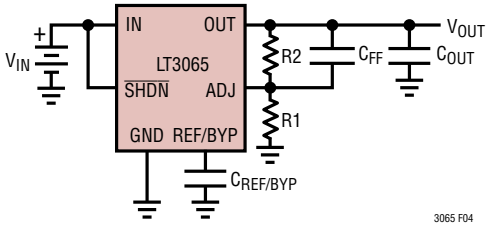
The LT3065 regulator provides low output voltage noise over a 10Hz to 100kHz bandwidth while operating at full load with the addition of a bypass capacitor ($C_{REF/BYP}$) from the REF/BYP pin to GND. A high quality low leakage capacitor is recommended. This capacitor bypasses the internal reference of the regulator, providing a low frequency noise pole for the internal reference. With the use of 10nF for $C_{REF/BYP}$, output voltage noise decreases to as low as 25µV_{RMS} when the output voltage is set for 0.6V. For higher output voltages (generated by using a feedback resistor divider), the output voltage noise gains up proportionately when using $C_{REF/BYP}$.

To lower the higher output voltage noise, connect a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin. A high quality, low leakage capacitor is recommended. This capacitor bypasses the error amplifier of the regulator, providing an additional low frequency noise pole. With the use of 10nF for both C_{FF} and $C_{REF/BYP}$, output voltage noise decreases to 25µV_{RMS} when the output voltage is set to 5V by a 10µA feedback resistor divider. If the current in the feedback resistor divider is doubled, C_{FF} must also be doubled to achieve equivalent noise performance.

Feedforward capacitance can also be used in fixed-voltage parts; the feedforward capacitor is connected from OUT to ADJ in the same manner. In this case, the current in the internal feedback resistor divider is 5µA.

Higher values of output voltage noise can occur if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces induces unwanted noise onto the LT3065's output. Power supply ripple rejection must also be considered. The LT3065 regulator does not have unlimited power supply rejection and passes a small portion of the input noise through to the output.

Using a feedforward capacitor (C_{FF}) connected between V_{OUT} and ADJ has the added benefit of improving transient response for output voltages greater than 0.6V. With no feedforward capacitor, the settling time increases as the output voltage increases above 0.6V. Use the equation in Figure 4 to determine the minimum value of C_{FF} to achieve a transient response that is similar to the 0.6V output voltage performance regardless of the chosen output voltage (See Figure 5 and Transient Response in the Typical Performance Characteristics section).



$$C_{FF} \geq \frac{10nF}{10\mu A} \bullet (I_{FB_DIVIDER})$$

$$I_{FB_DIVIDER} = \frac{V_{OUT}}{R1+R2}$$

Figure 4. Feedforward Capacitor for Fast Transient Response

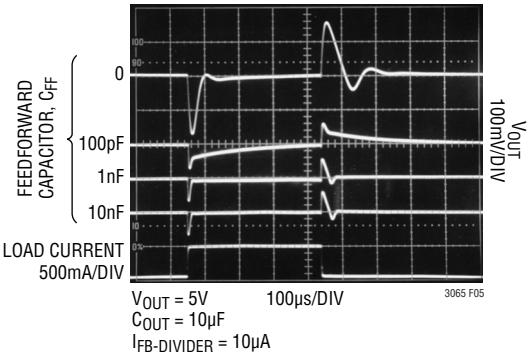


Figure 5. Transient Response vs Feedforward Capacitor

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APPLICATIONS INFORMATION

During start-up, the internal reference soft-starts when a REF/BYP capacitor is used. Regulator start-up time is directly proportional to the size of the bypass capacitor (see Start-Up Time vs REF/BYP Capacitor in the Typical Performance Characteristics section). The reference bypass capacitor is actively pulled low during shutdown to reset the internal reference.

Using a feedforward capacitor also affects start-up time. Start-up time is directly proportional to the size of the feedforward capacitor and the output voltage, and is inversely proportional to the feedback resistor divider current, slowing to 15ms with a 10nF feedforward capacitor and a 10µF output capacitor for an output voltage set to 5V by a 10µA feedback resistor divider.

Output Capacitance and Transient Response

The LT3065 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 3.3µF with an ESR of 1Ω or less to prevent oscillations. For V_{OUT} less than 1.2V, use a minimum C_{OUT} of 4.7µF. If a feedforward capacitor is used with output voltages set for greater than 24V, use a minimum output capacitor of 10µF. The LT3065 is a micropower device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3065, increase the effective output capacitor value. For applications with large load current transients, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figures 6 and 7. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied, and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor.

The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

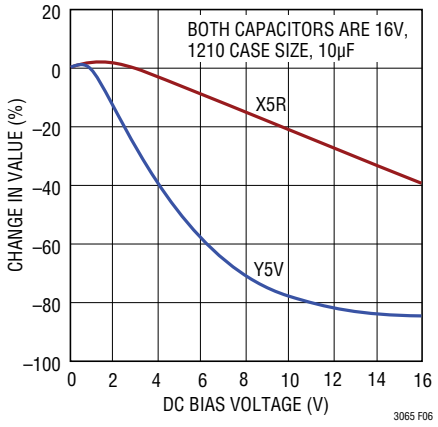

Figure 6. Ceramic Capacitor DC Bias Characteristics

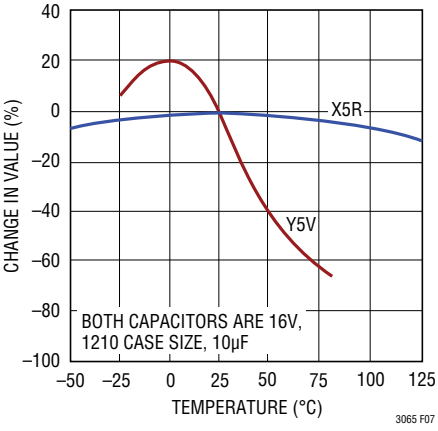

Figure 7. Ceramic Capacitor Temperature Characteristics

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APPLICATIONS INFORMATION

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 8 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

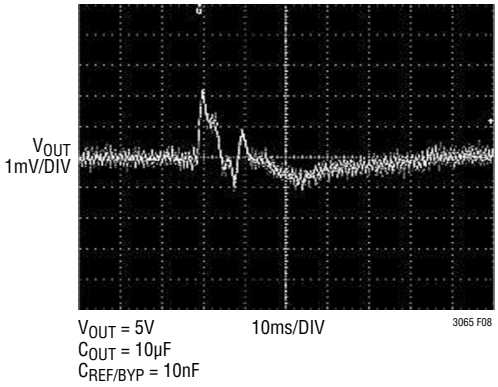

Figure 8. Noise Resulting from Tapping On a Ceramic Capacitor

Stability and Input Capacitance

Low ESR, ceramic input bypass capacitors are acceptable for applications without long input leads. However, applications connecting a power supply to an LT3065 circuit's IN and GND pins with long input wires combined with a low ESR, ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations.

The input wire inductance found in many battery-powered applications, combined with the low ESR ceramic input capacitor, forms a high Q LC resonant tank circuit. In some instances this resonant frequency beats against the output current dependent LDO bandwidth and interferes with proper operation. Simple circuit modifications/solutions are then required. This behavior is not indicative of LT3065 instability, but is a common ceramic input bypass capacitor application issue.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. Wire diameter is not a major factor on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire (diameter = 0.26") is about half the self-inductance of a 30-AWG wire (diameter = 0.01"). One foot of 30-AWG wire has approximately 465nH of self-inductance.

Two methods can reduce wire self-inductance. One method divides the current flowing towards the LT3065 between two parallel conductors. In this case, the farther apart the wires are from each other, the more the self-inductance is reduced; up to a 50% reduction when placed a few inches apart. Splitting the wires connects two equal inductors in parallel, but placing them in close proximity creates mutual inductance adding to the self-inductance. The second and most effective way to reduce overall inductance is to place both forward and return current conductors (the input and GND wires) in very close proximity. Two 30-AWG wires separated by only 0.02", used as forward and return current conductors, reduce the overall self-inductance to approximately one-fifth that of a single isolated wire.

If a battery, mounted in close proximity, powers the LT3065, a 10µF input capacitor suffices for stability. However, if a distant supply powers the LT3065, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 8 inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3065's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3065 input bypassing. Series resistance between the supply and the LT3065 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3065 input in place of ceramic capacitors.

I_{MAX} Pin Operation

The I_{MAX} pin is the collector of a PNP that sources a current equal to 1/500th of output load current (see Block Diagram). The I_{MAX} pin is also the input to the precision

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APPLICATIONS INFORMATION

current limit amplifier. Connecting a resistor (R_{IMAX}) from I_{MAX} to GND sets the current limit threshold. If the output load increases to a level such that the I_{MAX} pin voltage reaches 0.6V, the current limit amplifier takes control and regulates the I_{MAX} voltage to 0.6V, regardless of the output voltage. Calculate the required R_{IMAX} value for a given current limit from the following formula:

$$R_{IMAX} = 500 \bullet \frac{0.6V}{I_{LIMIT}}$$

In cases where the IN to OUT differential voltage exceeds 10V, current limit foldback lowers the internal current limit level, possibly causing it to override the external programmable current limit. See the Internal Current Limit vs $V_{IN} – V_{OUT}$ graph in the Typical Performance Characteristics section.

The I_{MAX} pin requires a 22nF decoupling capacitor. If the external programmable current limit is not used, connect the I_{MAX} pin directly to GND. LT3065 power dissipation increases the I_{MAX} threshold at a rate of approximately 0.5 percent per watt.

PWRGD Pin Operation

The PWRGD pin is an open-drain high voltage NMOS digital output capable of sinking 50µA. The PWRGD pin de-asserts and becomes high impedance if the output rises above 90% of its nominal value. If the output falls below 88.4% of its nominal value for more than 25µs, the PWRGD pin asserts low. The PWRGD comparator has 1.6% hysteresis and 25µs of deglitching. The PWRGD comparator has a dedicated reference that does not soft-start if a capacitor is used on the REF/BYP pin.

The use of a feed-forward capacitor, C_{FF}, as shown in Figure 4, can result in the ADJ pin being pulled artificially high during startup transients, which causes the PWRGD flag to assert early. To avoid this problem, ensure that the REF/BYP capacitor is significantly larger than the feed-forward capacitor, causing REF/BYP time constant to dominate over the time constant of the resistor divider network.

Operation in Dropout

Some degradation of the I_{MAX} current mirror accuracy occurs for output currents less than 50mA when operating in dropout.

Overload Recovery

Like many IC power regulators, the LT3065 has safe operating area protection. The safe area protection decreases current limit as input-to-output voltage increases, and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT3065 provides some output current at all values of input-to-output voltage up to the device's Absolute Maximum Rating.

When power is first applied, the input voltage rises and the output follows the input; allowing the regulator to start-up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein the removal of an output short will not allow the output to recover. Other regulators, such as the LT1083/LT1084/LT1085 family and LT1764A also exhibit this phenomenon, so it is not unique to the LT3065. The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short circuit or if the shutdown pin is pulled high after the input voltage is already turned on. The load line intersects the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply needs to be cycled down to zero and back up again to recover the output.

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APPLICATIONS INFORMATION

Thermal Considerations

The LT3065's maximum rated junction temperature of 125°C (E-, I-grades) or 150°C (MP-, H-grades) limits its power handling capability. Two components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differential:

   $I_{OUT} \bullet (V_{IN} - V_{OUT})$,

   and

2. GND pin current multiplied by the input voltage:

   $I_{GND} \bullet V_{IN}$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation equals the sum of the two components listed above.

The LT3065 regulator has internal thermal limiting that protects the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature of 125°C (E-, I-grades) or 150°C (MP-, H-grades). Carefully consider all sources of thermal resistance from junction-to-ambient including other heat sources mounted in proximity to the LT3065.

The undersides of the LT3065 DFN and MSE packages have exposed metal from the lead frame to the die attachment. These packages allow heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-inline pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3065 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes also can spread the heat generated by power devices.

Table 3 and Table 4 list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

Table 3. MSOP Measured Thermal Resistance

COPPER AREA			
TOPSIDE	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	28°C/W
1000 sq mm	2500 sq mm	2500 sq mm	31°C/W
225 sq mm	2500 sq mm	2500 sq mm	32°C/W
100 sq mm	2500 sq mm	2500 sq mm	33°C/W

Table 4. DFN Measured Thermal Resistance

COPPER AREA TOPSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	31°C/W
1000 sq mm	2500 sq mm	32°C/W
225 sq mm	2500 sq mm	34°C/W
100 sq mm	2500 sq mm	35°C/W

Calculating Junction Temperature

Example: Given an output voltage of 5V, an input voltage range of 12V ±5%, a maximum output current range of 75mA and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The power dissipated by the device equals:

$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$

where:

$I_{OUT(MAX)} = 75mA$

$V_{IN(MAX)} = 12.6V$

I_{GND} at ($I_{OUT} = 75mA$, $V_{IN} = 12V$) = 3.5mA

So:

$P = 75mA \bullet (12.6V - 5V) + 3.5mA \bullet 12.6V = 0.614W$

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APPLICATIONS INFORMATION

Using a DFN package, the thermal resistance ranges from 31°C/W to 35°C/W depending on the copper area. So the junction temperature rise above ambient approximately equals:

0.614W • 35°C/W = 21.5°C

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

T_{JMAX} = 85°C + 21.5°C = 106.5°C

Protection Features

The LT3065 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse input voltages, reverse output voltages and reverse output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at the LT3065's output. The typical thermal shutdown temperature is 165°C with about 7°C of hysteresis. For normal operation, do not exceed a junction temperature of 125°C (E-, I-grades) or 150°C (MP-, H-grades).

The LT3065 IN pin withstands reverse voltages of 50V. The device limits current flow to less than 1µA (typically less than 25nA) and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

The LT3065 incurs no damage if its output is pulled below ground. If the input is left open circuit or grounded, the output can be pulled below ground by 50V. No current flows through the pass transistor from the output. However, current flows in (but is limited by) the feedback resistor divider that sets the output voltage. Current flows from the bottom resistor in the divider and from the ADJ pin's internal clamp through the top resistor in the divider to the external circuitry pulling OUT below ground. If a voltage source powers the input, the output sources current equal to its current limit capability and the LT3065 protects itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin turns off the device and stops the output from sourcing current.

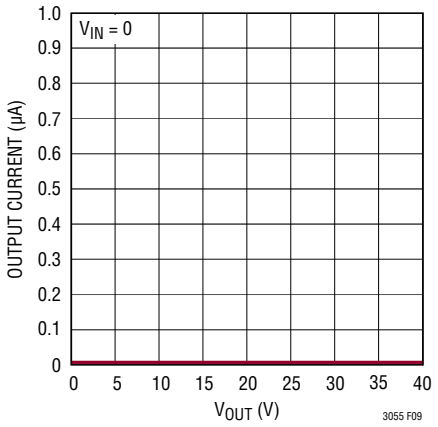

Figure 9. Reverse Output Current

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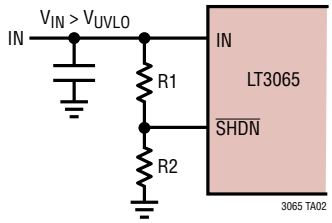
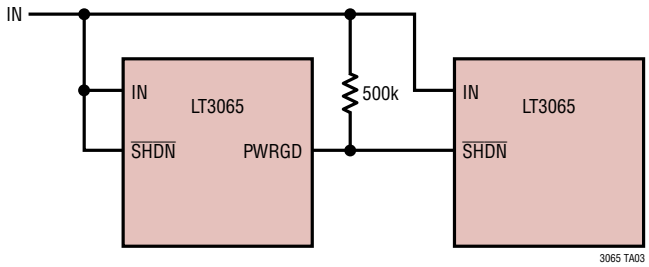
TYPICAL APPLICATIONS

Programming Undervoltage Lockout

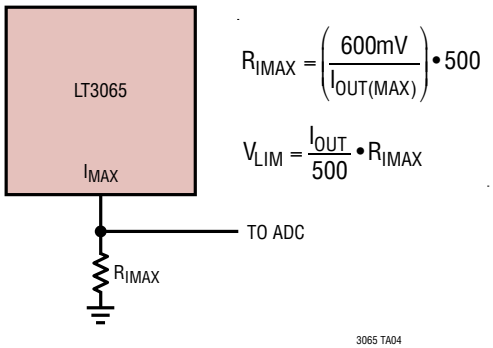


$$V_{UVLO} = \frac{R1+R2}{R2} \bullet 1.1V$$

Power Supply Sequencing Using PWRGD



Current Monitor



$$R_{IMAX} = \left(\frac{600mV}{I_{OUT(MAX)}}\right) \bullet 500$$

$$V_{LIM} = \frac{I_{OUT}}{500} \bullet R_{IMAX}$$

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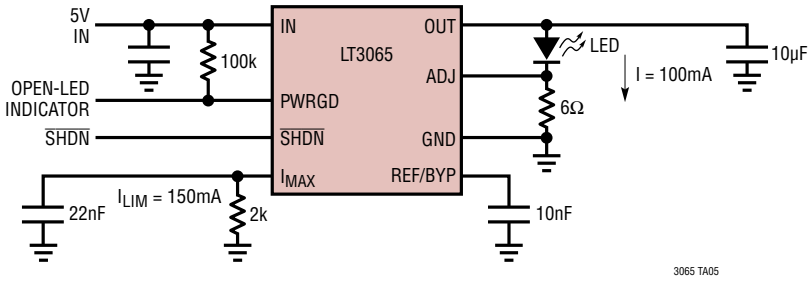
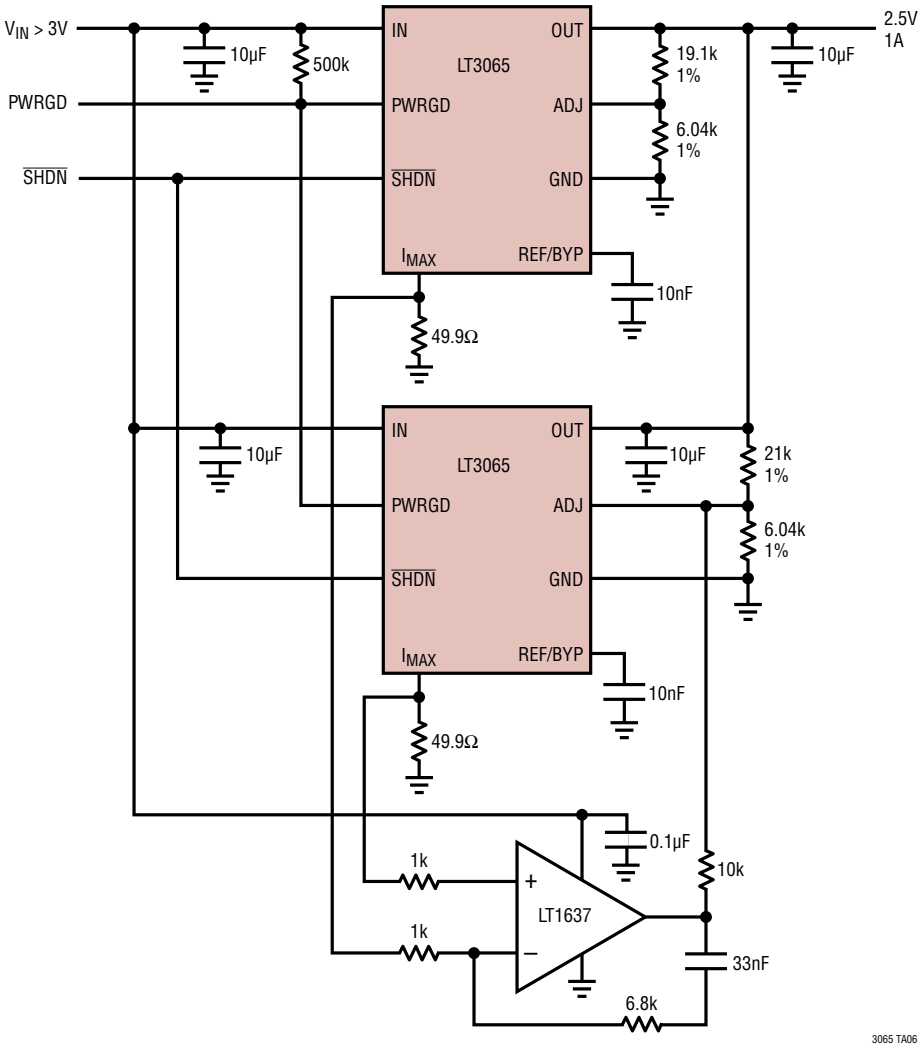
TYPICAL APPLICATIONS

LED Driver/Current Source



Paralleling Regulators for Higher Output Current



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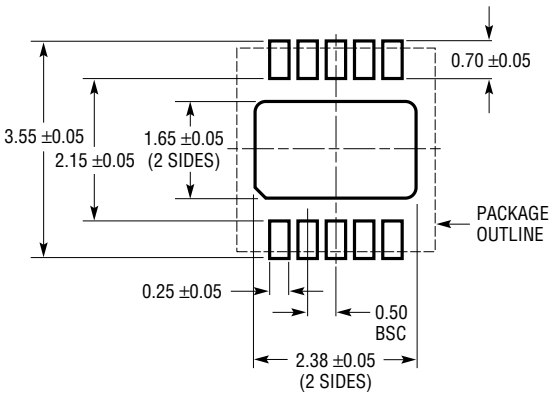
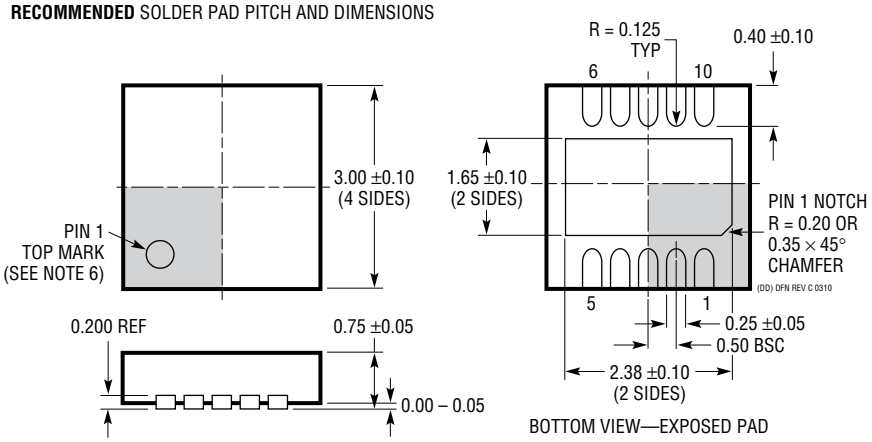
PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

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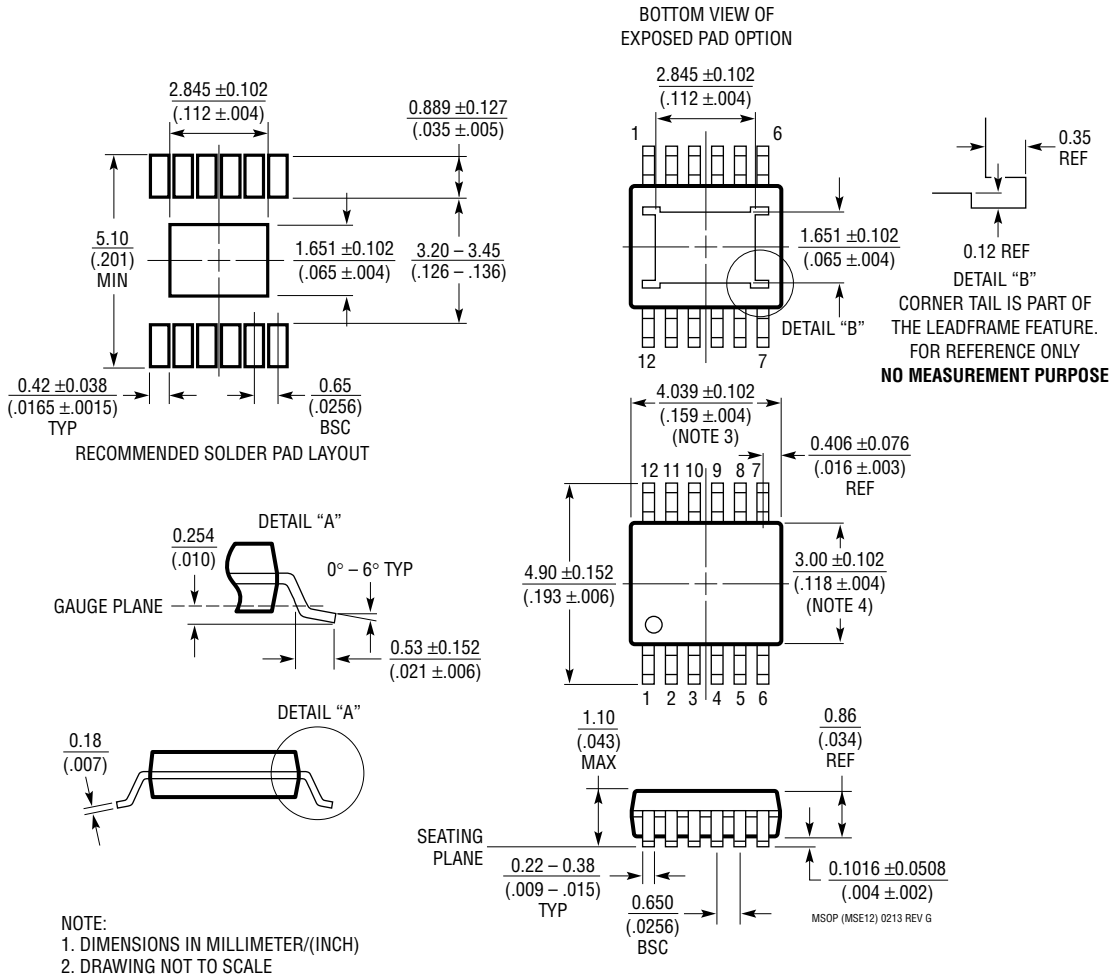
PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/14	Added fixed voltage options and related specs, curves, pin functions, text.	Throughout
		Modified pinouts to accommodate new fixed voltage options.	2
		Added specification for Absolute Maximum SENSE pin voltage.	2
		Modified Bypass Capacitance section.	10
B	11/14	Fixed Pin Functions description.	13
C	05/17	Corrected Input Ripple Rejection graph; changed 100nF to 100pF.	9
		Added bypass capacitor to LED Driver Application circuit.	23
D	11/18	Changed typical Minimum Input Voltage from 1.8V to 1.6V.	1, 4, 15
		Replaced Typical Performance curve Minimum Input Voltage with new graph.	10
		Updated Related Parts section with new 1.6V Minimum V_{IN} (LT3050/LT3055/LT3060).	28
E	01/21	Added AEC-Q100 Qual complete statement.	1
		Added AEC-Q100 part numbers.	4
F	02/21	Added 5V MSE package AEC-Q100 part numbers.	4

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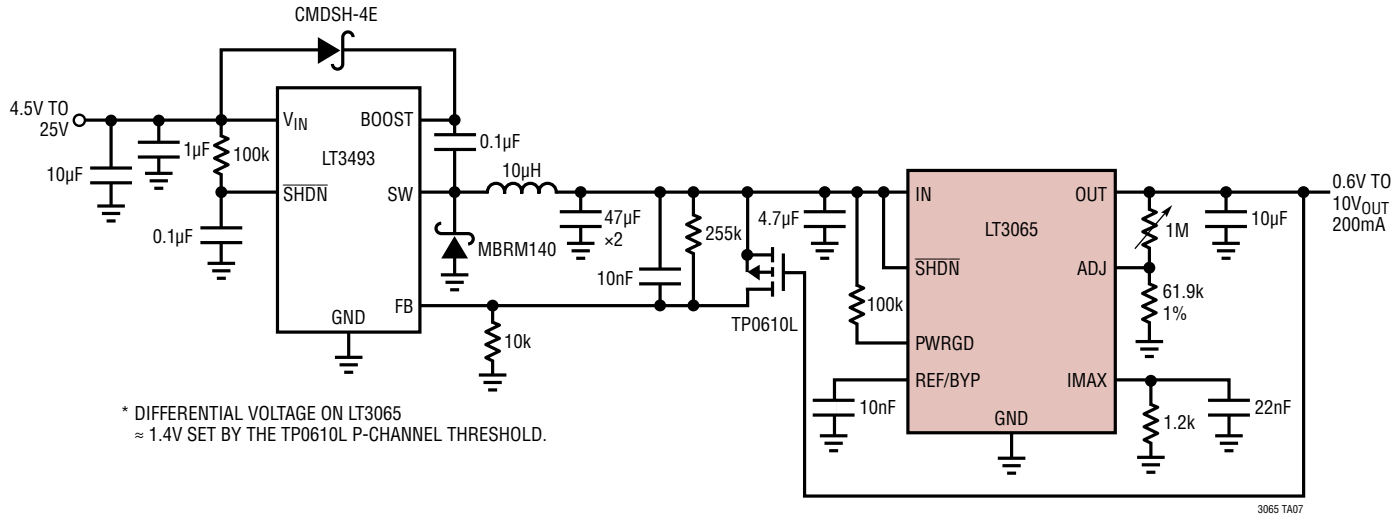
TYPICAL APPLICATION

Adjustable High Efficiency Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT™ Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, SO-8 and 3mm × 4mm DFN Packages
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1964	200mA, Low Noise Negative LDO	V_{IN} = –2.2V to –20V, $V_{OUT(MIN)}$ = –1.21V, V_{DO} = 0.34V, I_Q = 30µA, I_{SD} = 3µA, Low Noise <30µV_{RMS}, Stable with Ceramic Capacitors, ThinSOT and 3mm × 3mm DFN Packages
LT1965	1.1A, Low Noise LDO	290mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 1.8V to 20V, V_{OUT} = 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DD-Pak, MSOP and 3mm × 3mm DFN Packages
LT3050	100mA LDO with Diagnostics and Precision Current Limit	340mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.6V to 45V, 3mm × 2mm DFN and MSOP Packages
LT3055	500mA LDO with Diagnostics and Precision Current Limit	350mV Dropout Voltage, Low Noise: 25µV_{RMS}, V_{IN} = 1.6V to 45V, 4mm × 3mm DFN and MSOP Packages
LT3060	100mA Low Noise LDO with Soft-Start	300mV Dropout Voltage, Low Noise: 30µV_{RMS}, V_{IN} = 1.6V to 45V, 2mm × 2mm DFN and ThinSOT Packages
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise LDO	300mV Dropout Voltage (2-Supply Operation), Low Noise 40µV_{RMS}, V_{IN} = 1.2V to 36V, V_{OUT} = 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable, Stable with Ceramic Capacitors, TO-220, SOT-223, MSOP and 3mm × 3mm DFN
LT3082	200mA, Parallelable, Low Noise LDO	Outputs may be Paralleled for Higher Output Current or Heat Spreading, Wide Input Voltage Range: 1.2V to 40V, Low Value Input/Output Capacitors Required: 2.2µF, Single Resistor Sets Output Voltage, 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages
LT3085	500mA, Parallelable, Low Noise LDO	275mV Dropout Voltage (2-Supply Operation), Low Noise 40µV_{RMS}, V_{IN} = 1.2V to 36V, V_{OUT} = 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set, Directly Parallelable, Stable with Ceramic Capacitors, MS8E and 2mm × 3mm DFN-6 Packages

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