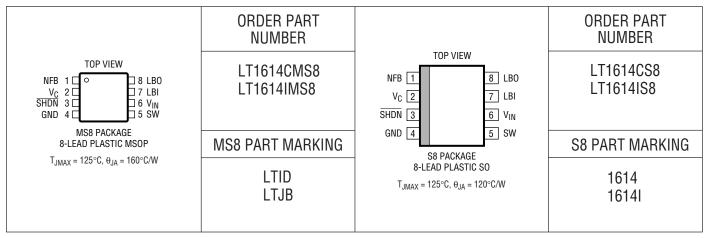
ABSOLUTE MAXIMUM RATINGS (Note 1)

V _{IN} , SHDN, LBO Voltage	12V
SW Voltage	0.4V to 30V
NFB Voltage	–3V
V _C Voltage	2V
LBI Voltage	$0V \le V_{LBI} \le 1V$
Current into FB Pin	±1mA
Junction Temperature	125°C

Operating Temperature Range
LT1614C 0°C to 70°C
LT1614I –40°C to 85°C
Extended Commercial
Temperature Range (Note 2)40°C to 85°C
Storage Temperature Range65°C to 150°C
Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION



Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS The \bullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Commercial Grade 0°C to 70°C. V_{IN} = 1.5V, V_{SHDN} = V_{IN} unless

temperature range, otherwise specifications are at T_A = 25°C. Commercial Grade 0°C to 70°C. V_{IN} = 1.5V, V_{SHDN} = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
Quiescent Current				1	2	mA
	$V_{\overline{SHDN}} = 0V$			5	10	μA
Feedback Voltage		•	-1.21	-1.24	-1.27	V
NFB Pin Bias Current (Note 3)	$V_{NFB} = -1.24V$	•	-2.5	-4.5	-7	μA
Reference Line Regulation	$1V \le V_{IN} \le 2V$			0.6	1.1	%/V
	$2V \le V_{IN} \le 6V$			0.3	0.8	%/V
Minimum Input Voltage				0.92	1	V
Maximum Input Voltage		•			6	V
Error Amp Transconductance	$\Delta I = 5 \mu A$			16		µmhos
Error Amp Voltage Gain				100		V/V
Switching Frequency		•	500	600	750	kHz
Maximum Duty Cycle			73	80		%
		•	70	80		%
Switch Current Limit (Note 4)			0.75	1.2		A



ELECTRICAL CHARACTERISTICS The \bullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Commercial Grade 0°C to 70°C. V_{IN} = 1.5V, V_{SHDN} = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
Switch V _{CESAT}	I _{SW} = 500mA (25°C, 0°C) I _{SW} = 500mA (70°C)			295	350 400	mV mV
Shutdown Pin Current	$V_{\overline{SHDN}} = V_{IN}$ $V_{\overline{SHDN}} = OV$			10 -5	20 -10	μΑ μΑ
LBI Threshold Voltage		•	190 185	200	210 215	mV mV
LBO Output Low	I _{SINK} = 10μΑ			0.1	0.25	V
LBO Leakage Current	V _{LBI} = 250mV, V _{LBO} = 5V			0.01	0.1	μA
LBI Input Bias Current (Note 5)	V _{LBI} = 150mV			10	50	nA
Low-Battery Detector Gain	1MΩ Load			1000		V/V
Switch Leakage Current	V _{SW} = 5V			0.01	3	μA

Industrial Grade –40°C to 85°C. V_{IN} = 1.5V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted.

PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
Quiescent Current				1	2	mA
	V _{SHDN} = 0V			5	10	μΑ
Feedback Voltage		•	-1.21	-1.24	-1.27	V
NFB Pin Bias Current (Note 3)	$V_{NFB} = -1.24V$	•	-2	-4.5	-7.5	μA
Reference Line Regulation	$\begin{array}{l} 1V \leq V_{IN} \leq 2V \\ 2V \leq V_{IN} \leq 6V \end{array}$			0.6 0.3	1.1 0.8	%/V %/V
Minimum Input Voltage	−40°C 85°C			1.1 0.8	1.25 1.0	V V
Maximum Input Voltage		•			6	V
Error Amp Transconductance	ΔI = 5μA			16		µmhos
Error Amp Voltage Gain				100		V/V
Switching Frequency		•	500	600	750	kHz
Maximum Duty Cycle		•	70	80		%
Switch Current Limit (Note 4)			0.75	1.2		A
Switch V _{CESAT}	I _{SW} = 500mA (-40°C) I _{SW} = 500mA (85°C)			250 330	350 400	mV mV
Shutdown Pin Current	$V_{\overline{SHDN}} = V_{IN}$ $V_{\overline{SHDN}} = 0V$			10 -5	20 -10	μΑ μΑ
LBI Threshold Voltage		•	180	200	220	mV
LBO Output Low	I _{SINK} = 10μA			0.1	0.25	V
LBO Leakage Current	V _{LBI} = 250mV, V _{LBO} = 5V			0.1	0.3	μA
LBI Input Bias Current (Note 5)	V _{LBI} = 150mV			5	30	nA
Low-Battery Detector Gain	1MΩ Load			1000		V/V
Switch Leakage Current	V _{SW} = 5V			0.01	3	μA

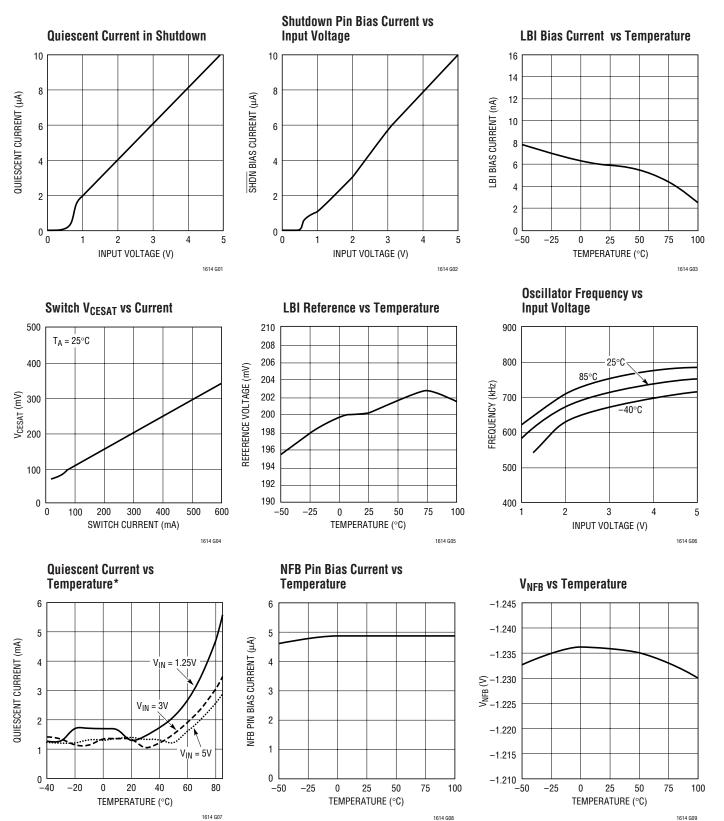
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 3: Bias current flows out of NFB pin.

Note 2: The LT1614C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at -40°C and 85°C. The LT1614I is guaranteed to meet the extended temperature limits.

Note 4: Switch current limit guaranteed by design and/or correlation to static tests. Duty cycle affects current limit due to ramp generator. Note 5: Bias current flows out of LBI pin.

TYPICAL PERFORMANCE CHARACTERISTICS



*Includes diode leakage





PIN FUNCTIONS

NFB (Pin 1): Negative Feedback Pin. Reference voltage is -1.24V. Connect resistive divider tap here. The suggested value for R2 is 24.9k. Set R1 and R2 according to:

$$R1 = \frac{|V_{OUT}| - 1.24}{\frac{1.24}{R2} + \left(4.5 \bullet 10^{-6}\right)}$$

 V_C (Pin 2): Compensation Pin for Error Amplifier. Connect a series RC from this pin to ground. Typical values are 100k Ω and 1nF. Minimize trace area at V_C .

SHDN (Pin 3): Shutdown. Ground this pin to turn off switcher. Must be tied to V_{IN} (or higher voltage) to enable switcher. Do not float the SHDN pin.

GND (Pin 4): Ground. Connect directly to local ground plane.

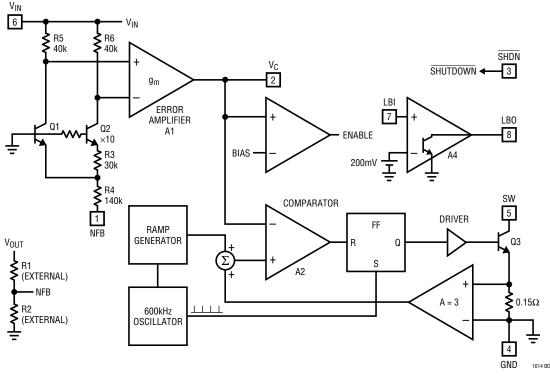
SW (Pin 5): Switch Pin. Minimize trace area at this pin to keep EMI down.

 V_{IN} (Pin 6): Supply Pin. Must have 1µF ceramic bypass capacitor right at the pin, connected directly to ground.

LBI (Pin 7): Low-Battery Detector Input. 200mV reference. Voltage on LBI must stay between ground and 700mV. Float this pin if not used.

LBO (Pin 8): Low-Battery Detector Output. Open collector, can sink 10μ A. A 1M Ω pull-up is recommended. Float this pin if not used. The low-battery detector is disabled when SHDN is low. LBO is high-Z in this state.

BLOCK DIAGRAM







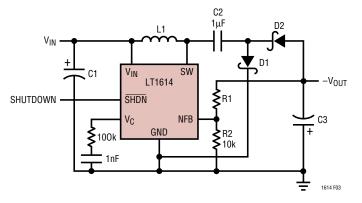
The LT1614 combines a current mode, fixed frequency PWM architecture with a -1.23V reference to directly regulate negative outputs. Operation can be best understood by referring to the block diagram of Figure 2. Q1 and Q2 form a bandgap reference core whose loop is closed around the output of the converter. The driven reference point is the lower end of resistor R4, which normally sits at a voltage of -1.23V. As the load current changes, the NFB pin voltage also changes slightly, driving the output of gm amplifier A1. Switch current is regulated directly on a cycle-to-cycle basis by A1's output. The flip-flop is set at the beginning of each cycle, turning on the switch. When the summation of a signal representing switch current and a ramp generator (introduced to avoid subharmonic oscillations at duty factors greater than 50%) exceeds the V_{C} signal, comparator A2 changes stage, resetting the flipflop and turning off the switch. Output voltage decreases (the magnitude increases) as switch current is increased. The output, attenuated by external resistor divider R1 and R2, appears at the NFB pin, closing the overall loop. Frequency compensation is provided externally by a series RC connected from the V_{C} pin to ground. Typical values are 100k and 1nF. Transient response can be tailored by adjustment of these values.

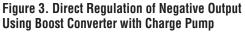
As load current is decreased, the switch turns on for a shorter period each cycle. If the load current is further decreased, the converter will skip cycles to maintain output voltage regulation.

The LT1614 can work in either of two topologies. The simpler topology appends a capacitive level shift to a boost converter, generating a negative output voltage, which is directly regulated. The circuit schematic is detailed in Figure 3. Only one inductor is required, and the two diodes can be in a single SOT-23 package. Output noise is the same as in a boost converter, because current is delivered to the output only during the time when the LT1614's internal switch is on.

If D2 is replaced by an inductor, as shown in Figure 4, a higher performance solution results. This converter topology was developed by Professor S. Cuk of the California Institute of Technology in the 1970s. A low ripple voltage results with this topology due to inductor L2 in series with the output. Abrupt changes in output capacitor current are eliminated because the output inductor delivers current to the output during both the off-time and the on-time of the LT1614 switch. With proper layout and high quality output capacitors, output ripple can be as low as $1mV_{P-P}$.

The operation of Cuk's topology is shown in Figures 5 and 6. During the first switching phase, the LT1614's switch, represented by Q1, is on. There are two current loops in operation. The first loop begins at input capacitor C1, flows through L1, Q1 and back to C1. The second loop flows from output capacitor C3, through L2, C2, Q1 and back to C3. The output current from R_{LOAD} is supplied by L2 and C3. The voltage at node SW is V_{CESAT} and at node SWX the voltage is $-(V_{IN} + |V_{OUT}|)$. Q1 must conduct both L1 and L2 current. C2 functions as a voltage level shifter, with an approximately constant voltage of $(V_{IN} + |V_{OUT}|)$ across it.





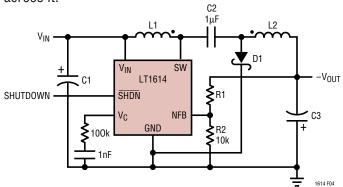


Figure 4. L2 Replaces D2 to Make Low Output Ripple Inverting Topology. Coupled or Uncoupled Inductors Can Be Used. Follow Phasing If Coupled for Best Results



When Q1 turns off during the second phase of switching, the SWX node voltage abruptly increases to $(V_{IN} + |V_{OUT}|)$. The SW node voltage increases to V_D (about 350mV). Now current in the first loop, begining at C1, flows through L1, C2, D1 and back to C1. Current in the second loop flows from C3 through L2, D1 and back to C3. Load current continues to be supplied by L2 and C3.

An important layout issue arises due to the chopped nature of the currents flowing in Q1 and D1. If they are both tied directly to the ground plane before being combined, switching noise will be introduced into the ground plane. It is almost impossible to get rid of this noise, once present in the ground plane. The solution is to tie D1's cathode to the ground pin of the LT1614 before the combined currents are dumped into the ground plane as drawn in Figures 4, 5 and 6. This single layout technique can virtually eliminate high frequency "spike" noise so often present on switching regulator outputs.

Output ripple voltage appears as a triangular waveform riding on V_{OUT} . Ripple magnitude equals the ripple current of L2 multiplied by the equivalent series resistance (ESR) of output capacitor C3. Increasing the inductance of L1 and L2 lowers the ripple current, which leads to lower output voltage ripple. Decreasing the ESR of C3, by using ceramic or other low ESR type capacitors, lowers output ripple voltage. Output ripple voltage can be reduced to arbitrarily low levels by using large value inductors and low ESR, high value capacitors.

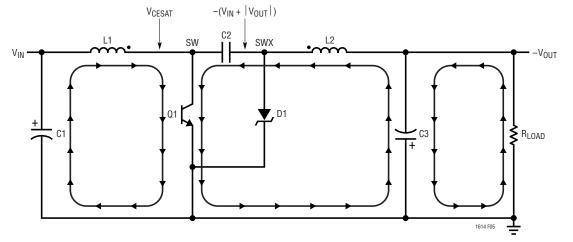


Figure 5. Switch-On Phase of Inverting Converter. L1 and L2 Current Have Positive dI/dt

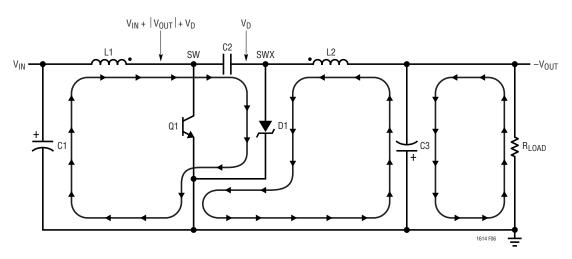


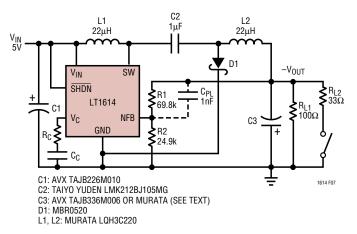
Figure 6. Switch-Off Phase of Inverting Converter. L1 and L2 Current Have Negative dl/dt



Transient Response

The inverting architecture of the LT1614 can generate a very low ripple output voltage. Recently available high value ceramic capacitors can be used successfully in LT1614 designs. The addition of a phase lead capacitor, C_{PL} , reduces output perturbations due to load steps when lower value ceramic capacitors are used and connected in parallel with feedback resistor R1. Figure 7 shows an LT1614 inverting converter with resistor loads R_{L1} and R_{L2} . R_{L1} is connected across the output, while R_{L2} is switched in externally via a pulse generator. Output voltage waveforms are pictured in subsequent figures, illustrating the performance of output capacitor type.

Figure 8 shows the output voltage with a 50mA to 200mA load step, using an AVX TAJ "B" case 33μ F tantalum capacitor at the output. Output perturbation is approximately 250mV as the load changes from 50mA to 200mA. Steady-state ripple voltage is $40mV_{P-P}$, due to L1's ripple current and C3's ESR. Figure 9 pictures the output voltage and switch pin voltage at 500ns per division. Note the absence of high frequency spikes at the output. This is easily repeatable with proper layout, described in the next section.





In Figure 10, output capacitor C3 is replaced by a ceramic unit. These large value capacitors have ESR of $2m\Omega$ or less and result in very low output ripple. A 1nF capacitor, C_{PL}, connected across R1 reduces output perburbation due to load step. This keeps the output voltage within 5% of steady-state value. Figure 11 pictures the output and switch nodes at 500ns per division. Output ripple is about $5mV_{P-P}$. Again, good layout is essential to achieve this low noise performance.

Layout

The LT1614 switches current at high speed, mandating careful attention to layout for best performance. *You will not get advertised performance with careless layout.* Figure 12 shows recommended component placement. Follow this closely in your printed circuit layout. The cut ground copper at D1's cathode is essential to obtain the low noise achieved in Figures 10 and 11's oscillographs. Input bypass capacitor C1 should be placed close to the LT1614 as shown. The load should connect directly to output capacitor C2 for best load regulation. You can tie the local ground into the system ground plane at C3's ground terminal.

COMPONENT SELECTION

Inductors

Each of the two inductors used with the LT1614 should have a saturation current rating (where inductance is approximately 70% of zero current inductance) of approximately 0.4A or greater. If the device is used in "charge pump" mode, where there is only one inductor, then its rating should be 0.75A or greater. DCR of the inductors should be 0.4Ω or less. 22μ H inductors are called out in the applications schematics because these Murata units are physically small and inexpensive. Increasing the inductance will lower ripple current, increasing available output current. A coupled inductor of 33µH, such as Coiltronics CTX33-2, will provide 290mA at -5V from a 5V input. Inductance can be reduced if operating from a supply voltage below 3V. Table 1 lists several inductors that will work with the LT1614, although this is not an exhaustive list. There are many magnetics vendors whose components are suitable.



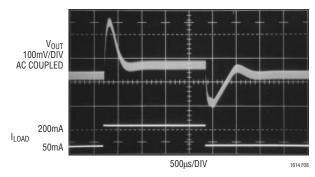


Figure 8. Load Step Response of LT1614 with 33 μF Tantalum Output Capacitor

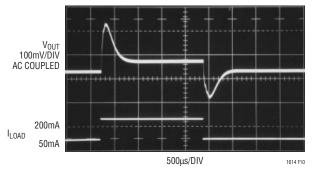


Figure 10. Replacing C3 with 22 μ F Ceramic Capacitor Lowers Output Voltage Ripple. 1nF Phase-Lead Capacitor in Parallel with R1 Lowers Transient Excursion

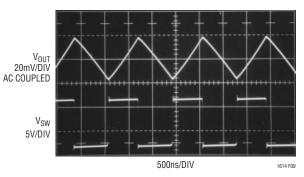


Figure 9. 33 μ F "B" Case Tantalum Capacitor Has ESR Resulting in 40mV_{P-P} Voltage Ripple at Output with 200mA Load

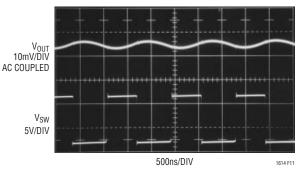


Figure 11. 22 μF Ceramic Capacitor at Output Reduces Output Ripple Voltage

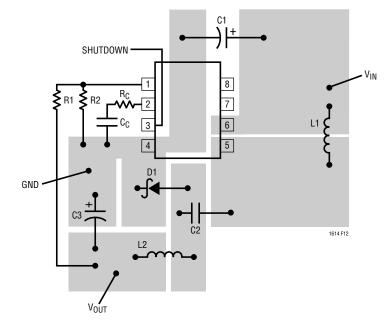


Figure 12. Suggested Component Placement. Note: Cut in Ground Copper at D1's Cathode



Capacitors

As described previously, ceramic capacitors can be used with the LT1614. For lower cost applications, small tantalum units can be used. A value of 22μ F is acceptable, although larger capacitance values can be used. ESR is the most important parameter in selecting an output capacitor. The "flying" capacitor (C2 in the schematic figures) should be a 1μ F ceramic type. An X5R or X7R dielectric should be used to avoid capacitance decreasing severely with applied voltage. The input bypass capacitor is less

critical, and either tantalum or ceramic can be used with little trade-off in circuit performance. Some capacitor types appropriate for use with the LT1614 are listed in Table 2.

Diodes

A Schottky diode is recommended for use with the LT1614. The Motorola MBR0520 is a very good choice. Where the input to output voltage differential exceeds 20V, use the MBR0530 (a 30V diode).

Table 1. Inductor Vendors

VENDOR	PHONE	URL	PART	COMMENT
Sumida	(847) 956-0666	www.sumida.com	CLS62-22022 CD43-470	22μH Coupled 47μH
Murata	(404) 436-1300	www.murata.com	LQH3C-220	22µH, 2mm Height
Coiltronics	(407) 241-7876	www.coiltronics.com	CTX20-1	20µH Coupled, Low DCR

Table 2. Capacitor Vendors

VENDOR	PHONE	URL	PART	COMMENT
Taiyo Yuden	(408) 573-4150	www.t-yuden.com	Ceramic Caps	X5R Dielectric
AVX	(803) 448-9411	www.avxcorp.com	Ceramic Caps Tantalum Caps	
Murata	(404) 436-1300	www.murata.com	Ceramic Caps	





APPLICATIONS INFORMATION

Shutdown Pin

The LT1614 has a Shutdown pin (\overline{SHDN}) that must be grounded to shut the device down or tied to a voltage equal or greater than V_{IN} to operate. The shutdown circuit is shown in Figure 13.

Note that allowing SHDN to float turns on both the startup current (Q2) and the shutdown current (Q3) for $V_{IN} > 2V_{BE}$. The LT1614 doesn't know what to do in this situation and behaves erratically. SHDN voltage above V_{IN} is allowed. This merely reverse-biases Q3's base emitter junction, a benign condition. The low-battery detector is disabled when SHDN is low.

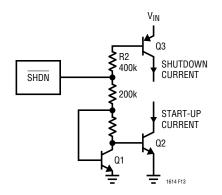
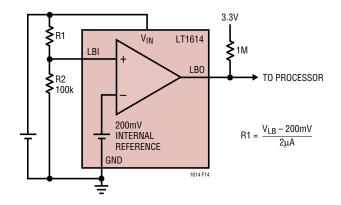


Figure 13. Shutdown Circuit

Low-Battery Detector

The LT1614's low-battery detector is a simple PNP input gain stage with an open collector NPN output. The negative input of the gain stage is tied internally to a 200mV reference. The positive input is the LBI pin. Arrangement as a low-battery detector is straightforward. Figure 14 details hookup. R1 and R2 need only be low enough in value so that the bias current of the LBI pin doesn't cause large errors. For R2, 100k is adequate. The 200mV reference can also be accessed as shown in Figure 15. The lowbattery detect is not operative when the device is shut down.





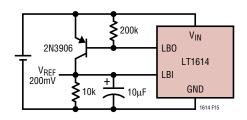


Figure 15. Accessing 200mV Reference

Coupled Inductors

The applications shown in this data sheet use two uncoupled inductors because the Murata units specified are small and inexpensive. This topology can also be used with a coupled inductor as shown in Figure 16. Be sure to get the phasing right.

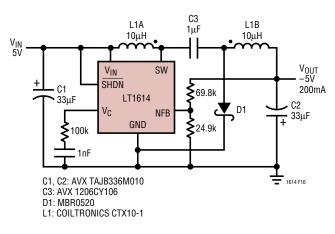
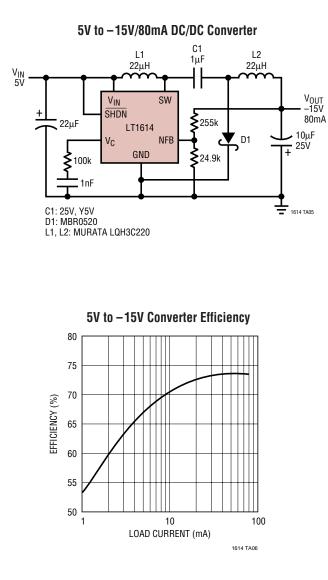


Figure 16. 5V to -5V Converter with Coupled Inductor

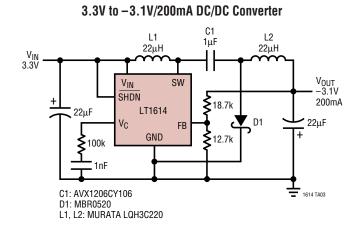


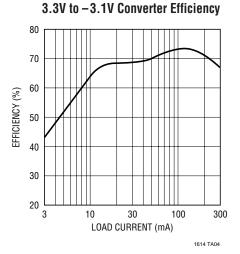
TYPICAL APPLICATIONS





TYPICAL APPLICATIONS

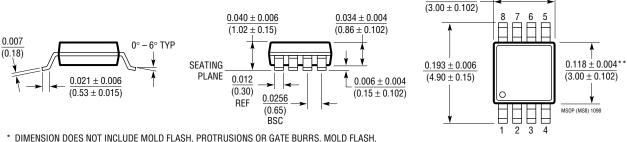






PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package 8-Lead Plastic MSOP (LTC DWG # 05-08-1660)



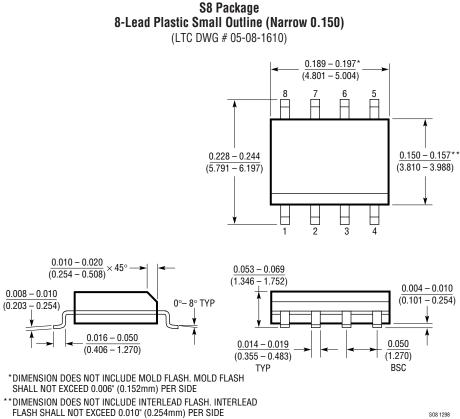
 $0.118 \pm 0.004^{*}$

* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE



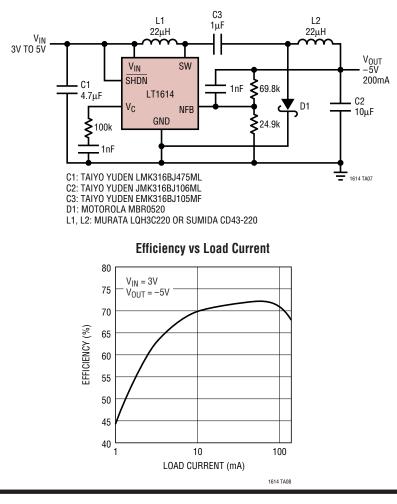
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.







TYPICAL APPLICATIONS



5V to -5V Converter Uses All Ceramic Capacitors

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC [®] 1174	High Efficiency Step-Down and Inverting DC/DC Converter	Selectable I _{PEAK} = 300mA or 600mA
LT1307	Single Cell Micropower 600kHz PWM DC/DC Converter	3.3V at 75mA from 1 Cell, MSOP Package
LT1308	Single Cell High Current Micropower 600kHz Boost Converter	5V at 1A from a Single Li-Ion Cell, SO-8 Package
LT1316	Micropower Boost DC/DC Converter	Programmable Peak Current Limit, MSOP Package
LT1317	Micropower 600kHz PWM DC/DC Converter	2 Cells to 3.3V at 200mA, MSOP Package
LTC1474	Low Quiescent Current High Efficiency DC/DC Converter	I _Q = 10μA, Programmable Peak Current Limit, MSOP
LT1610	1.7MHz Single Cell Micropower DC/DC Converter	5V at 200mA from 3.3V, MSOP Package
LT1611	Inverting 1.4MHz Switching Regulator in 5-Lead SOT-23	-5V at 150mA from 5V Input, Tiny SOT-23 Package
LT1613	1.4MHz Switching Regulator in 5-Lead SOT-23	5V at 200mA from 3.3V Input, Tiny SOT-23 Package
LT1615	Micropower Constant Off-Time DC/DC Converter in 5-Lead SOT-23	20V at 12mA from 2.5V, Tiny SOT-23 Package
LT1617	Micropower Inverting DC/DC Converter in 5-Lead SOT-23	–15V at 12mA from 2.5V, Tiny SOT-23 Package
LT1930	1.2MHz Boost DC/DC Converter in 5-Lead SOT-23	5V at 480mA from 3.3V Input, V _{OUT} Up to 34V
LT1931	1.2MHz Inverting DC/DC Converter in 5-Lead SOT-23	–5V at 350mA from 5V Input, 1mV _{P-P} Output Ripple