ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- Power Supply Voltage ($12V_{IN}$) ..... –0.3V to 20V
- Topside Supply Voltage (V_{BOOST})
  - V_{TS} – 0.3V to V_{TS} + 20V (V_{MAX} = 75V)
- Topside Reference Pin Voltage (TS) ..... –0.3V to 60V

Input Voltages
- Sense Amplifier Input Common Mode ... –0.3V to 60V
- RUN/SHDN Pin Voltage ..... –0.3V to $12V_{IN}$
- All Other Inputs ..... –0.3V to 7V

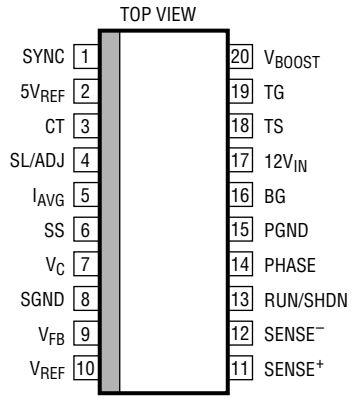
Maximum Currents
- 5V Reference Output Current 65mA

Maximum Temperatures
- Operating Ambient Temperature Range
  - LT1339C ..... 0°C to 70°C
  - LT1339I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 20-LEAD PDIP

SW PACKAGE 20-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)

T_{JMAX} = 125°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER

LT1339CN
LT1339CSW
LT1339IN
LT1339ISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$12V_{IN}$ = V_{BOOST} = 12V, V_C = 2V, TS = 0V, V_{FB} = V_{REF} = 1.25V, C_{TG} = C_{BG} = 3000pF, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Protection							
I_{12VIN}	DC Active Supply Current (Note 2) DC Standby Supply Current	 $V_{RUN/SHDN}$ < 0.5V	● ●		14 150	20 250	mA µA
I_{BOOST}	DC Active Supply Current (Note 2) DC Standby Supply Current	 $V_{RUN/SHDN}$ < 0.5V			2.2 0		mA µA
$V_{RUN/SHDN}$	Shutdown Rising Threshold		●	1.15	1.25	1.35	V
V_{SSHYST}	Shutdown Threshold Hysteresis				25		mV
I_{SS}	Soft Start Charge Current		●	4	8	14	µA
V_{UVLO}	Undervoltage Lockout Threshold - Falling Undervoltage Lockout Threshold - Rising Undervoltage Lockout Hysteresis		● ● ●	8.20 200	9.00 9.35 350	9.75 9.95	V V mV
5V Reference							
V_{REF5}	5V Reference Voltage	Line, Load and Temperature	●	4.75	5.00	5.25	V
	5V Reference Line Regulation	10V ≤ $12V_{IN}$ ≤ 15V	●		3	5	mV/V
I_{REF5}	5V Reference Load Range - DC Pulse		● ●			10 20	mA mA
	5V Reference Load Regulation	0 ≤ I_{REF5} ≤ 20mA	●		–1.25	–2	V/A
I_{SC}	5V Reference Short-Circuit Current				45		mA

ELECTRICAL CHARACTERISTICS

$12V_{IN} = V_{BOOST} = 12V$, $V_C = 2V$, TS = 0V, $V_{FB} = V_{REF} = 1.25V$, $C_{TG} = C_{BG} = 3000pF$, $T_A = 25°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier							
V_{FB}	Error Amplifier Reference Voltage	Measured at Feedback Pin	 ●	1.242 1.235	1.250 1.250	1.258 1.265	V V
I_{FB}	Feedback Input Current	$V_{FB} = V_{REF}$	●	0.1	0.5	1.0	µA
g_m	Error Amplifier Transconductance		●	1200	2000	3200	µmho
A_V	Error Amplifier Voltage Gain		●	1500	3000		V/V
I_{VC}	Error Amplifier Source Current Error Amplifier Sink Current	 $V_{FB} - V_{REF} = 500mV$	● ●	200 280	275 400		µA µA
V_{VC}	Absolute V_C Clamp Voltage	Measured at V_C Pin			3.5		V
V_{SENSE}	Peak Current Limit Threshold Average Current Limit Threshold (Note 4)	Measured at Sense Inputs Measured at Sense Inputs	● ●	170 110	190 120	 130	mV mV
V_{IAVG}	Average Current Limit Threshold	Measured at I_{AVG} Pin			2.5		V
Current Sense Amplifier							
A_V	Amplifier DC Gain	Measured at I_{AVG} Pin			15		V/V
V_{OS}	Amplifier Input Offset Voltage	$2V < V_{CMSENSE} < 60V$, $SENSE^+ - SENSE^- = 5mV$	●	0.1			mV
I_B	Input Bias Current	Sink ($V_{CMSENSE} > 5V$) Source ($V_{CMSENSE} = 0V$)	● ●		45 700	75 1200	µA µA
Oscillator							
f_O	Operating Frequency, Free Run Frequency Programming Error (Note 3)	 $f_O \leq 150kHz$	● ●	 –5		150 5	kHz %
I_{CT}	Timing Capacitor Discharge Current	LT1339C LT1339I	● ●	2.20 2.10	2.50 2.50	2.75 2.75	mA mA
V_{SYNC}	SYNC Input Threshold	Rising Edge	●	0.8		2.0	V
f_{SYNC}	SYNC Frequency Range	$f_{SYNC} \leq 150kHz$	●	f_O		$1.4f_O$	
Output Drivers							
$V_{TG,BG}$	Undervoltage Output Clamp Standby Mode Output Clamp	$12V_{IN} \leq 8V$ $V_{RUN} < 0.5V$	● ●		0.4	0.7 0.1	V V
V_{TG}	Top Gate On Voltage Top Gate Off Voltage		● ●	11.0	11.9 0.4	12.0 0.7	V V
t_{TGR}	Top Gate Rise Time		●		130	200	ns
t_{TGF}	Top Gate Fall Time		●		60	140	ns
V_{BG}	Bottom Gate On Voltage Bottom Gate Off Voltage		● ●	11.0	11.9 0.4	12.0 0.7	V V
t_{BGR}	Bottom Gate Rise Time		●		70	200	ns
t_{BGF}	Bottom Gate Fall Time		●		60	140	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

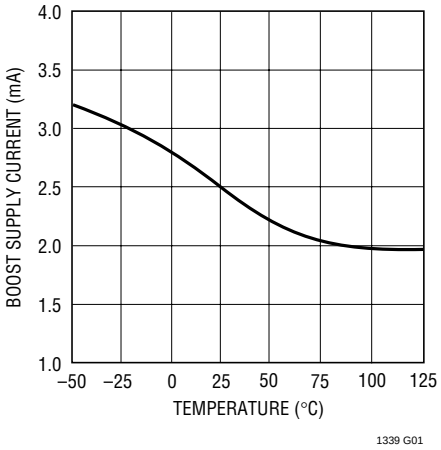
Note 2: Supply current specification does not include external FET gate charge currents. Actual supply currents will be higher and vary with operating frequency, operating voltages and the type of external FETs used. See Application Information section.

Note 3: Test condition: $R_{CT} = 16.9k$, $C_{CT} = 1000pF$.

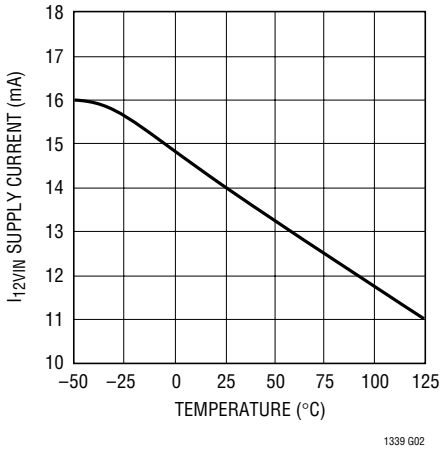
Note 4: Test Condition: $V_{CMSENSE} = 10V$.

TYPICAL PERFORMANCE CHARACTERISTICS

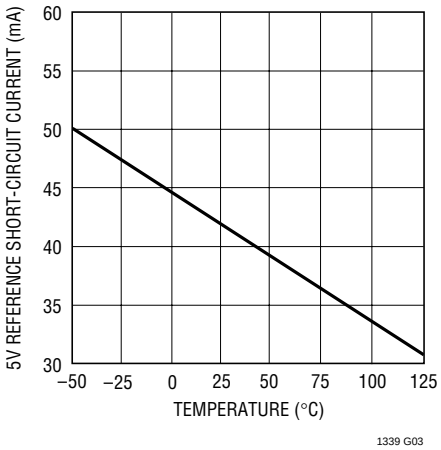
Boost Supply Current vs Temperature



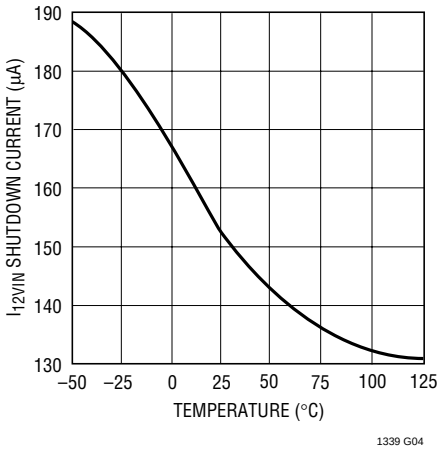
$12V_{IN}$ Supply Current vs Temperature



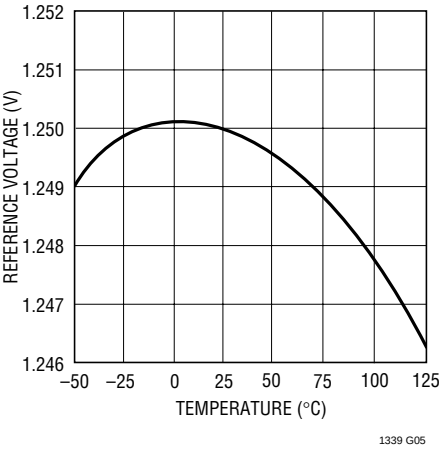
5V Reference Short-Circuit Current vs Temperature



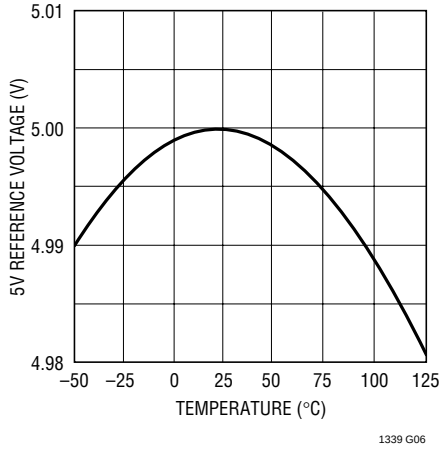
I_{12VIN} Shutdown Current vs Temperature



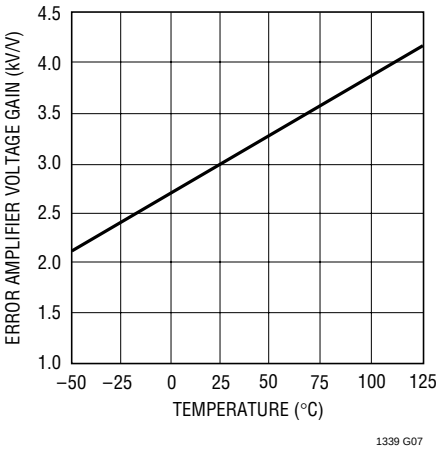
Reference Voltage vs Temperature



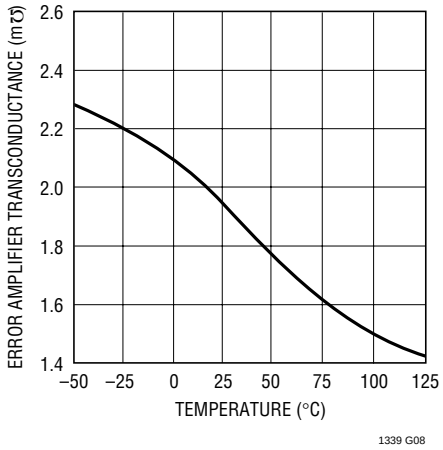
5V Reference Voltage vs Temperature



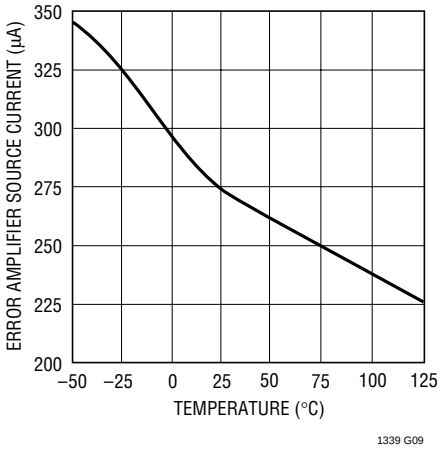
Error Amplifier Voltage Gain vs Temperature



Error Amplifier Transconductance vs Temperature

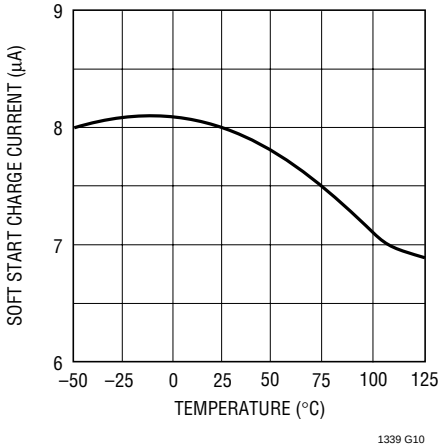


Error Amplifier Maximum Source Current vs Temperature

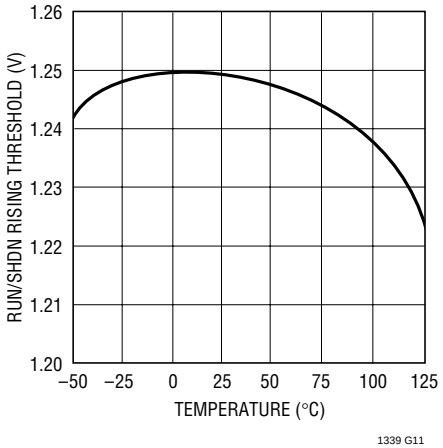


TYPICAL PERFORMANCE CHARACTERISTICS

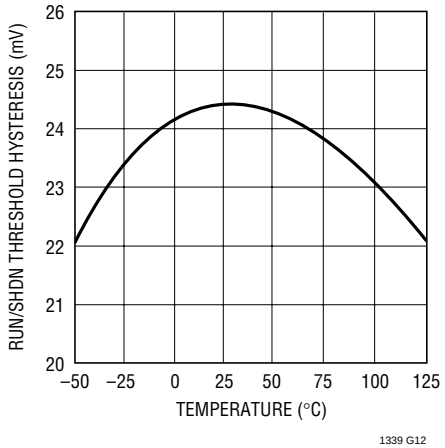
Soft Start Charge Current vs Temperature



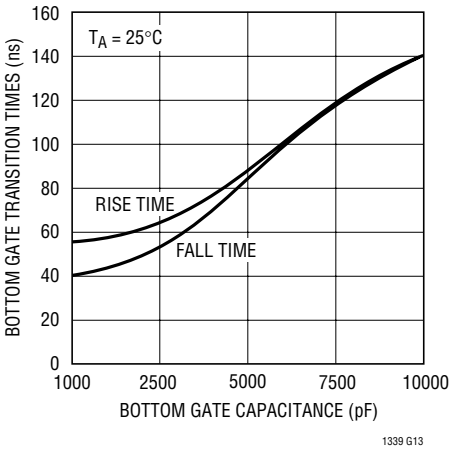
RUN/SHDN Rising Threshold vs Temperature



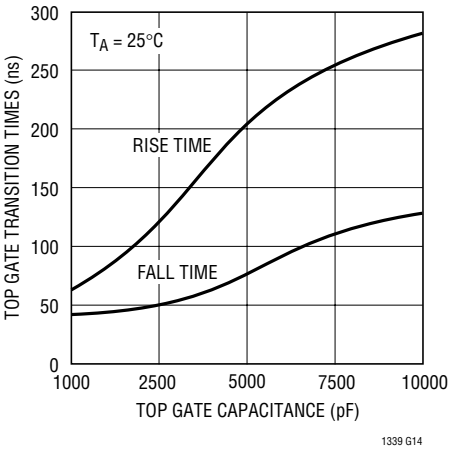
RUN/SHDN Threshold Hysteresis vs Temperature



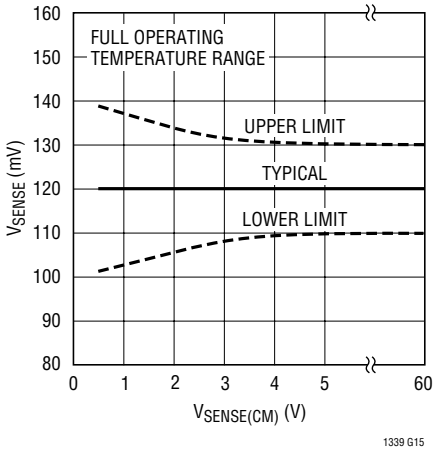
Bottom Gate Transition Times vs Bottom Gate Capacitance



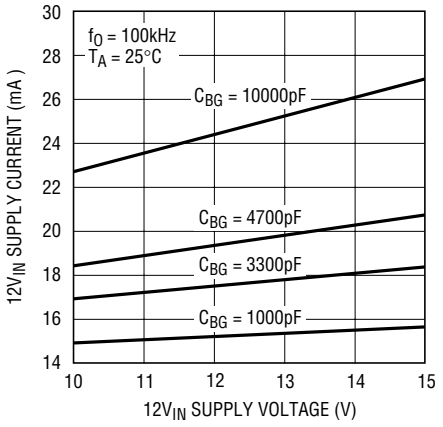
Top Gate Transition Times vs Top Gate Capacitance



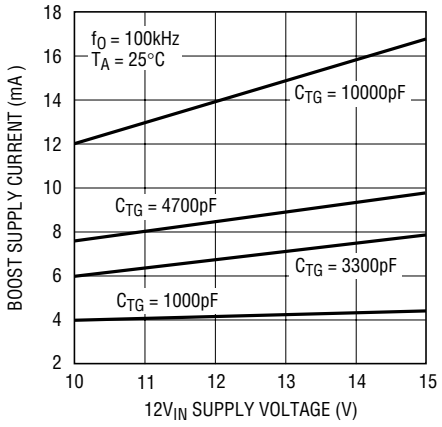
Average Current Limit Threshold Sense Voltage Tolerance vs Common Mode Voltage



$12V_{IN}$ Supply Current vs Supply Voltage

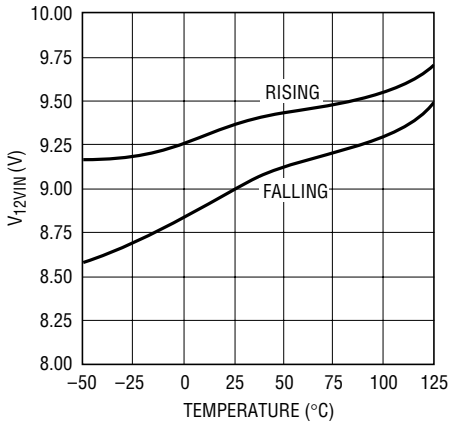


Boost Supply Current vs $12V_{IN}$ Supply Voltage

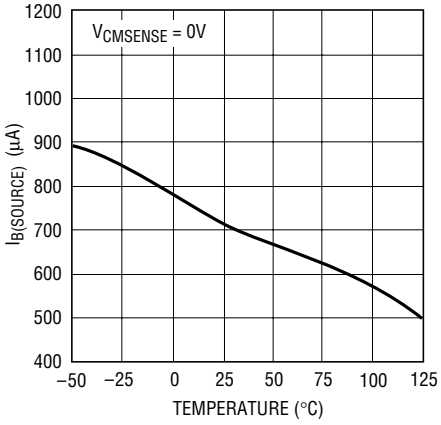


TYPICAL PERFORMANCE CHARACTERISTICS

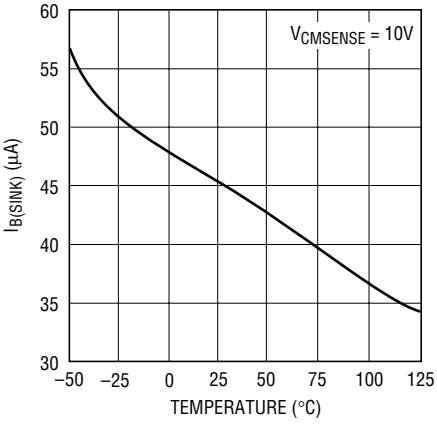
UVLO Thresholds vs Temperature



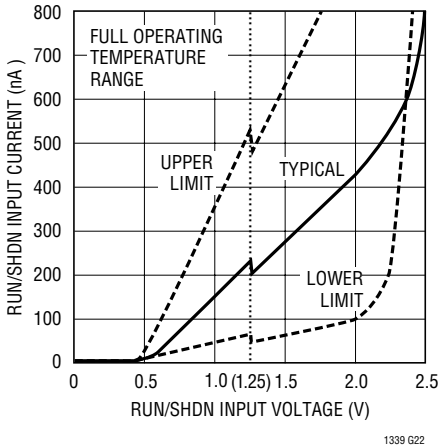
Sense Amplifier Input Bias Current (Source) vs Temperature



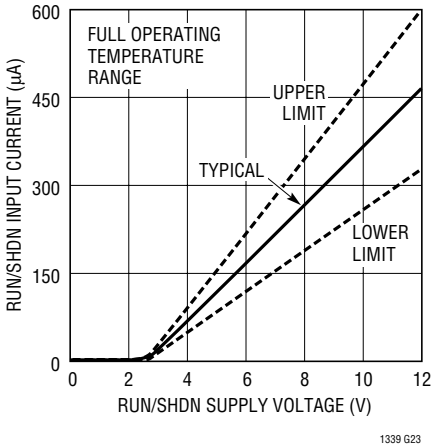
Sense Amplifier Input Bias Current (Sink) vs Temperature



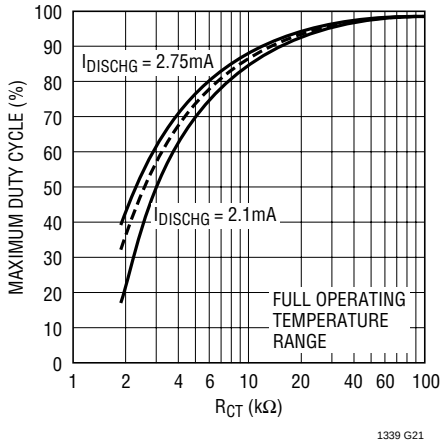
RUN/SHDN Input Current vs Pin Voltage



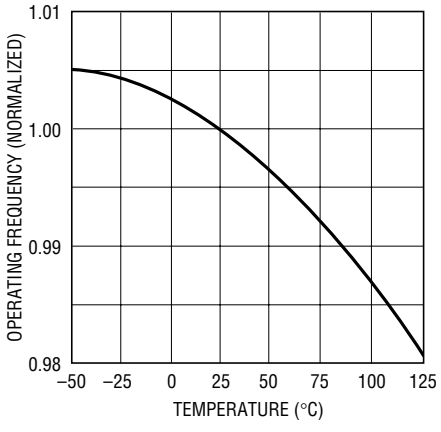
RUN/SHDN Input Current vs Pin Voltage



Maximum Duty Cycle vs R_{CT}



Operating Frequency (Normalized) vs Temperature



PIN FUNCTIONS

SYNC (Pin 1): Oscillator Synchronization Pin with TTL-Level Compatible Input. Input drives internal rising edge triggered one-shot; sync signal on/off times should be ≥1μs (10% to 90% DC at 100kHz). Does not contain internal pull-up. Connect to SGND if not used.

$5V_{REF}$ (Pin 2): 5V Output Reference. Allows connection of external loads up to 10mA DC. (Reference is not available in shutdown.) Typically bypassed with 1μF capacitor to SGND.

CT (Pin 3): Oscillator Timing Pin. Connect a capacitor (C_{CT}) to ground and a pull-up resistor (R_{CT}) to the $5V_{REF}$ supply. Typical values are CT = 1000pF and 10k ≤ R_{CT} ≤ 30k.

SL/ADJ (Pin 4): Slope Compensation Adjustment. Allows increased slope compensation for certain high duty cycle applications. Resistive loading of the pin increases effective slope compensation. A resistor divider from the $5V_{REF}$ pin can tailor the onset of additional slope compensation to specific regions in each switch cycle. Pin can be floated or connected to $5V_{REF}$ if no additional slope compensation is required. (See Applications Information section for slope compensation details.)

I_{AVG} (Pin 5): Average Current Limit Integration. Frequency response characteristic is set using the 50kΩ output impedance and external capacitor to ground. Averaging roll-off typically set at 1 to 2 orders of magnitude under switching frequency. (Typical capacitor value ~1000pF for f_O = 100kHz.) Shorting this pin to SGND will disable the average current limit function.

SS (Pin 6): Soft Start. Generates ramping threshold for regulator current limit during start-up and after UVLO event by sourcing about 8μA into an external capacitor.

V_C (Pin 7): Error Amplifier Output. RC load creates dominant compensation in power supply regulation feedback loop to provide optimum transient response. (See Applications Information section for compensation details.)

SGND (Pin 8): Small-Signal Ground. Connect to negative terminal of C_{OUT}.

V_{FB} (Pin 9): Error Amplifier Inverting Input. Used as voltage feedback input node for regulator loop. Pin sources about 0.5μA DC bias current to protect from an open feedback path condition.

V_{REF} (Pin 10): Bandgap Generated Voltage Reference Decoupling. Connect a capacitor to signal ground. (Typical capacitor value ~0.1μF.)

$SENSE^+$ (Pin 11): Current Sense Amplifier Inverting Input. Connect to most positive (DC) terminal of current sense resistor.

$SENSE^-$ (Pin 12): Current Sense Amplifier Noninverting Input. Connect to most negative (DC) terminal of current sense resistor.

RUN/SHDN (Pin 13): Precision Referenced Shutdown. Can be used as logic level input for shutdown control or as an analog monitor for input supply undervoltage protection, etc. IC is enabled when RUN/SHDN pin rising edge exceeds 1.25V. About 25mV of hysteresis helps assure stable mode switching. All internal functions are disabled in shutdown mode. If this function is not desired, connect RUN/SHDN to $12V_{IN}$ (typically through a 100k resistor). See Applications Information section.

PHASE (Pin 14): Output Driver Phase Control. If Pin 14 is not connected (floating), the topside driver operates the main switch, with the bottom side driver operating the synchronous switch. Shorting Pin 14 to ground reverses the roles of the output drivers. PHASE is typically shorted to ground for inverting and boost configurations. Positive buck configuration requires the PHASE pin to float. See Applications Information section.

PGND (Pin 15): Power Ground. References the bottom side output switch and internal driver control circuits. Connect with low impedance trace to V_{IN} decoupling capacitor negative (ground) terminal.

BG (Pin 16): Bottom Side Output Driver. Connects to gate of bottom side external power FET.

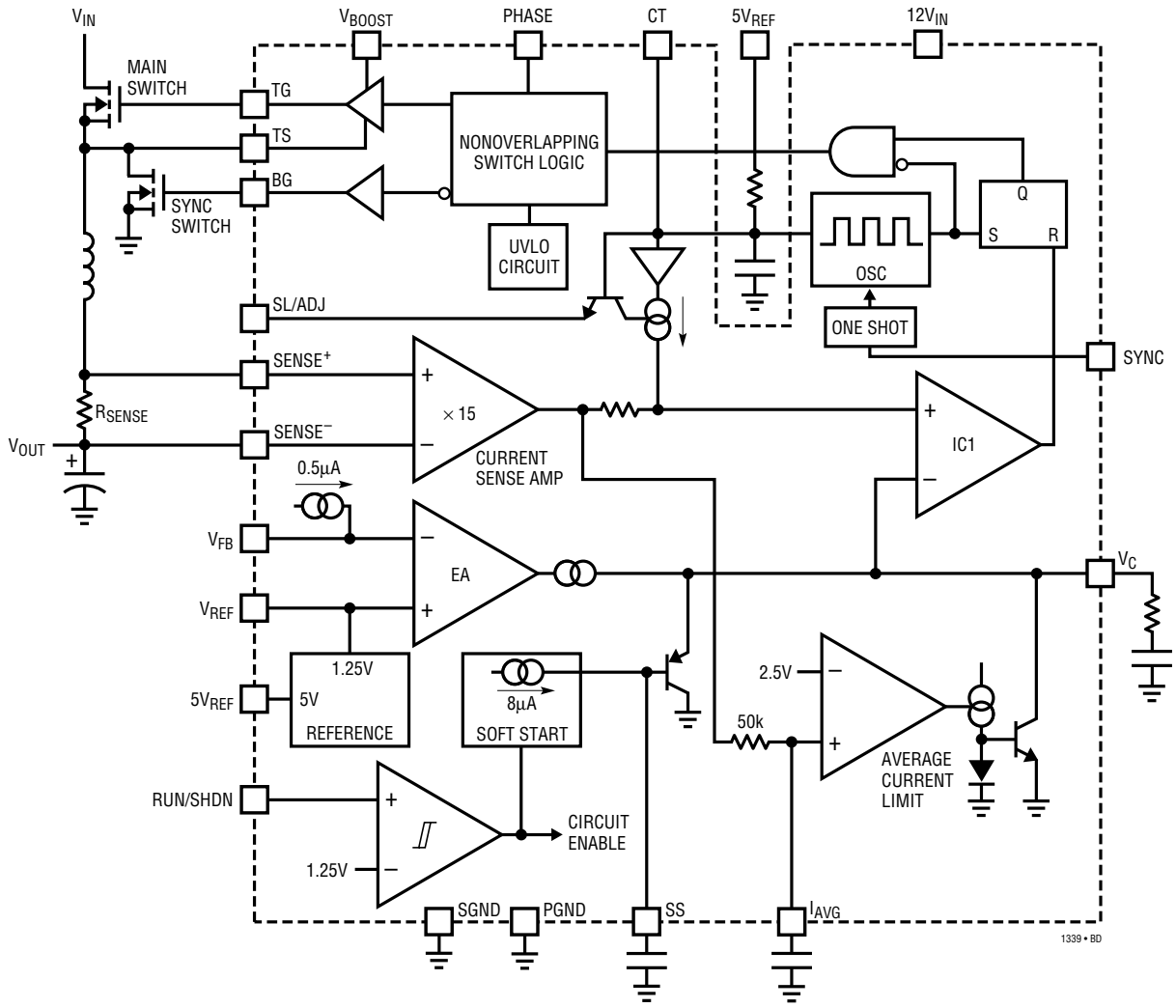
$12V_{IN}$ (Pin 17): 12V Power Supply Input. Bypass with at least 1μF to PGND.

TS (Pin 18): Boost Output Driver Reference. Typically connects to source of topside external power FET and inductive switch node.

TG (Pin 19): Topside (Boost) Output Driver. Connects to gate of topside external power FET.

V_{BOOST} (Pin 20): Topside Power Supply. Bootstrapped via 1μF capacitor tied to switch node (Pin 18) and Schottky diode connected to the $12V_{IN}$ supply.

FUNCTIONAL BLOCK DIAGRAM



OPERATION (Refer to Functional Block Diagram)

Basic Control Loop

The LT1339 uses a constant frequency, current mode synchronous architecture. The timing of the IC is provided through an internal oscillator circuit, which can be synchronized to an external clock, programmable to operate at frequencies up to 150kHz. The oscillator creates a modified sawtooth wave at its timing node (CT) with a slow charge, rapid discharge characteristic.

During typical positive buck operation, the main switch MOSFET is enabled at the start of each oscillator cycle. The main switch stays enabled until the current through the switched inductor, sensed via the voltage across a series sense resistor (R_{SENSE}), is sufficient to trip the current comparator (IC1) and, in turn, reset the RS latch. When the RS latch resets, the main switch is disabled, and the synchronous switch MOSFET is enabled. Shoot-through prevention logic prohibits enabling of the synchronous switch until the main switch is fully disabled. If the current comparator threshold is not obtained throughout the entire oscillator charge period, the RS latch is bypassed and the main switch is disabled during the oscillator discharge time. This “minimum off time” assures adequate charging of the bootstrap supply, protects the main switch, and is typically about 1µs.

OPERATION (Refer to Functional Block Diagram)

The current comparator trip threshold is set on the V_C pin, which is the output of a transconductance amplifier, or error amplifier (EA). The error amplifier integrates the difference between a feedback voltage (on the V_{FB} pin) and an internal bandgap generated reference voltage of 1.25V, forming a signal that represents required load current. If the supplied current is insufficient for a given load, the output will droop, thus reducing the feedback voltage. The error amplifier forces current out of the V_C pin, increasing the current comparator threshold. Thus, the circuit will servo until the provided current is equal to the required load and the average output voltage is at the value programmed by the feedback resistors.

Average Current Limit

The output of the sense amplifier is monitored by a single pole integrator comprised of an external capacitor on the I_{AVG} pin and an internal impedance of approximately 50kΩ. If this averaged value signal exceeds a level corresponding to 120mV across the external sense resistor, the current comparator threshold is clamped and cannot continue to rise in response to the error amplifier. Thus, if average load current requirements exceed $120mV/R_{SENSE}$, the supply will current limit and the output voltage will fall out of regulation. The average current limit circuit monitors the sense amplifier output without slope compensation or ripple current contributions, therefore the average load current limit threshold is unaffected by duty cycle.

Undervoltage Lockout

The LT1339 employs an undervoltage lockout circuit (UVLO) that monitors the 12V supply rail. This circuit disables the output drive capability of the LT1339 if the 12V supply drops below about 9V. Unstable mode switching is prevented through 350mV of UVLO threshold hysteresis.

Adaptive Nonoverlapping Output Stage

The FET driver output stage implements adaptive nonoverlapping control. This circuitry maintains dead time independent of the type, size or operating conditions of the switch elements. The control circuit monitors the output gate drive signals, insuring that the switch gate (being disabled) is fully discharged before enabling the other switch driver.

Shutdown

The LT1339 can be put into low current shutdown mode by pulling the RUN/SHDN pin low, disabling all circuit functions. The shutdown threshold is a bandgap referred voltage of 1.25V typical. Use of a precision threshold on the shutdown circuit enables use of this pin for undervoltage protection of the V_{IN} supply and/or power supply sequencing.

Soft Start

The LT1339 incorporates a soft start function that operates by slowly increasing the internal current limit. This limit is controlled by clamping the V_C node to a low voltage that climbs with time as an external capacitor on the SS pin is charged with about 8μA. This forces a graceful climb of output current capability, and thus a graceful increase in output voltage until steady-state regulation is achieved. The soft start timing capacitor is clamped to ground during shutdown and during undervoltage lockout, yielding a graceful output recovery from either condition.

5V Internal Reference

Power for the oscillator timing elements and most other internal LT1339 circuits is derived from an internal 5V reference, accessible at the $5V_{REF}$ pin. This supply pin can be loaded with up to 10mA DC (20mA pulsed) for convenient biasing of local elements such as control logic, etc.

Slope Compensation

For duty cycles greater than 50%, slope compensation is required to prevent current mode duty cycle instability in the regulator control loop. The LT1339 employs internal slope compensation that is adequate for most applications. However, if additional slope compensation is desired, it is available through the SL/ADJ pin. Excessive slope compensation will cause reduction in maximum load current capability and therefore is not desirable.

APPLICATIONS INFORMATION

R_{SENSE} Selection for Output Current

R_{SENSE} generates a voltage that is proportional to the inductor current for use by the LT1339 current sense amplifier. The value of R_{SENSE} is based on the required load current. The average current limit function has a typical threshold of 120mV/R_{SENSE}, or:

$$R_{SENSE} = 120mV/I_{LIMIT}$$

Operation with V_{SENSE} common mode voltage below 4.5V may slightly degrade current limit accuracy. See Average Current Limit Threshold Tolerance vs Common Mode Voltage curve in the Typical Performance Characteristics section for more information.

Output Voltage Programming

Output voltage is programmed through a resistor feedback network to V_{FB} (Pin 9) on the LT1339. This pin is the inverting input of the error amplifier, which is internally referenced to 1.25V. The divider is ratioed to provide 1.25V at the V_{FB} pin when the output is at its desired value.

The output voltage is thus set following the relation:

$$V_{OUT} = 1.25(1 + R2/R1)$$

when an external resistor divider is connected to the output as shown in Figure 1.

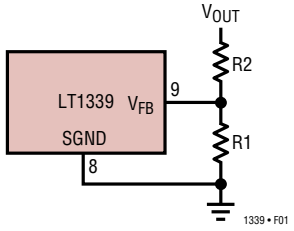


Figure 1. Programming LT1339 Output Voltage

If high value feedback resistors are used, the input bias current of the V_{FB} pin (1µA maximum) could cause a slight increase in output voltage. A Thevenin resistance at the V_{FB} pin of <5k is recommended.

Oscillator Components R_{CT} and C_{CT}

The LT1339 oscillator creates a modified sawtooth wave at its timing node (CT) with a slow charge, rapid discharge characteristic. The rapid discharge time corresponds to the minimum off-time of the PWM controller. This limits maximum duty cycle (DC_{MAX}) to:

$$DC_{MAX} = 1 - (t_{DISCH})(f_O)$$

This relation corresponds to the minimum value of the timing resistor (R_{CT}), which can be determined according to the following relation (R_{CT} vs DC_{MAX} graph appears in the Typical Performance Characteristics section):

$$R_{CT(MIN)} \approx [(0.8)(10^{-3})(1 - DC_{MAX})]^{-1}$$

Values for R_{CT} > 15k yield maximum duty cycles above 90%. Given a timing resistor value, the value of the timing capacitor (C_{CT}) can then be determined for desired operating frequency (f_O) using the relation:

$$C_{CT} \approx \frac{\left(1/f_O\right) - \left(100\right)\left(10^{-9}\right)}{\left(R_{CT}/1.85\right) + \frac{1.75}{\left(2.5\right)\left(10^{-3}\right) - \left(3.375/R_{CT}\right)}}$$

A plot of Operating Frequency vs R_{CT} and C_{CT} is shown in Figure 2. Typical 100kHz operational values are C_{CT} = 1000pF and R_{CT} = 16.9k.

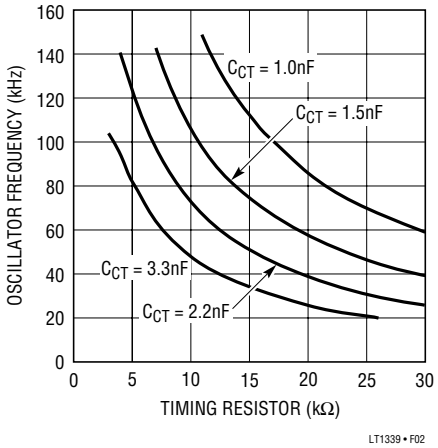


Figure 2. Oscillator Frequency vs R_{CT}, C_{CT}

Average Current Limit

The average current limit function is implemented using an external capacitor (C_{AVG}) connected from I_{AVG} to SGND that forms a single pole integrator with the 50kΩ output

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impedance of the I_{AVG} pin. The integrator corner frequency is typically set 1 to 2 orders of magnitude below the oscillator frequency and follows the relation:

$$f_{-3dB} = (3.2)(10^{-6})/C_{AVG}$$

The average current limit function can be disabled by shorting the I_{AVG} pin directly to SGND.

Soft Start Programming

The current control pin (V_C) limits sensed inductor current to zero at voltages less than a transistor V_{BE}, to full average current limit at $V_C = V_{BE} + 1.8V$. This generates a 1.8V full regulation range for average load current. An internal voltage clamp forces the V_C pin to a $V_{BE} – 100mV$ above the SS pin voltage. This 100mV "dead zone" assures 0% duty cycle operation at the start of the soft start cycle, or when the soft start pin is pulled to ground. Given the typical soft start current of 8µA and a soft start timing capacitor C_{SS}, the start-up delay time to full available average current will be:

$$t_{SS} = (1.5)(10^5)(C_{SS})$$

Boost Supply

The V_{BOOST} supply is bootstrapped via an external capacitor. This supply provides gate drive to the topside switch FET. The bootstrap capacitor is charged from $12V_{IN}$ through a diode when the switch node is pulled low.

The diode reverse breakdown voltage must be greater than $V_{IN} + 12V_{IN}$. The bootstrap capacitor should be at least 100 times greater than the total input capacitance of the topside FET. A capacitor in the range of 0.1µF to 1µF is generally adequate for most applications.

Shutdown Function—Input Undervoltage Detect and Threshold Hysteresis

The LT1339 RUN/SHDN pin uses a bandgap generated reference threshold of about 1.25V. This precision threshold allows use of the RUN/SHDN pin for both logic-level shutdown applications and analog monitoring applications such as power supply sequencing.

Because an LT1339 controlled converter is a power transfer device, a voltage that is lower than expected on the input supply could require currents that exceed the sourcing capabilities of that supply, causing the system to lock up in an undervoltage state. Input supply start-up protection can be achieved by enabling the RUN/SHDN pin using a resistor divider from the input supply to ground. Setting the divider output to 1.25V when that supply is almost fully enabled prevents the LT1339 regulator from drawing large currents until the input supply is able to provide the required power.

If additional hysteresis is desired for the enable function, an external feedback resistor can be used from the LT1339 regulator output. If connection to the regulator output is not desired, the $5V_{REF}$ internal supply pin can be used. Figure 3 shows a resistor connection on a 48V to 5V converter that yields a 40V V_{IN} start-up threshold for regulator enable and also provides about 10% input referred hysteresis.

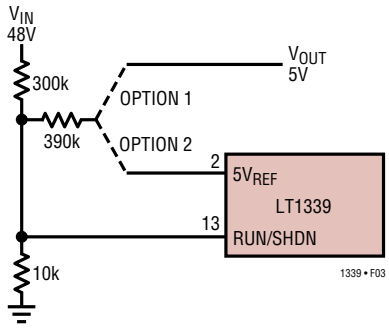

Figure 3. Input Supply Sequencing Programming

The shutdown function can be disabled by connecting the RUN/SHDN pin to the $12V_{IN}$ rail. This pin is internally clamped to 2.5V through a 20k series input resistance and will therefore draw about 0.5mA when tied directly to 12V. This additional current can be minimized by making the connection through an external resistor (100k is typically used).

Operation with Split Supplies and Supply Sequencing

N-channel power MOSFETs can parasitically turn themselves on due to leakage currents or capacitive coupling onto the MOSFET gate. In shutdown, this is prevented by active pull-down clamps on the TG and BG driver outputs of the LT1339. These clamps are active when $12V_{IN} > 0.7V$. The $12V_{IN}$ power supply for the LT1339 is usually derived from the converter input supply; however, these supplies can be independent. If these supplies are independent and

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the converter input supply is enabled with no voltage on the LT1339 $12V_{IN}$ pin, the LT1339 driver output clamps will not be activated. To prevent turn-on, an external current path must be used to bleed off charge on the switch MOSFET gates. High value bleed resistors (50k to 250k) should be connected between the TG and SW pins and between BG and PGND. This provides discharge paths for the switch MOSFET gates, preventing parasitic turn-on and damage to the MOSFETs.

Inductor Selection

The inductor for an LT1339 converter is selected based on output power, operating frequency and efficiency requirements. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (ΔI). For a buck converter, the minimum inductor value for a desired maximum operating ripple current can be determined using the following relation:

$$L_{MIN} = \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(\Delta I)(f_O)(V_{IN})}$$

where f_O = operating frequency. Given an inductor value (L), the peak inductor current is the sum of the average inductor current (I_{AVG})and half the inductor ripple current (ΔI), or:

$$I_{PK} = I_{AVG} + \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(2)(L)(f_O)(V_{IN})}$$

The inductor core type is determined by peak current and efficiency requirements. The inductor core must withstand peak current without saturating, and series winding resistance and core losses should be kept as small as is practical to maximize conversion efficiency.

The LT1339 peak current limit threshold is 40% greater than the average current limit threshold. Slope compensation effects reduce this margin as duty cycle increases. This margin must be maintained to prevent peak current limit from corrupting the programmed value for average current limit. Programming the peak ripple current to less than 15% of the desired average current limit value will assure porper operation of the average current limit feature through 90% duty cycle (see Slope Compensation section).

Oscillator Synchronization

The LT1339 oscillator generates a modified sawtooth waveform at the C_T pin between low and high thresholds of about 0.8V (vl) and 2.5V (vh) respectively. The oscillator can be synchronized by driving a TTL level pulse into the SYNC pin. This inputs to a one-shot circuit that reduces the oscillator high threshold to 2V for about 200ns. The SYNC input signal should have minimum high/low times of ≥1µs.

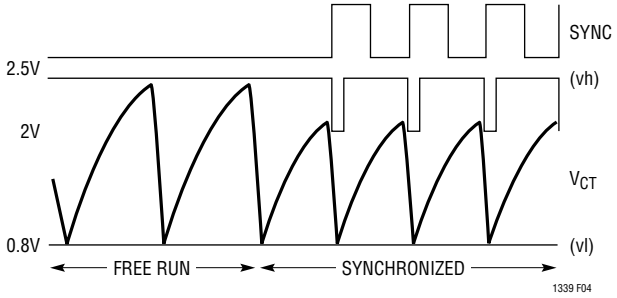

Figure 4. Free Run and Synchronized Oscillator Waveforms (at C_T Pin)

Slope Compensation

Current mode switching regulators that operate with a duty cycle greater than 50% and have continuous inductor current can exhibit duty cycle instability. While a regulator will not be damaged and may even continue to function acceptably during this type of subharmonic oscillation, an irritating high-pitched squeal is usually produced.

The criterion for current mode duty cycle instability is met when the increasing slope of the inductor ripple current is less than the decreasing slope, which is the case at duty cycles greater than 50%. This condition is illustrated in Figure 5a. The inductor ripple current starts at I_1, at the beginning of each oscillator switch cycle. Current increases at a rate S1 until the current reaches the control trip level I_2. The controller servo loop then disables the main switch (and enables the synchronous switch) and inductor current begins to decrease at a rate S2. If the current switch point (I_2) is perturbed slightly and increased by ΔI, the cycle time ends such that the minimum current point is increased by a factor of (1 + S2/S1) to start the next cycle. On each successive cycle, this error is multiplied by a factor of S2/S1. Therefore, if S2/S1 is ≥ 1, the system is unstable.

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Subharmonic oscillations can be eliminated by augmenting the increasing ripple current slope (S1) in the control loop. This is accomplished by adding an artificial ramp on the inductor current waveform internal to the IC (with a slope S_X) as shown in Figure 5b. If the sum of the slopes S1 + S_X is greater than S2, the condition for subharmonic oscillation no longer exists.

For a buck converter, the required additional current waveform slope, or "Slope Compensation," follows the relation:

$$S_X \geq \left(\frac{V_{IN}}{L}\right)(2DC-1)$$

For duty cycles less than 50% (DC < 0.5), S_X is negative and is not required. For duty cycles greater than 50%, S_X takes on values dependent on S1 and duty cycle. This leads to a minimum inductance requirement for a given V_{IN} and duty cycle of:

$$L_{MIN} = \left(\frac{V_{IN}}{S_X}\right)(2DC-1)$$

The LT1339 contains an internal S_X slope compensation ramp that has an equivalent current referred value of:

$$0.084\left(\frac{f_O}{R_{SENSE}}\right) \quad \text{Amp/s}$$

where f_O is oscillator frequency. This yields a minimum inductance requirement of:

$$L_{MIN} \geq \frac{(V_{IN})(R_{SENSE})(2DC-1)}{(0.084)(f_O)}$$

A down side of slope compensation is that, since the IC servo loop senses an increase in perceived inductor current, the internal current limit functions are affected such that the maximum current capability of a regulator is reduced by the same amount as the effective current referred slope compensation. The LT1339, however, uses a current limit scheme that is independent of slope compensation effects (average current limit). This provides operation at any duty cycle with no reduction in current sourcing capability, provided ripple current peak amplitude is less than 15% of the current limit value. For example, if the supply is set up to current limit at 10A, as long as the peak inductor current is less than 11.5A, duty cycles up to 90% can be achieved without compromising the average current limit value.

If an inductor smaller than the minimum required for internal slope compensation (calculated above as L_{MIN}) is desired, additional slope compensation is required. The LT1339 provides this capability through the SL/ADJ pin. This feature is implemented by referencing this pin via a resistor divider from the $5V_{REF}$ pin to ground. The additional slope compensation will be affected at the point in the oscillator waveform (at pin CT) corresponding to the voltage set by the resistor divider. Additional slope compensation can be calculated using the relation:

$$S_{XADD} = \frac{(2500)(f_O)}{(R_{EQ})(R_{SENSE})} \quad \text{Amp/s}$$

where R_{EQ} is the effective resistance of the resistor divider. Actual compensation will be somewhat greater due to internal curvature correction circuitry that imposes an exponential increase in the slope compensation waveform,

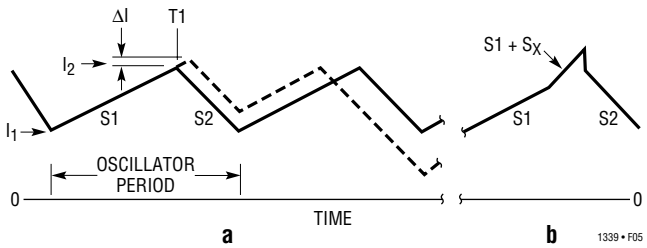

Figure 5. Inductor Current at DC > 50% and Slope Compensation Adjusted Signal

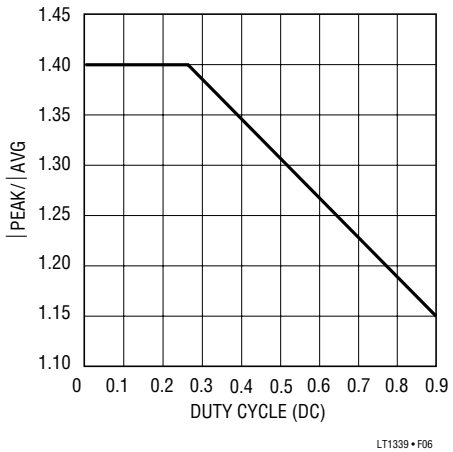

Figure 6. Maximum Ripple Current (Normalized) vs Duty Cycle for Average Current Limit

APPLICATIONS INFORMATION

further increasing the effective compensation slope up to 20% for a given setting.

Design Example:

V_{IN} = 20V
V_{OUT} = 15V (DC = 0.75)
R_{SENSE} = 0.01Ω
f_O = 100kHz
L = 5µH

The minimum inductor usable with no additional slope compensation is:

$$L_{MIN} \geq \frac{(20V)(0.01\Omega)(1.5-1)}{(0.084)(100000)} = 11.9\mu H$$

Since L = 5µH is less than L_{MIN}, additional slope compensation is necessary. The total slope compensation required is:

$$S_X \geq \left(\frac{20V}{5\mu H}\right)(1.5-1) = (2)(10^6) \quad \text{Amp/s}$$

Subtracting the internally generated slope compensation and solving for the required effective resistance at SL/ADJ yields:

$$R_{EQ} \leq \frac{(2500)(f_O)}{(2)(10^6)(R_{SENSE}) - (0.084)(f_O)} = 21.5k$$

Setting the resistor divider reference voltage at 2V assures that the additional compensation waveform will be enabled at 75% duty cycle. As shown in Figure 7a, using R_{SL1} = 45k and R_{SL2} = 30k sets the desired reference voltage and has a R_{EQ} of 18k, which meets both design requirements. Figure 7b shows the slope compensation effective waveforms both with and without the SL/ADJ external resistors.

Power MOSFET and Catch Diode Selection

External N-channel MOSFET switches are used with the LT1339. The positive gate-source drive voltage of the LT1339 for both switches is roughly equivalent to the $12V_{IN}$ supply voltage, so standard threshold MOSFETs can be used.

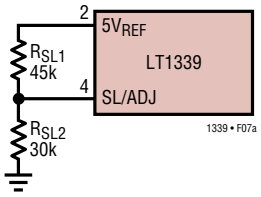

Figure 7a. External Slope Compensation Resistors

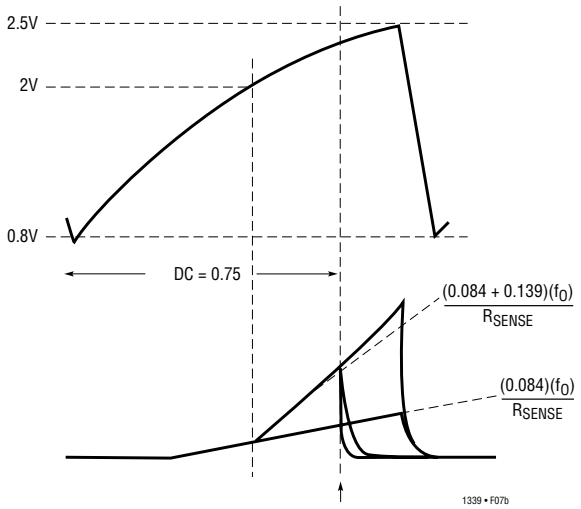

Figure 7b. Slope Compensation Waveforms

Selection criteria for the power MOSFETs include the "ON" resistance ($R_{DS(ON)}$), reverse transfer capacitance (C_{RSS}), maximum drain-source voltage (V_{DSS}) and maximum output current.

The power FETs selected must have a maximum operating V_{DSS} exceeding the maximum V_{IN}. V_{GS} voltage maximum must exceed the $12V_{IN}$ supply voltage.

Once voltage requirements have been determined, $R_{DS(ON)}$ can be selected based on allowable power dissipation and required output current.

In an LT1339 buck converter, the average inductor current is equal to the DC load current. The average currents through the main and synchronous switches are:

$I_{MAIN} = (I_{LOAD})(DC)$

$I_{SYNC} = (I_{LOAD})(1 - DC)$

The $R_{DS(ON)}$ required for a given conduction loss can be calculated using the relation:

$P_{LOSS} = (I_{SWITCH})^2(R_{DS(ON)})$

APPLICATIONS INFORMATION

In high voltage applications (V_{IN} > 20V), the topside switch is required to slew very large voltages. As V_{IN} increases, transition losses increase through a square relation, until it becomes the dominant power loss term in the main switch. This transition loss takes the form:

$$P_{TR} \approx (k)(V_{IN})^2(I_{MAX})(C_{RSS})(f_O)$$

where k is a constant inversely related to the gate drive current, approximated by k = 2 in LT1339 applications.

The maximum power loss terms for the switches are thus:

$$P_{MAIN} = (DC)(I_{MAX})^2(1 + \delta)(R_{DS(ON)}) + 2(V_{IN})^2(I_{MAX})(C_{RSS})(f_O)$$

$$P_{SYNC} = (1 - DC)(I_{MAX})^2(1 + \delta)(R_{DS(ON)})$$

The (1 + δ) term in the above relations is the temperature dependency of $R_{DS(ON)}$, typically given in the form of a normalized $R_{DS(ON)}$ vs Temperature curve in a MOSFET data sheet.

In some applications, parasitic FET capacitances couple the negative going switch node transient onto the bottom gate drive pin of the LT1339, causing a negative voltage in excess of the Absolute Maximum Rating to be imposed on that pin. Connection of a catch Schottky (rated to about 1A is typically sufficient) from this pin to ground will eliminate this effect.

C_{IN} and C_{OUT} Supply Decoupling Capacitor Selection

The large currents typical of LT1339 applications require special consideration for the converter input and output supply decoupling capacitors. Under normal steady state operation, the source current of the main switch MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is provided by the input bypass capacitor. To prevent large input voltage transients and avoid bypass capacitor heating, a low ESR input capacitor sized for the maximum RMS current must be used. This maximum capacitor RMS current follows the relation:

$$I_{RMS} \approx \frac{(I_{MAX})(V_{OUT}(V_{IN} - V_{OUT}))^{1/2}}{V_{IN}}$$

which peaks at a 50% duty cycle, when $I_{RMS} = I_{MAX}/2$. Capacitor ripple current ratings are often based on only 2000 hours (three months) lifetime; it is advisable to derate either the ESR or temperature rating of the capacitor for increased MTBF of the regulator.

The output capacitor in a buck converter generally has much less ripple current than the input capacitor. Peak-to-peak ripple current is equal to that in the inductor (ΔI_L), typically a fraction of the load current. C_{OUT} is selected to reduce output voltage ripple to a desirable value given an expected output ripple current. Output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\{ESR + [(4)(f_O) \bullet C_{OUT}]^{-1}\}$$

where f_O = operating frequency.

Efficiency Considerations and Heat Dissipation

High output power applications have inherent concerns regarding power dissipation in converter components. Although high efficiencies are achieved using the LT1339, the power dissipated in the converter climbs to relatively high values when the load draws large amounts of power. Even at 90% efficiency, an application that provides 500W to the load has conversion loss of 55W.

I^2R dissipation through the switches, sense resistor and inductor series resistance create substantial losses under high currents. Generally, the dominant I^2R loss is evident in the FET switches. Loss in each switch is proportional to the conduction time of that switch. For example, in a 48V to 5V converter the synchronous FET conducts load current for almost 90% of the cycle time and thus, requires greater consideration for dissipating I^2R power.

Gate charge/discharge current creates additional current drain on the 12V supply. If powered from a high voltage input through a linear regulator, the losses in that regulator device can become significant. A supply solution bootstrapped from the output would draw current from a lower voltage source and reduce this loss component.

Transition losses are significant in the topside switch FET when high V_{IN} voltages are used. Transition losses can be estimated as:

$$P_{TLOSS} \approx 2(V_{IN})^2(I_{MAX})(C_{RSS})(f_O)$$

Since the conduction time in the main switch of a 48V to 5V converter is small, the I^2R loss in the main switch FET

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is also small. However, since the FET gate must switch up past the 48V input voltage, transition loss can become a significant factor. In such a case, it is often prudent to take the increased I^2R loss of a smaller FET in order to reduce C_{RSS} and thus, the associated transition losses.

Gate Drive Buffers

The LT1339 is designed to drive relatively large capacitive loads. However, in certain applications, efficiency improvements can be realized by adding an external buffer stage to drive the gates of the FET switches. When the switch gates load the driver outputs such that rise/fall times exceed about 100ns, buffers can sometimes result in efficiency gains. Buffers also reduce the effect of back injection into the bottom side driver output due to coupling of switch node transitions through the switch FET C_{MILLER}.

Paying the Physicists

In high power synchronous buck configurations, certain physical characteristics of the external MOSFET switches can impact conversion efficiency. As the input voltage approaches about 30V, the bottom MOSFETs will begin to exhibit "phantom turn-on." This phenomenon is caused by coupling of the instantaneous voltage step on the bottom side switch drain through C_{MILLER} to the device gate, yielding internal localized gate-source voltages above the turn-on threshold of the FET. This generates a shoot-through blip that ultimately eats away at efficiency numbers. In Figure 8 a negative prebias circuit is added to the bottom side gate. The addition of this ~3V of negative offset to the bottom gate drive provides additional off-state voltage range to prevent phantom turn-on.

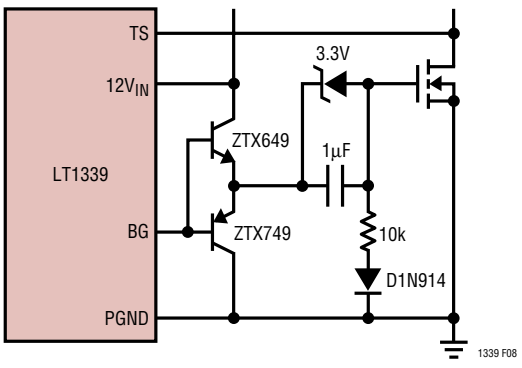


Figure 8. Bottom Side Driver Negative Prebias Circuit

This type of prebias circuit is used in the 48V to 5V, 50A converter pictured in the Typical Applications section.

As currents increase beyond the 10A to 15A range, the bottom side FET body diode experiences hard turn-on during switch dead time due to local current loop inductance preventing the timely transfer of charge to the Schottky catch diode. The charge current required to commutate this body diode creates a high dV/dt Schottky avalanche when the diode charge is finally exhausted (due to an effective inductor current discontinuity at the moment the body diode no longer requires charge). This generates an increased turn-on power burst in the topside switch, causing additional conversion efficiency loss. This effect of this parasitic inductance can be reduced by using *FETKEY*™ MOSFETs, which have parallel catch Schottky diodes internal to their packages. *FETKEY* MOSFETs are not available for high voltages, so as input voltage continues to increase, they can no longer be used. Because this necessitates the use of discrete FETs and Schottkys, interdigitation of a number of smaller devices is required to minimize parasitic inductances. This technique is also used in the 48V to 5V, 50A converter shown in the Typical Applications section.

Optimizing Transient Response—Compensation Component Values

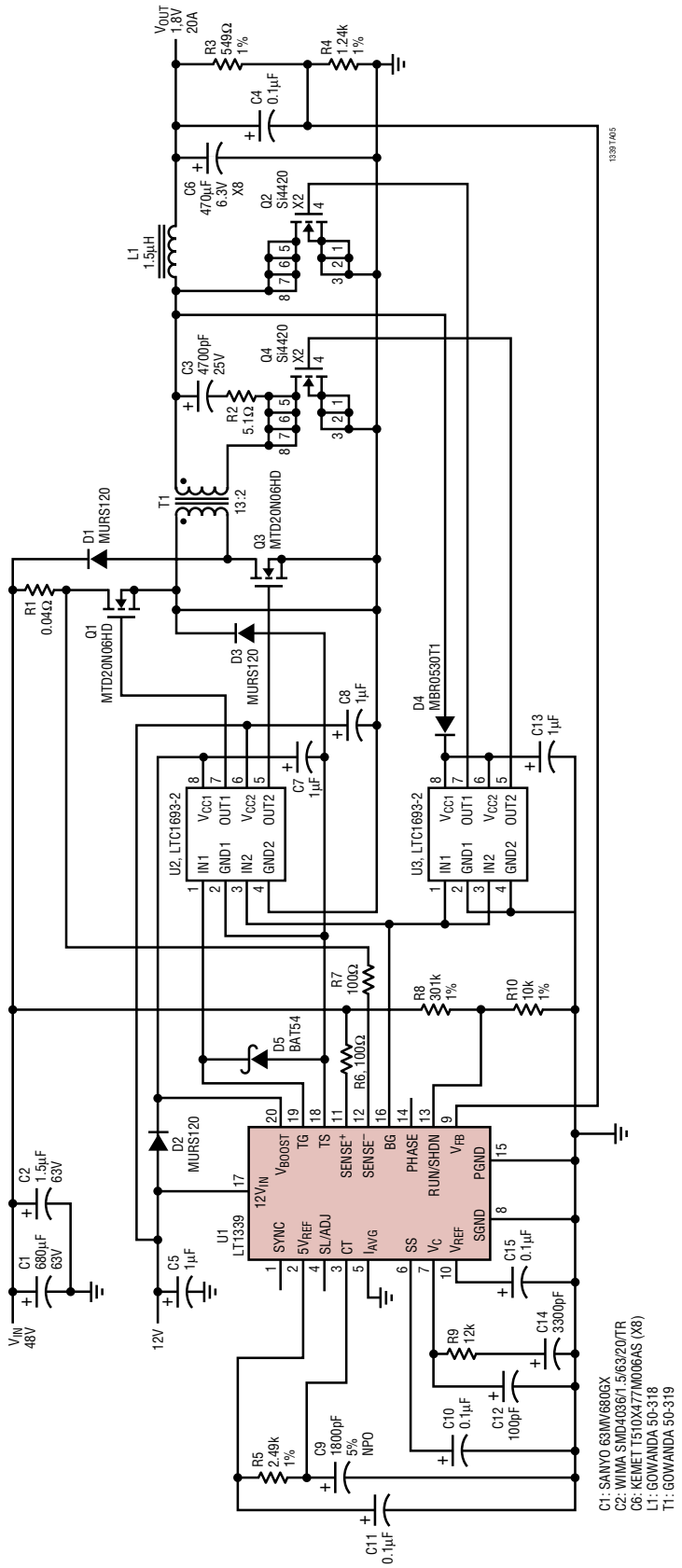
The dominant compensation point for an LT1339 converter is the V_C pin (Pin 7), or error amplifier output. This pin is connected to a series RC network, R_{VC} and C_{VC}. The infinite permutations of input/output filtering, capacitor ESR, input voltage, load current, etc. make for an empirical method of optimizing loop response for a specific set of conditions.

Loop response can be observed by injecting a step change in load current. This can be achieved by using a switchable load. With the load switching, the transient response of the output voltage can be observed with an oscilloscope. Iterating through RC combinations will yield optimized response. Refer to LTC Application Note 19 in *1990 Linear Applications Handbook, Volume 1* for more information.

FETKEY is a trademark of International Rectifier Corporation.

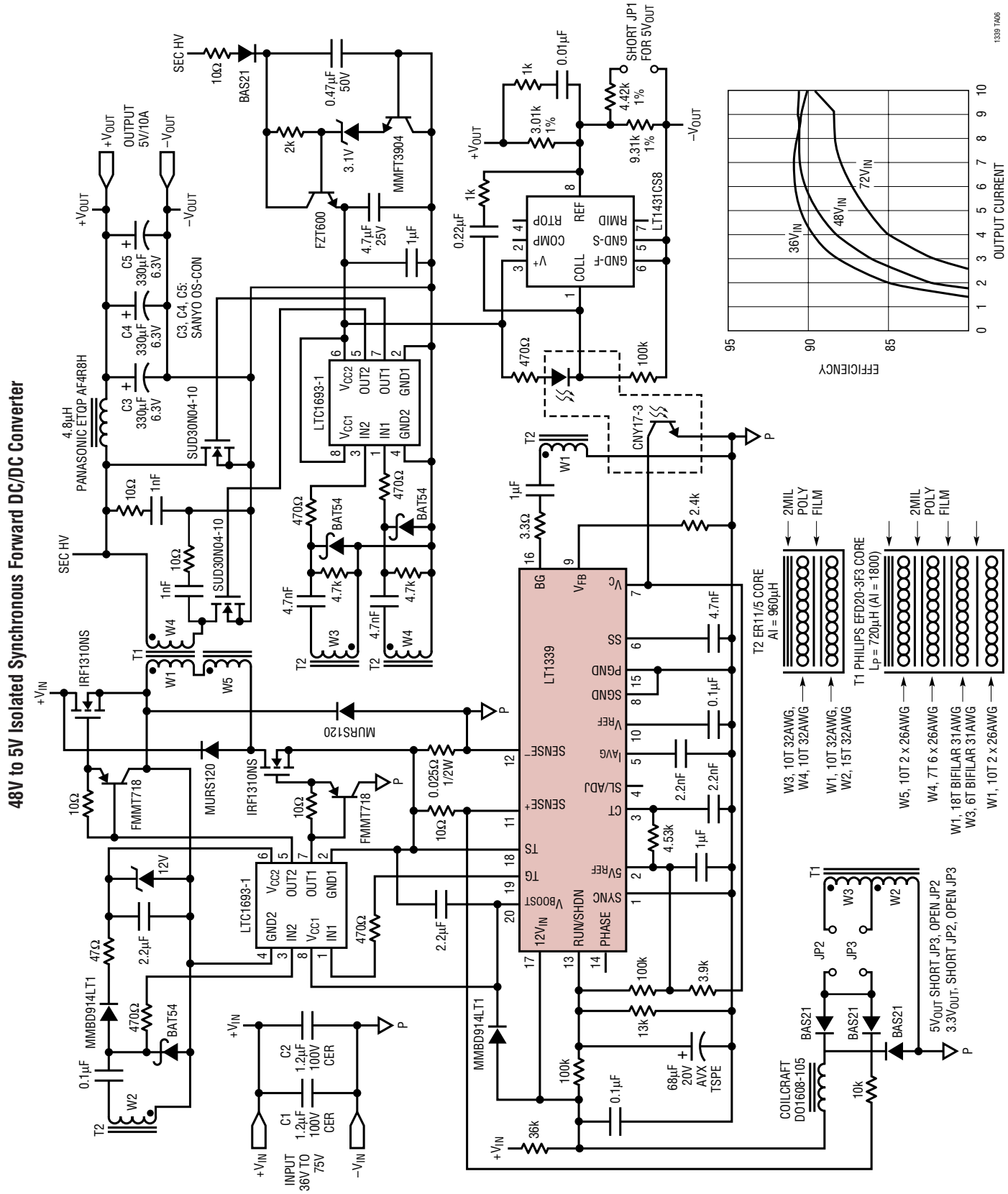
TYPICAL APPLICATIONS

48V to 1.8V 2-Transistor Synchronous Forward Converter



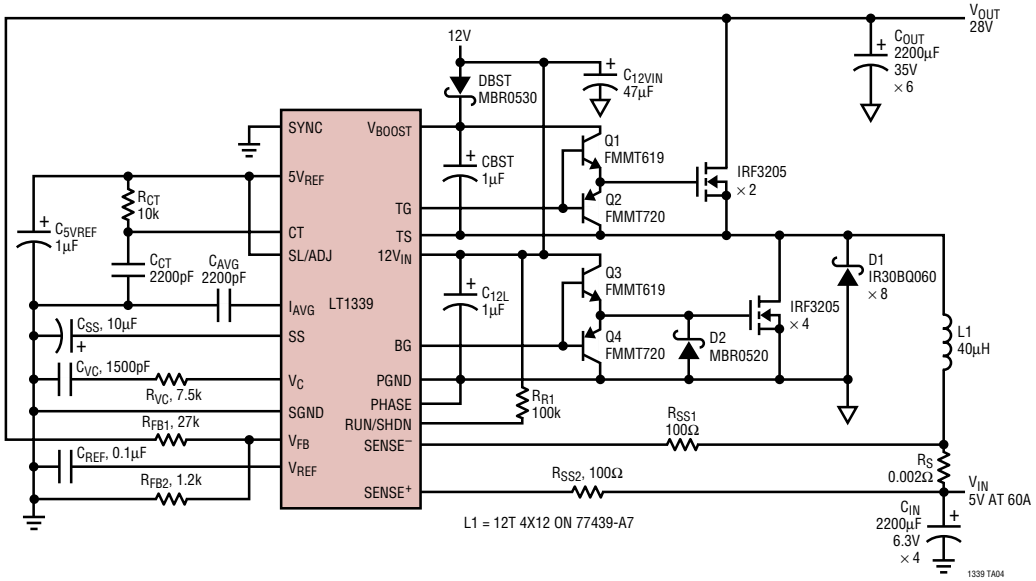
TYPICAL APPLICATIONS

48V to 5V Isolated Synchronous Forward DC/DC Converter



TYPICAL APPLICATIONS

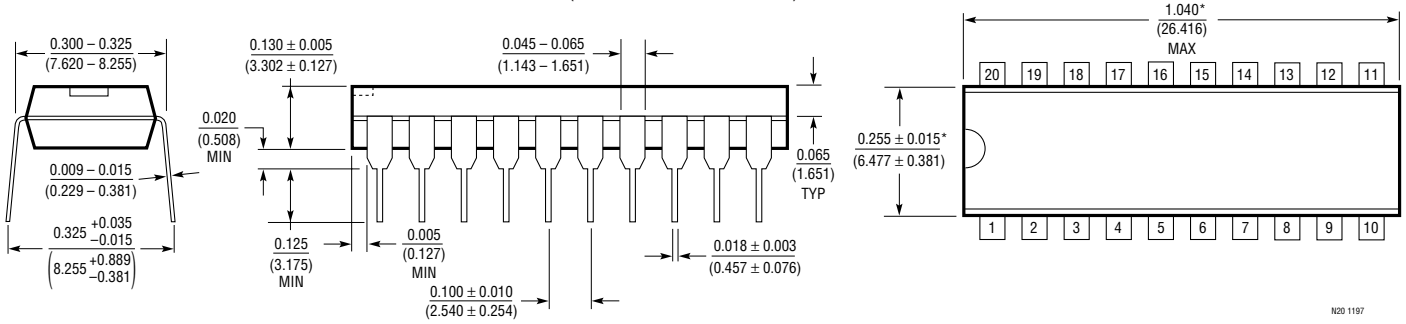
5V to 28V DC/DC Synchronous Boost Converter Limits Input Current at 60A (DC)



PACKAGE DESCRIPTION

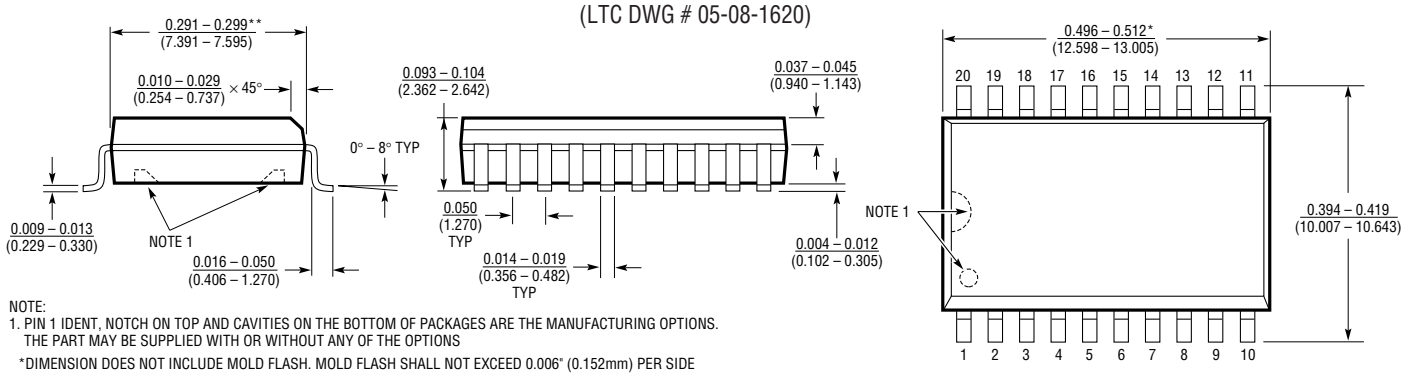
Dimensions in inches (millimeters) unless otherwise noted.

N Package
20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



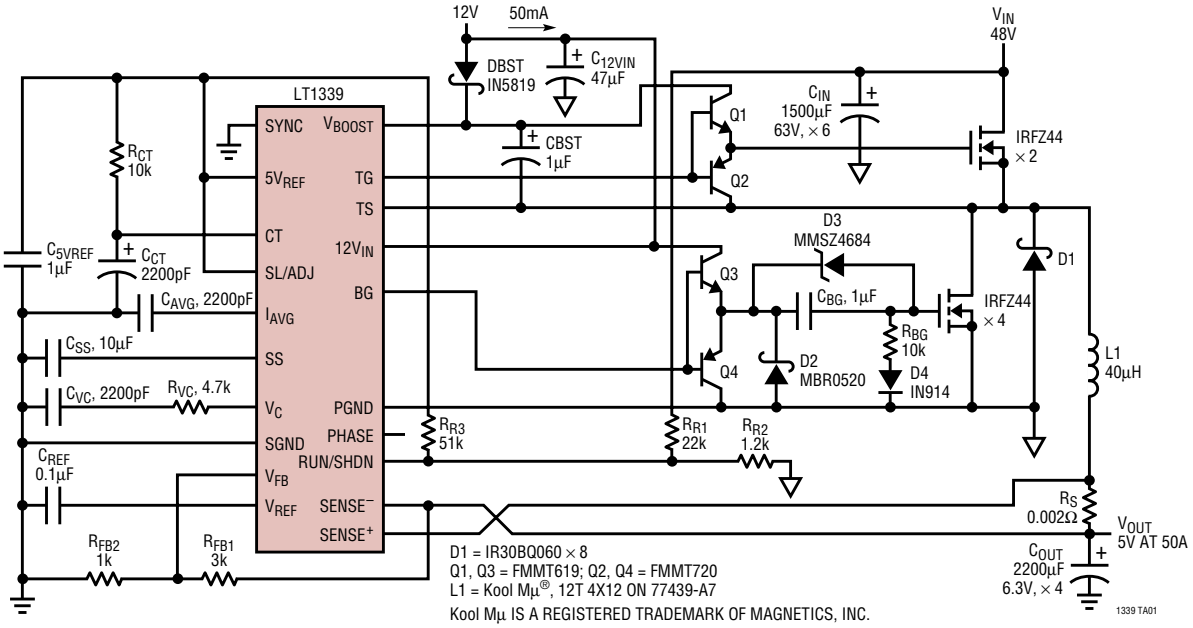
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

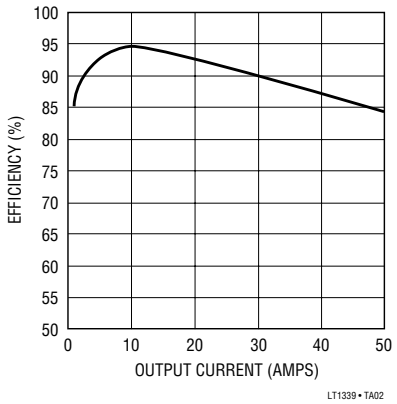
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

48V to 5V 50A DC/DC Converter with Input Supply Start-Up Protection



48V to 5V Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1158	Half-Bridge N-Channel MOSFET Driver	Current Limit Protection, 100% of Duty Cycle
LT1160	Half-Bridge N-Channel MOSFET Driver	Up to 60V Input Supply, No Shoot-Through
LT1162	Dual Half-Bridge N-Channel MOSFET Driver	V_{IN} to 60V, Good for Full-Bridge Applications
LT1336	Half-Bridge N-Channel MOSFET Driver	Smooth Operation at High Duty Cycle (95% to 100%)
LTC®1530	High Power Step-Down Switching Regulator Controller	Excellent for 5V to 3.xV Up to 50A
LTC1435A	High Efficiency, Low Noise Current Mode Step-Down DC/DC Converter	Drives Synchronous N-Channel MOSFETs
LTC1438	Dual High Efficiency, Low Noise Synchronous Step-Down Controller	Tight 1% Reference
LT1680	High Power DC/DC Current Mode Step-Up Controller	High Side Current Sense, Up to 60V Input

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408)434-0507 • www.linear-tech.com

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