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1 Block diagram and pin description

Figure 1. Block diagram

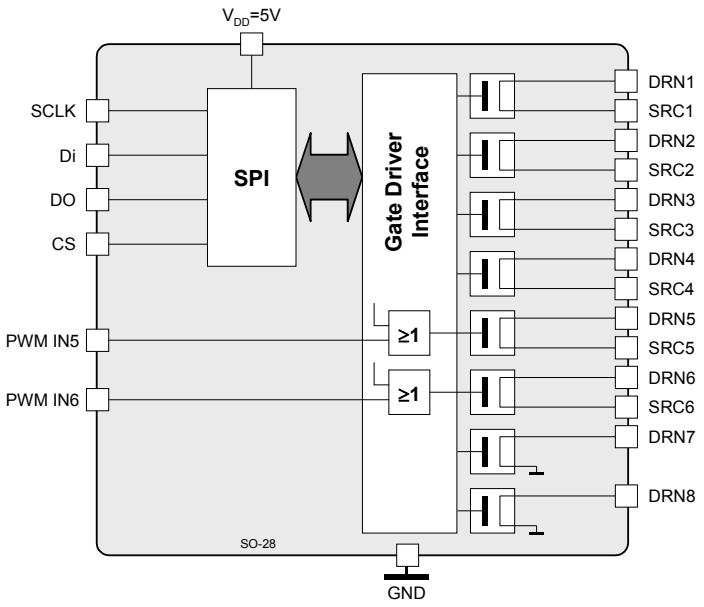


Figure 2. Pin connection (top view)

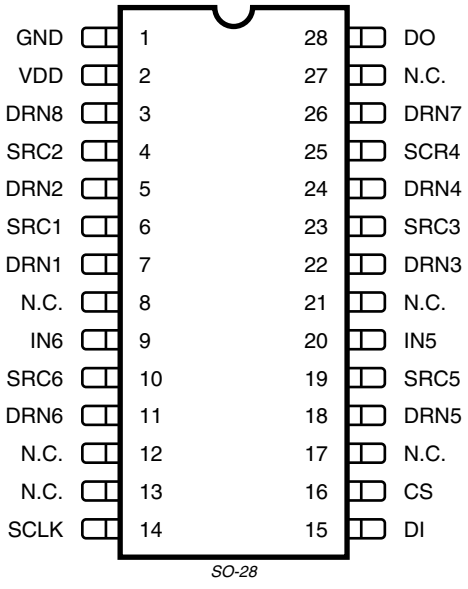


Table 2. Pin description

N°	Pin	Description
1	GND	Analog ground
2	VDD	5V supply input
3	DRN8	Drain of low side driver #8
4	SRC2	Source of configurable driver #2
5	DRN2	Drain of configurable driver #2
6	SRC1	Source of configurable driver #1
7	DRN1	Drain of configurable driver #1
8	NC	Not connected
9	IN6	PWM input for driver #6
10	SRC6	Source of configurable driver #6
11	DRN6	Drain of configurable driver #6
12	NC	Not connected
13	NC	Not connected
14	SCLK	SPI serial clock input
15	DI	SPI data in
16	CS	SPI chip select (active high)
17	NC	Not connected
18	DRN5	Drain of configurable driver #5
19	SRC5	Source of configurable driver #5
20	IN5	PWM input for driver #5
21	NC	Not connected
22	DRN3	Drain of configurable driver #3
23	SRC3	Source of configurable driver #3
24	DRN4	Drain of configurable driver #4
25	SRC4	Source of configurable driver #4
26	DRN7	Drain of low side driver #7
27	NC	Not connected
28	DO	SPI data out

2 Electrical specifications

2.1 Absolute maximum ratings

Warning: **For voltages and currents applied externally to the device. This part may be irreparably damaged if taken outside the specified absolute maximum rating range**

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 7.0	V
Pin voltages			
V_{CS}, V_{DI}, V_{DO}, V_{SCLK}	Data lines voltages	-0.3 to 7.0	V
V_{IN5}, V_{IN6}	Input voltages	-0.3 to 7.0	V
$V_{SRC1} - V_{SRC8}$	Output DC voltages	-13.5 to 40	V
$V_{DRN1} - V_{DRN6}$	Output DC voltages	-13.5 to 60 (1)	V
$V_{SRC1} - V_{SRC8}$	Output transient voltages	-20 to 40	V
$V_{DRN1} - V_{DRN6}$	Output transient voltages	-20 to 60	V
$E_{out\ 1-8}$	Max. dissipation energy (@ 300mA)	60	mJ

1. Internally limited.

2.2 Operation conditions

Warning: **This part may not operate if taken outside the maximum ratings. Once the condition is returned to within the specified maximum rating or the power is re-cycled, the part will recover with no damage or degradation.**

Table 4. Operation conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.75 to 5.25	V
V_{Batt}	Battery supply voltage	9 to 18	V
I_{out}	Output current (channel 1-8)	350	mA
T_j	Junction temperature	-40 to 150	°C

2.3 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
T_{st}	Storage temperature	-65 to 150	°C
$R_{th(j-a)}$	Thermal resistance junction to ambient	max. 70	°C/W
$R_{th(j-a)}$	Thermal resistance junction to ambient(1)	max. 50	°C/W

1. With 6cm^2 on board heatsink area.

2.4 Electrical characteristcs

2.4.1 DC characteristics

Table 6. Electrical characteristcs

(T_j = -40°C to 150°C, V_{DD} = 4.75 V_{dc} to 5.25 V_{dc}, V_{Batt}=9 V to 18 V, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IN5,6(ih)}$ $V_{IN5,6(il)}$	IN5, 6 input voltage		 0.8		2.0	V V
$I_{IN5,6(il)}$ $I_{IN5,6(ih)}$	IN5, 6 input current	$V_{IN5,6}$ = 0V_{dc} $V_{IN5,6}$ = V_{DD}	 30		|10| 100	µA µA
$V_{CS(ih)}$ $V_{CS(il)}$	CS input voltage		 0.8		2.0	V V
$I_{CS(il)}$ $I_{CS(ih)}$	CS input current	V_{CS} = 0V_{dc} V_{CS} = V_{DD}	 30		|10| 100	µA µA
$V_{SCLK(ih)}$ $V_{SCLK(il)}$	SCLK input voltage		 0.8		2.0	V V
$I_{SCLK(il)}$ $I_{SCLK(ih)}$	SCLK input current	V_{SCLK} = 0V_{dc} V_{SCLK} = V_{DD}			|10| |10|	µA µA
$V_{DI(ih)}$ $V_{DI(il)}$	DI input voltage		 0.8		2.0	V V
$I_{DI((il)}$ $I_{DI((ih)}$	DI input current	V_{DI} = 0V_{dc} V_{DI} = V_{DD}			|10| |10|	µA µA
I_{VDD}	V_{DD} current	All outputs ON		4.5	6	mA
I_{VDD}	V_{DD} current	All outputs OFF	0.5	2.0	5.0	mA
$V_{DO(ol)}$ $V_{DO(oh)}$	DO output voltage	I_{DO} = 1.6 mA I_{DO} = -200 µA	 V_{DD}-0.8		0.4	V V
$I_{DO(zol)}$ $I_{DO(zoh)}$	DO tri-state current	V_{DO} = 0V_{dc} V_{DO} = V_{DD}			|10| |10|	µA µA

Table 6. Electrical characteristcs (continued)

(T_j = -40°C to 150°C, V_{DD} = 4.75 V_{dc} to 5.25 V_{dc}, V_{Batt}=9 V to 18 V, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DRN1-8(lk)}$	DRN1-8 leakage current (low side)	V_{DD}=0.5V_{dc}, V_{SRC1-6}=0V_{dc}, V_{DRN1-8}=18 V_{dc} V_{DD}=0.5V_{dc}, V_{SRC1-6}=0V_{dc}, V_{DRN}=35 V		0.1 1.5	5 10	µA µA
$I_{SRC1-6(lk)}$	SRC1-6 leakage current (high side)	V_{DD}=0.5V_{dc}, V_{SRC1-6}=0V_{dc}, V_{DRN1-8}=18 V_{dc} V_{DD}=0.5V_{dc}, V_{SRC1-6}=0V_{dc}, V_{DRN}=35 V	-5 -10	-0.1 -1.5		µA µA
$I_{DRN1-8(Sink)}$	DRN1-8 current sink (low side)	V_{SRC1-6}=0V_{dc}, DI=00h, V_{DRN1-8} = 18 V_{dc} V_{SRC1-6}=0V_{dc}, DI=00h, V_{DRN}=35 V	50 50	 60	80 100	µA µA
$I_{SRC1-6(Sour)}$	SRC1-6 current source (high side)	V_{SRC1-6}=0V_{dc}, DI=00h, V_{DRN1-8} =18 V_{dc} V_{SRC1-6}=0V_{dc}, DI=00h, V_{DRN}=35 V	-80 -100	-50 -60	-30 -30	µA µA
$I_{DRN1-8(Limit)}$	DRN1-8 current limit (low side)	V_{SRC1-6}=0V_{dc}, DI=FFh, V_{DRN1-8} = 4-16 V_{dc}	0.8	1.3	1.8	A
$I_{SRC1-6(Limit)}$	SRC1-6 current limit (high side)	V_{SRC1-6}=0-12 V_{dc}, DI=FFh, V_{DRN1-8} = V_{Batt}	-0.8	1.3	-1.8	A
$V_{DRN1-8(Cl+)}$	DRN1-8 clamp voltage (low side)	V_{SRC1-6}=0V_{dc}, DI=00h, I_{DRN1-8}=10 mA	35	45	55	V
$V_{SRC1-6(Cl+)bat}$	SRC1-6 clamp voltage (high side)	V_{DRN1-8}=25 V DI=00h, I_{DRN1-8}=10 mA		V_{Batt}–45		V
$V_{SRC1-6GND}$		V_{DRN} = 10 V; I_{SRC} = -10 mA	-36	-31	-27	V
$V_{DRN1-8(Fault)}$	DRN1-8 fault voltage (low side)	V_{SRC1-6}=0 V_{dc}, DI=00h	0.9V_{DD}		1.1V_{DD}	V
$V_{SRC1-6(Fault)}$	SRC1-6 fault voltage (high side)	V_{DRN1-8}=V_{Batt}, DI=00h	0.55V_{DD}		0.65V_{DD}	V
$R_{DSONDRN1-8}$	On-resistance (DRN1-8)	T_j=110 °C T_j=25 °C T_j=-40 °C		1.5 1.0	2.0 1.5 1.3	W W W
T_{jTS}	Thermal shutdown junction temperature(1)		155		185	°C
T_{jTSH}	Thermal shutdown threshold hysteresis*		5		15	K
POR_{wih}	Power on reset threshold on		3.40		4.50	V
POR_{whyst}	Power on reset hysteresis		0.4		0.8	V

1. Guaranteed by design, not tested

2.4.2 AC characteristics

Table 7. AC characteristics

(T_j = - 40 °C to 150 °C, V_{DD} = 4.75 V to 5.25 V_{dc}, V_{Batt} = 9 V to 18 V, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Slew rate (low side)	See *Figure 4* and *5*				
$t_{DRN1-8slewon}$	Turn on		10	25	100	µs
$t_{DRN1-8slewoff}$	Turn off		10	25	100	µs
	Delay time (low side)	See *Figure 4* and *5*				
$t_{DRN1-8delon}$	Turn on		2	10	20	µs
$t_{DRN1-8deloff}$	Turn off		10		100	µs
$t_{DRN1-8deloffon}$	Delta	$t_{DRN1-8deloff}$ - $t_{DRN1-8delon}$	20	50	60	µs
	Slew rate (high side)	See *Figure 4* and *5*				
$t_{SRC1-6slewon}$	Turn on		10	50	100	µs
$t_{SRC1-6slewoff}$	Turn off		10	25	100	µs
	Delay time (high side)	See *Figure 4* and *5*				
$t_{SRC1-6delon}$	Turn on		2		20	µs
$t_{SRC1-6deloff}$	Turn Off		10	50	100	µs
$t_{SRC1-6deloffon}$	Delta	$t_{SRC1-6deloff} - t_{SRC1-6delon}$	20		60	µs
C_{DI}	Input Capacitance*				20	pF
C_{SCLK}					20	pF
	Output data (DO)					
t_{DOrise}	Rise time	50 pF from DO to GND, see Fig. *6*			30	ns
t_{DOfall}	Fall time	50 pF from DO to GND, see Fig. *6*			30	ns
t_{DOacc}	Access time	50 pF from DO to GND, see Fig. *7*			70	ns
t_{DOset}	Set up time	50 pF from DO to GND, see Fig. *7*	20			ns
t_{DOhold}	Hold time	50 pF from DO to GND, see Fig. *7*	10			ns
t_{DOdis}	Disable time	No capacitor on DO, see *Figure 3*			140	ns
$t_{FltDlyInt}$	Fault delay time (Internal)	Duration of open/short fault until Fault Bit is ”Set”	100		300	µs
$t_{thFltDlyInt}$	Thermal fault delay time (Internal)	Duration of thermal fault until Fault Bit is ”Set”	40		50	µs

Figure 3. DO loading for disable time measurement

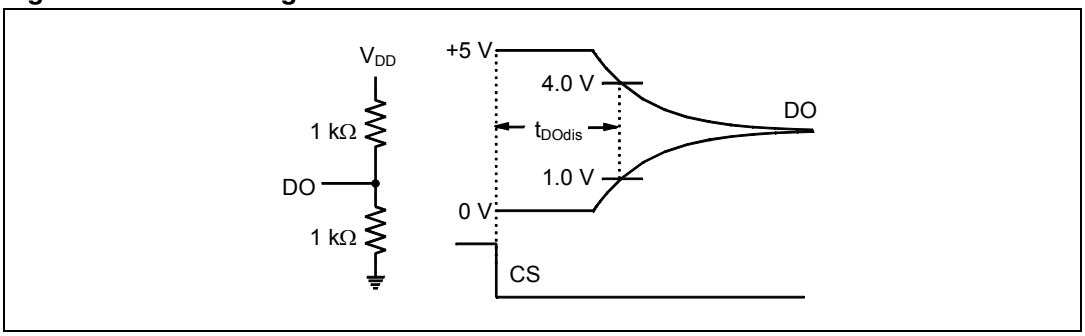


Figure 4. Output loading for slew rate measurement

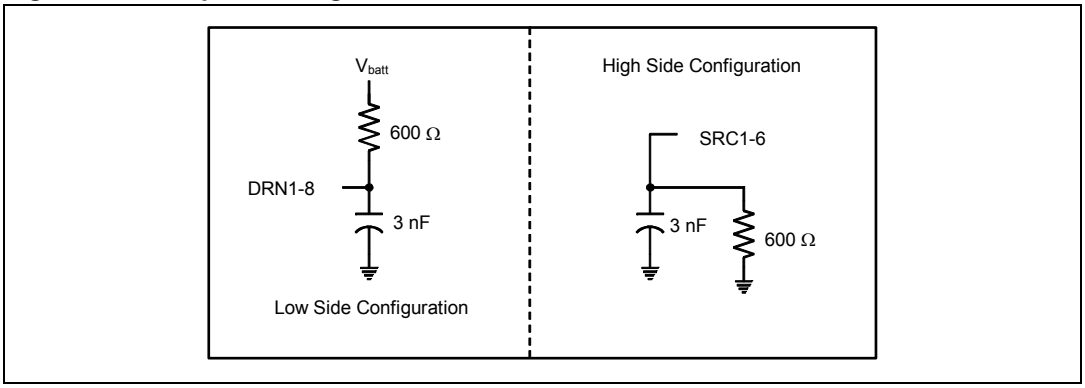
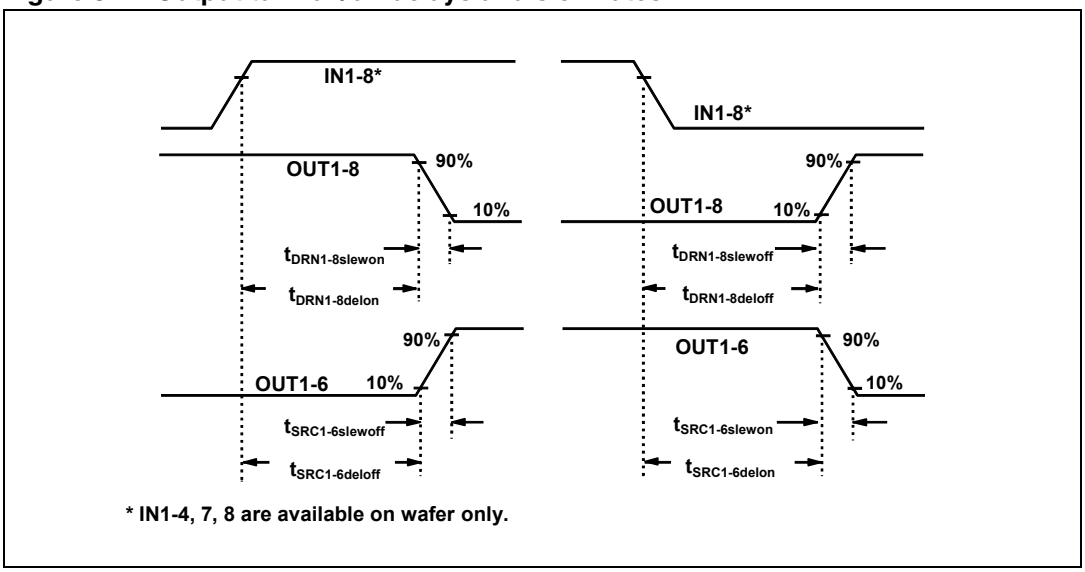


Figure 5. Output turn on/off delays and slew rates



*** IN1-4, 7, 8 are available on wafer only.**

Figure 6. SPI input/output slew ratest

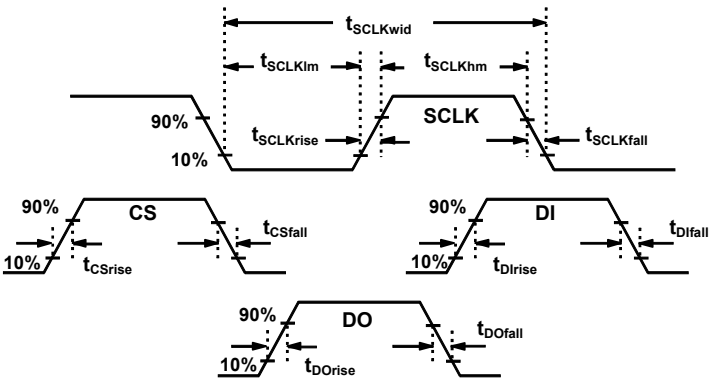
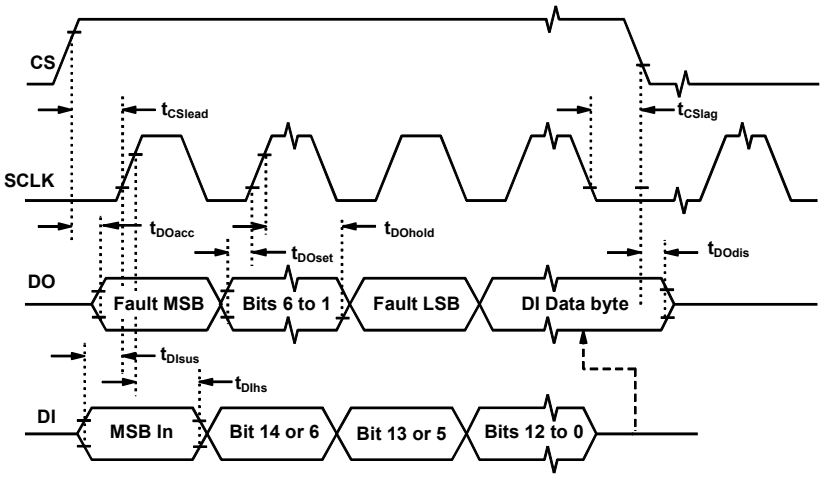


Figure 7. SPI timing diagram



3 Functional description

3.1 General features

The L9848 IC is a monolithic integrated circuit, which provides high flexibility for driving medium loads. 8 outputs, whereof 6 (Output1-6) can be used as either internal low or high side drives in any combination and 2 are dedicated low side outputs (Output7-8). The use of this device reduces the I/O port requirements of the microprocessor by having serially controlled outputs via a SPI interface. In addition, Output5-6 are capable of being PWMed via an external pin (Input5-6). The 8bit SPI input is used to command the 8 output drivers either ON or OFF and additional to indicate latched fault conditions that may have occurred.

Multiple L9848s may be daisy-chained with one additional microprocessor I/O port (CSn) for each device. The implemented self-configuration allows the user to connect a high or low side load to any of these outputs and the L9848 will drive them correctly as well as provide proper fault mode operation with no other needed inputs. This device switch variable load currents within the operation temperature range. The outputs are MOSFET drivers to minimize Vdd current requirements. There's no V_{Batt} input pin however V_{Batt} is connected to the drains of high side outputs.

The L9848 meets all required specifications when the supply voltage applied to the drain(s) of the outputs is within the operating range. For supply voltages applied to the drain(s) down to 6.8V the part is functional however, it does not meet all parametric limits, i.e. output on-state voltages.

3.2 Outputs - Common characteristics

The 6 self-configuring outputs (Outputs1-6) are able to drive either incandescent lamps, inductive loads (non-PWMed), or resistive loads biased to VBatt. These outputs are enabled and disabled via the SPI bus. Each of these outputs is short circuit current limited and has an over-temperature protection as described under "Functional Description - Thermal Shutdown".

When a high side configured output is commanded OFF after having been commanded ON, the source voltage will go to the lesser negative of (VBatt-45V). This is due to the design of the circuitry and the transconductance of the MOSFET.

When a low side configured output is commanded OFF after having been commanded ON, the output voltage will rise to the internal zener clamp voltage (40 Vdc minimum) due to the flyback of the inductive load.

3.2.1 Output 1-4

These four outputs can be used as either high or low side drives. Integrated current source pull-ups and pull-downs are employed to correctly latch "open load" fault data. Both of these current sources are needed to detect an open load state since these outputs self configure as either high or low side drives.

Drain connections of output1-4 (DRN1-4)
These pins are connected to the drains of the n-channel MOSFET transistors.

Source connections of output1-4 (SRC1-4)
These pins are connected to the sources of the n-channel MOSFET transistors.

3.2.2 Output 5-6

These two self-configuring outputs can be used to drive either high or low side loads. In addition to be controlled by the SPI BUS these outputs can also be enabled and disabled via IN5 and IN6 inputs. IN5 and IN6 inputs are logically ORed with the SPI commands to allow either the IN5-6 inputs or the SPI commands to activate these outputs. The use of IN5-6 for PWM control on these outputs should only be done with non-inductive loads. Integrated current source pull-ups and pull-downs are employed to correctly latch "open load" fault data. Both of these current sources are needed to detect an open since these outputs self configure as either high or low side drives.

Drain connections of Output5-6 (DRN5-6)
These pins are connected to the drains of the n-channel MOSFET transistors.

Source connections of Output5-6 (SRC5-6)
These pins are connected to the sources of the n-channel MOSFET transistors.

3.2.3 Output7-8

These two outputs (DRN7-8) are dedicated low side drives. Integrated current source pull down are required to correctly latch "open load" fault data.

3.3 Main power input (VDD)

The VDD input is the primary power source of the L9848. This supply is used as the power source for all of its logic circuitry and other miscellaneous functions. Notice that if the L9848 is interfaced to a processor operating with a lower voltage (e.g. 3.0 VDC), the microprocessor inputs connected to the L9848 will swing from 0 to 5.0 VDC.

3.4 Discrete inputs (IN5-6)

These inputs allow Output5-6 to be enabled via this external pin without the use of the SPI. A logic "1" on these inputs enables the corresponding output no matter what the status of the SPI command register. A logic "0" on these inputs disables the corresponding output if the SPI command register is not commanding this output on. These pins can be left "open" if the outputs are controlled only via the SPI (internally pulled down). These inputs are ideally suited for non-inductive loads that are pulse width modulated (PWMed). This allows PWM control without the use of the SPI. The TTL level compatible input voltages allow proper operation with microprocessors that are using 5.0V or 3.0V for their Vdd supply.

3.5 Serial peripheral interface (SPI)

A standard serial peripheral interface, consisting of Serial Clock (SCLK), Data Out (DO), Data In (DI), and Chip Select (CS) is implemented to allow access to the internal registers of the L9848. All outputs are controlled via the SPI.The input pins CS, SCLK, and DI have TTL level compatible input voltages allowing proper operation from microprocessors that are using 5.0V or 3.0V for their VDD supply. The design of the L9848 allows a "daisy-chaining" of multiple L9848's to further reduce the need for controller pins.

3.5.1 Serial data output (DO)

This output pin is in a tri-state condition when CS is a logic "0" (LOW). When CS is a logic "1" (HIGH), this pin always transmits 8bits of data from the fault register to the digital controller. After the first 8bits data are transmitted the DO output then sequentially transmits the digital data that was just received (8 SCLK cycles earlier) on the DI pin. The DO output continues to transmit the 8 SCLK delayed bit data from the DI input until CS eventually transitions from a logic "1" to a logic "0". DO data changes state 10 ns or later, after the falling edge of SCLK. By definition, the MSB (Table 3) is the first bit of the byte transmitted on DO and the LSB is the last bit of the byte transmitted on DO, once CS transitions from a logic "0" to a logic "1".

3.5.2 Serial data input (DI)

This input takes data from the digital controller while CS is HIGH. The L9848 accepts an 8bit data stream to command the outputs ON or OFF. By definition, the MSB (Table 1) is the first bit of each byte received on DI and the LSB is the last bit of each byte received on DI, once CS transitions from a logic "0" to a logic "1".

3.5.3 Chip select (CS)

This is the chip select input pin. On the rising edge of CS, the DO pin switches from tri-state to active-out mode. While CS is high, register data is shifted in and shifted out by the DI and DO pin, respectively, on each subsequent SCLK. On the falling edge of CS, the DO pin switches back to tri-state mode and the fault register will be "Cleared" if a valid DI byte was received.

A valid DI byte is defined as such:

- 1st A multiple of 8 bits was received
- 2nd SCLK was low when CS went low
- 3rd Current SPI cycle started when SCLK was low

The fault data is not cleared unless all of the 3 previous conditions have been met. A SCLK transition must be seen before CS is interpreted as active. To allow sufficient time to reload the fault registers, the CS pin must remain low for a minimum of 1µs prior to going high again, before it starts shifting the fault data bits out on the DO pin. CS has an integrated glitch filter for spurious pulses of 50ns or shorter (i.e. no fault data and Outputs1-8 enable status will be altered). For open circuit condition the CS is internally pulled down to GND.

3.5.4 Serial clock (SCLK)

This is the clock signal input for synchronization of serial data transfer. DI data is shifted into the DI input on the rising edge of SCLK and DO data changes on the falling edge of SCLK.

3.6 SPI DI input command register

An input byte (8 bits) is routed to the Command Register. The content of this Command Register is given in *Table 8* and *Table 9*. Additional DI data will continue to be wrapped around to the DO pin. If CS will go low before a complete reception of the current byte, this just transmitted byte will be ignored

Table 8. Bit command register definition

MSB							LSB
OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
D07	D06	D05	D04	D03	D02	D01	D00

Table 9. Command register logic definition

Bit	State	Status
D00-D07	0	OUTPUT1-8 are commanded OFF
D00-D07	1	OUTPUT1-8 are commanded ON

3.7 Fault operation

The fault diagnostic capability consists of one internal 8bit shift register. Open or shorted load detection is provided by comparing the source or drain voltage with the VDD voltage. When an output connected as either a low side device or a high side device is commanded OFF, an open load can be detected. When an output connected as either a low side device or a high side device is commanded ON a shorted load can be detected.

The fault bit is "set" for each channel if a short, open, or over-temperature condition occurs for Outputs1-8. The content of this Fault Register is given in *Table 10*.

The output load status of each individual channel is defined in *Table 11*. Open and shorts are subsequently re-latched provided they meet the minimum duration criterion and thermal faults will be re-latched provided they meet the duration criterion after CS goes "LOW", if these fault conditions are still present.

The fault register is capable of detecting and latching multiple fault conditions (among the 8 outputs) that have occurred between clearing of the fault flags.

All of the faults will be cleared on the falling edge of Chip Select (CS).

Table 10. Fault register definition

MSB							LSB
Fault8	Fault7	Fault6	Fault5	Fault4	Fault3	Fault2	Fault1
D07	D06	D05	D04	D03	D02	D01	D00

Table 11. Fault logic definition

BIT	STATE	STATUS
Fault1-8	0	OUT1-8 are not open or shorted (nominal)
Fault1-8	1	OUT1-8 are either open or shorted or in thermal shutdown

3.7.1 Initial fault register SPI Cycle

After initial application of VDD to the L9848, the fault register is "Cleared" by the POR circuitry during the initial SPI cycle, and all subsequent cycles, valid fault data will be clocked out of DO (fault bits). The bits that are "Set" indicate which particular output(s) have a fault condition.

3.7.2 Incandescent lamp outputs

Software filtering may be needed to ignore fault signals due to the long turn on delay associated with lamp loads. For example, the lamp load channel gets enabled during one SPI cycle. Approximately 20ms-100ms later, a SPI cycle is required to read the correct fault latch data, which will be cleared after the falling edge of CS of that SPI cycle.

3.8 Configuration for Output1-6

The drain and source pins for each output must be connected in one of the two following configurations (see Figure 6a and Figure 6b).

3.8.1 Low side drivers

When any combination of Output1-6 are connected in a low side drive configuration the source of the applicable output (SRC1-6) has to be connected to ground. The drain of the applicable output (DRN1-6) has to be connected to the low side of the load.

3.8.2 High side drivers

When any combination of Output1-6 are connected in a high side drive configuration the drain of the applicable output (DRN1-6) has to be connected to VBatt. The source of the applicable output (SRC1-6) has to be connected to the high side of the load.

3.9 DRN1-6 susceptibility to negative voltage transients

For any output(s) connected and used for a high side drive a fast negative transient slew rate does not inadvertently issue a POR (power on reset) or cause parasitic latching to occur. Nevertheless under some conditions it may be necessary to have a ceramic chip capacitor of 10nF to 100nF connected from drain to GND to aid in preventing the occurance of a problem due to very fast negative transient(s) on the drain(s) of the device.

3.10 Thermal shutdown

Each of the 8 outputs have independent thermal protection circuitry that disables each output driver once the local n-channel MOSFET device temperature reaches the overtemperature shutdown limit. Due to the hysteresis of the enable and disable temperature levels the faulted channel will periodically turn off and on until the fault condition is cleared, the ambient temperature is decreased sufficiently or the output is commanded OFF.

Once any individual channel goes into thermal shutdown, a logic "1" is latched into the Fault Register if it meets the thermal fault filter (Note: does NOT go through the open/short fault filter).

Note: Due to the design of the L9848 each output's thermal limit "may not" be truly independent to the extent that if one output is shorted, it may impact the operation of other outputs (due to lateral heating in the die). The user may be required to monitor the fault bits periodically. If a fault bit is "Set" for the last enabled output, and subsequently, fault bits for other enabled outputs start to be "Set", the user will send two SPI write cycles within 100ms of each other. The first SPI write cycle will "Clear" the fault latches. If multiple faults are indicated after the second SPI write cycle, these faults are most likely thermal faults. The user will then disable this output that was most recently enabled. The fault register should be subsequently interrogated to verify proper operations of the other enabled output channels.

3.11 Charge pump usage

The L9848 uses a separate charge pump and oscillator for each of the 6 configurable output channels to provide low RDSON values when connected in a high side configuration These oscillators are operating in a non-synchronous mode of operation. The frequency range of these charge pumps is designed to be above the AM radio band and below 8.0 MHz so that harmonics do not get within the FM radio band.

3.12 Waveshaping

Both the turn on and the turn off slew rates on all outputs (OUTPUT1-8) are limited to reduce conducted EMC energy in the vehicle's wiring harness.

The characteristic of the turn-on and turn-off voltage is linear, with no discontinuities, during the output driver state transition.

3.13 POR register initialization

L9848 wakes up if the VDD supply increases from 0 to 5VDC in 0.3ms to 3ms.

The L9848 has a POR circuit, which monitors the VDD voltage. When the VDD voltage reaches roughly 4.1VDC, and remains above this trip level for minimum 20µs, the Command and Fault Registers are "cleared". Before VDD reaches this trip level, all eight outputs are guaranteed in OFF-state.

After a valid POR has occurred and the VDD voltage falls below the valid high level for a required amount of time, the L9848 is powered down in a fully controlled manner. No outputs will glitch "ON" and no erroneous fault data is allowed on the DO output.

3.14 Abnormal voltage conditions

The L9848 survives the following abnormal voltage conditions.

3.14.1 Reverse Battery

applied either directly, or through a load to the drain pins (DRN1-6) with the source pins (SRC1-6) connected to a load or to ground (cold lamp, solenoid, etc).

3.14.2 Maximum negative transients

that force the drains or sources of the outputs going -20V below the module ground.

3.14.3 Ground offsets

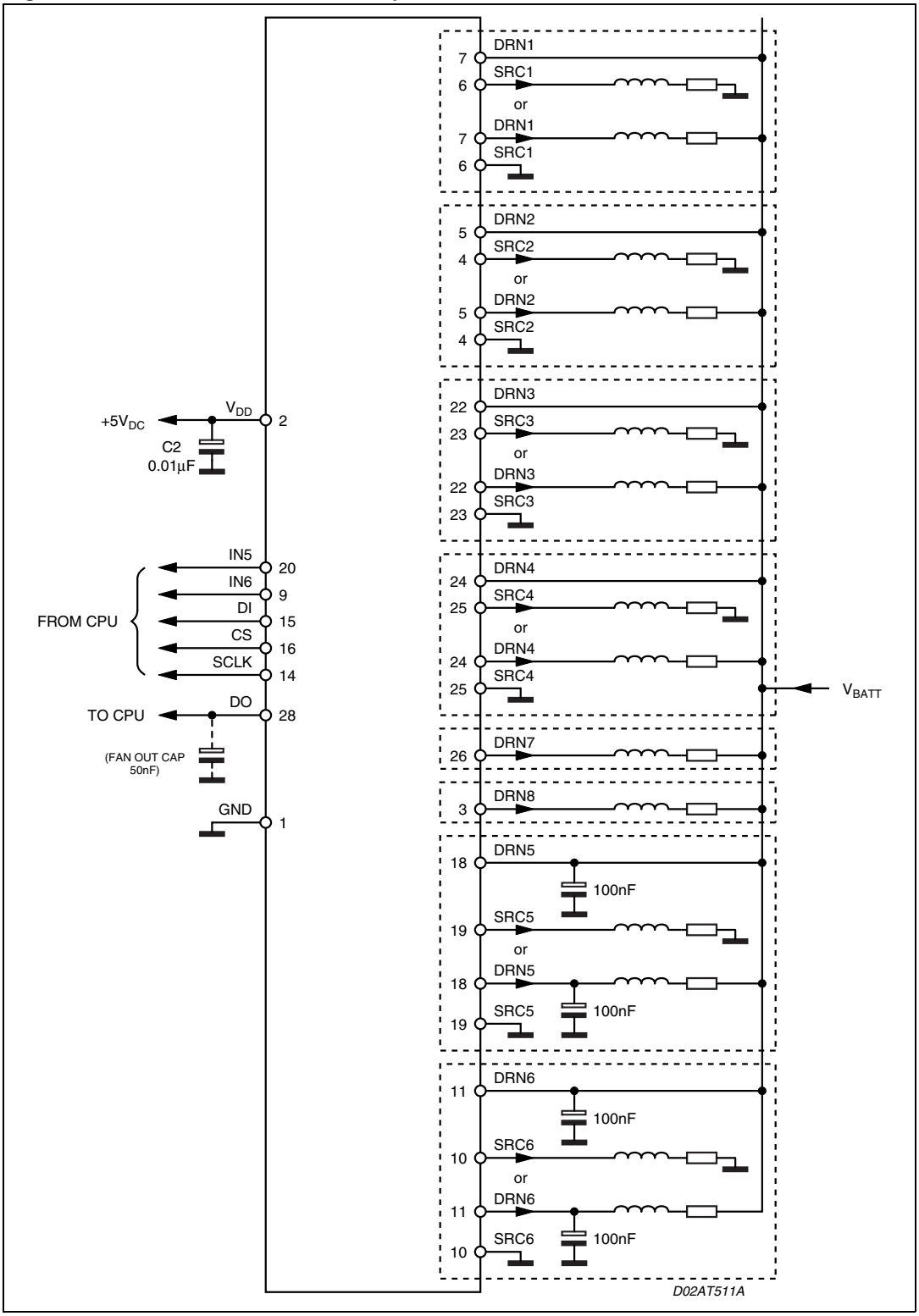
with a maximum of -0.5V to 1.0V between the L9848 ground and any load directly connected to a chassis ground in the case of high side loads. If driving a low side load there will not be an offset between the L9848 ground and the load ground. In addition there may be a maximum ground difference between the L9848 ground and any other module interfacing with it of -0.5V to 1.0V or ±VAC (10-200Hz).

3.14.4 Loss of ground operation

Any outputs are protected to become active in case of lost ground of the L9848 module with the supply is still applied.

4 Functional block diagram

Figure 8. L9848 with external components



5 Application examples

Figure 9. L9848 as mirror axis control motor drivers

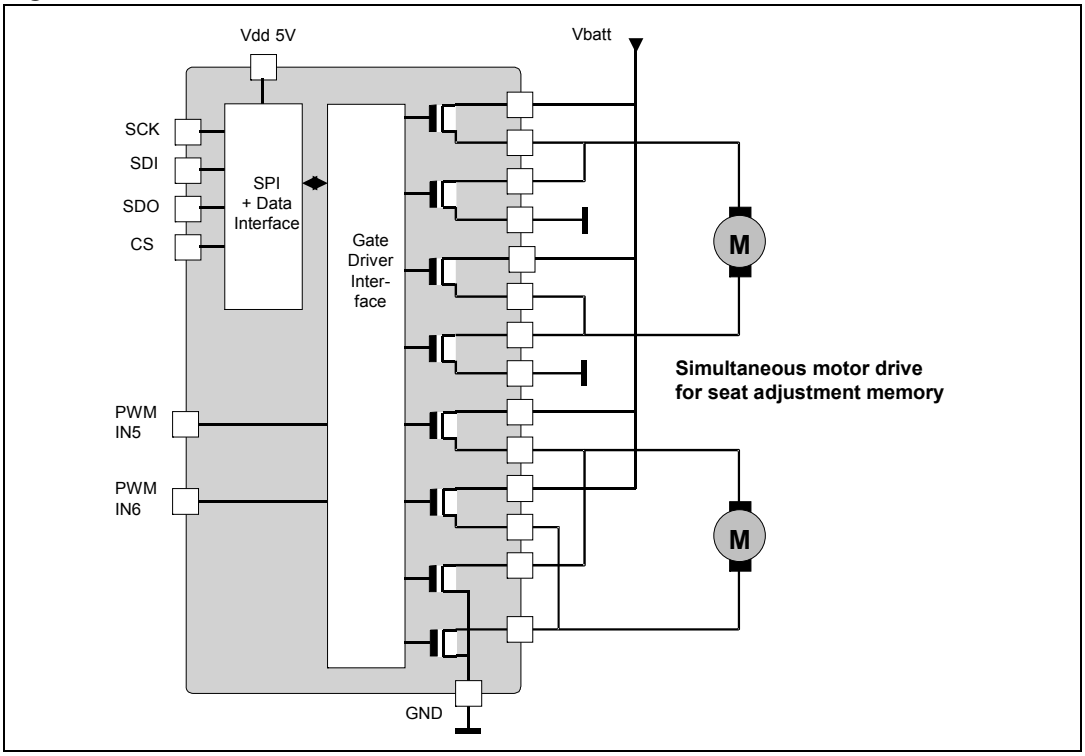


Figure 10. L9848 as mirror motor and bulb driver

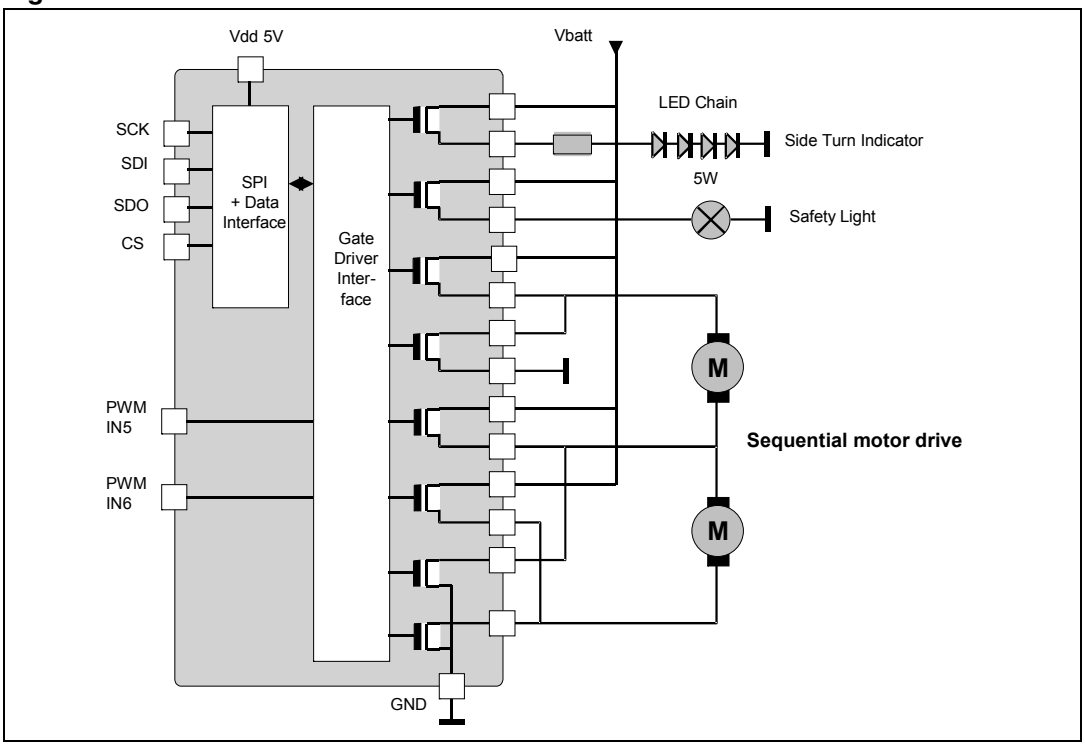


Figure 11. L9848 as window lift relay and mirror motor driver

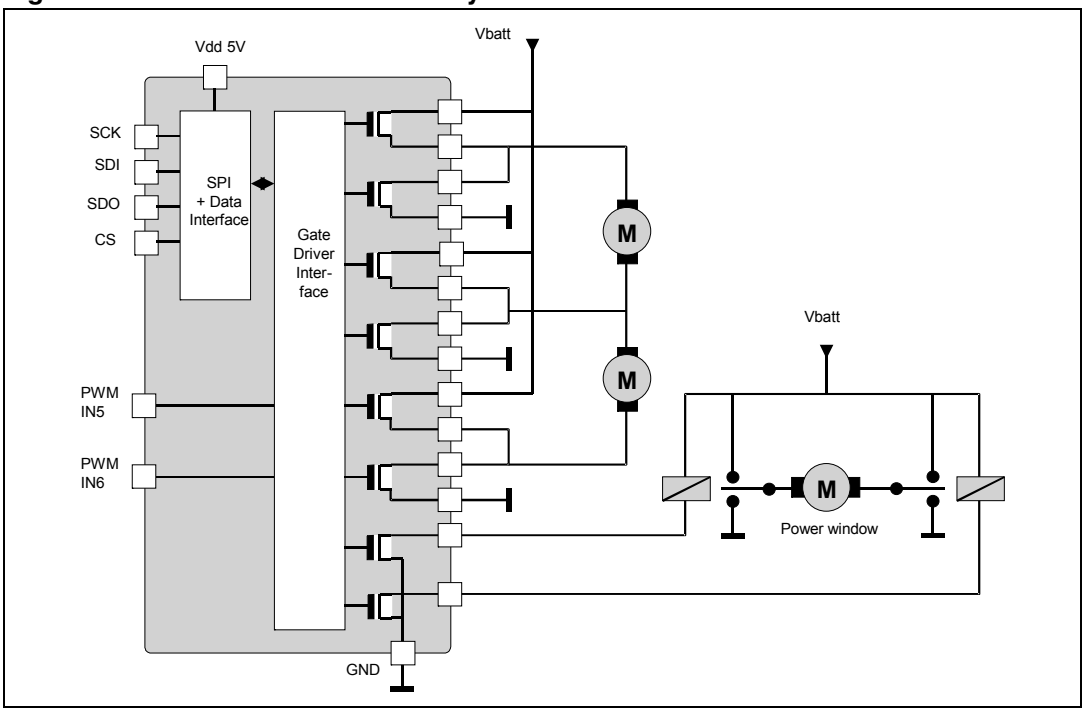


Figure 12. L9848 as bipolar stepper motor driver

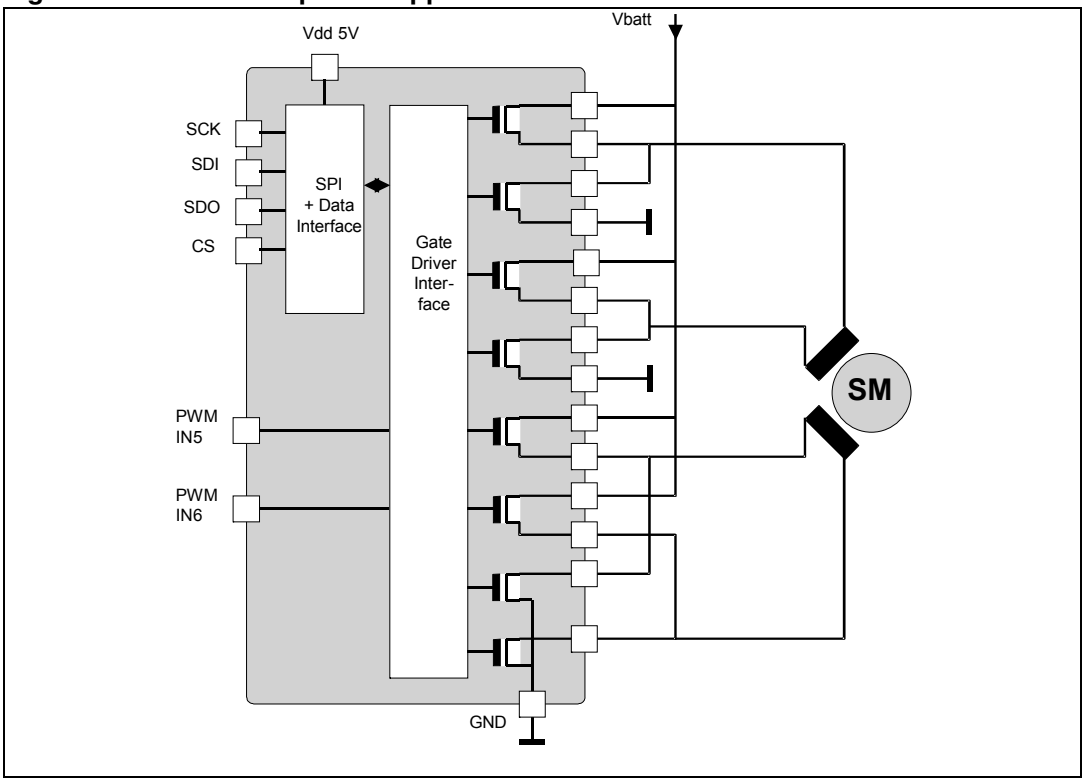
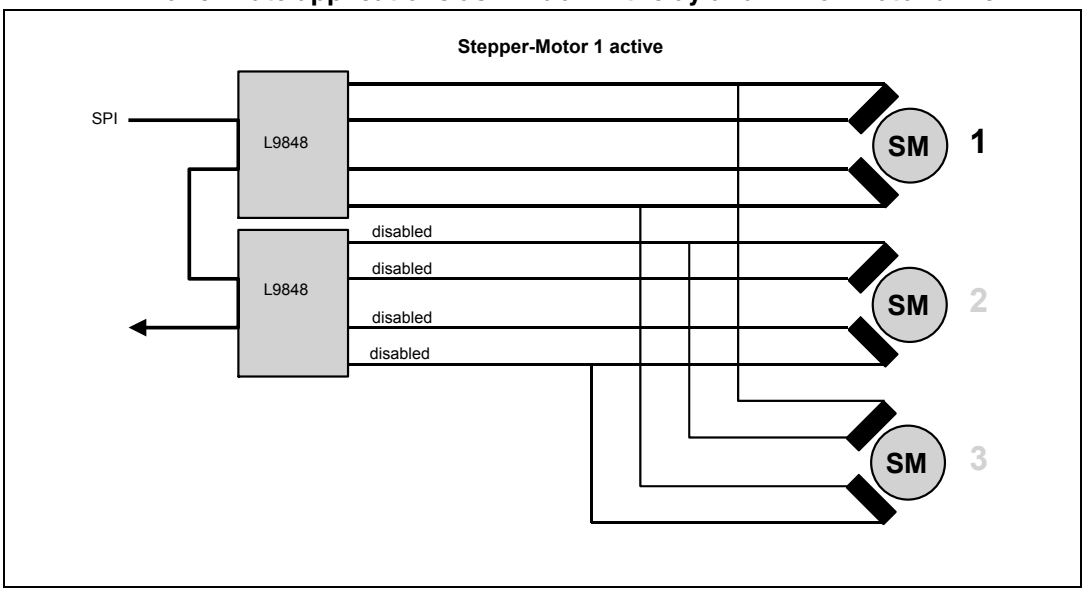


Figure 13. L9848 driving approach for 3 bipolar stepper-motors in sequential mode for climate applications as window lift relay and mirror motor driver



6 Package information

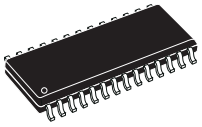
In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

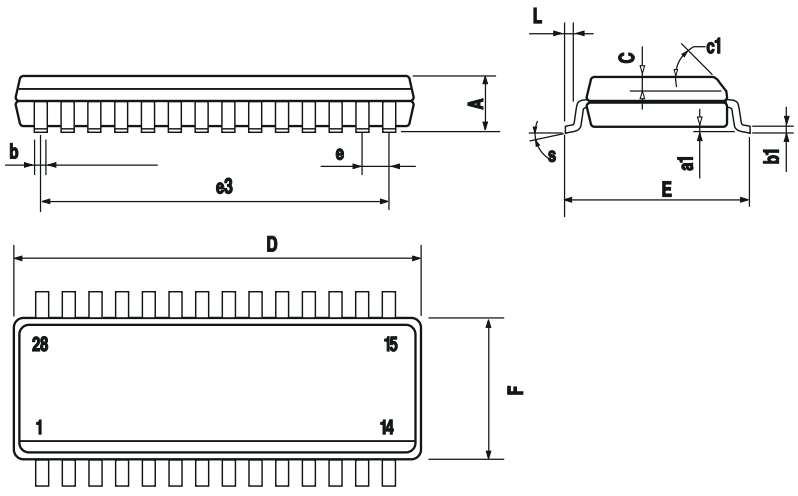
Figure 14. SO-28 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28



7 Revision history

Table 12. Document revision history

Date	Revision	Changes
12-Jul-2003	4	Initial release.
18-Nov-2008	5	Document reformatted. Updated *Table 2: Pin description*. Updated *Figure 8: L9848 with external components*. Updated *Section 6: Package information on page 25*.
19-Sep-2013	6	Updated Disclaimer.

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