## Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Barrana		_			T
	Parameter	Min	Тур	Мах	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-100	_	_	V	VGS = 0V, ID = -1.0mA
ΔBVDSS/ΔTJ	Temperature Coefficient of Breakdown Voltage	_	-0.1	_	V/°C	Reference to 25°C, ID = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	_	_	0.30	Ω	VGS = -10V, ID = -7.1A <sub>④</sub>
VGS(th)	Gate Threshold Voltage	-2.0	_	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
9fs	Forward Transconductance	2.5	_	_	S (7)	V <sub>DS</sub> > -15V, I <sub>DS</sub> = -7.1A ④
IDSS	Zero Gate Voltage Drain Current		_	-25	μА	V <sub>DS</sub> = -80V ,V <sub>GS</sub> =0V
		_	_	-250		V <sub>DS</sub> = -80V,
						VGS = 0V, TJ = 125°C
IGSS	Gate-to-Source Leakage Forward	_	_	-100	nA	V <sub>GS</sub> = -20V
IGSS	Gate-to-Source Leakage Reverse	_	_	100	I IIA	VGS = 20V
Qg	Total Gate Charge	_	_	30		Vgs = -10V, ID = -11.2A
Qgs	Gate-to-Source Charge	_	_	7.1	nC	V <sub>DS</sub> = -50V
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge		_	2.1		
<sup>t</sup> d(on)	Turn-On Delay Time		_	60		V <sub>DD</sub> = -50V, I <sub>D</sub> = -11.2A,
tr	Rise Time	_	_	140		$R_G = 7.5\Omega$
<sup>t</sup> d(off)	Turn-Off Delay Time		_	140	ns	
tf	Fall Time		_	140		
LS+LD	Total Inductance	_	6.8	_	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from
0.	lanut Canacitanas		000			package)
Ciss	Input Capacitance		800			$V_{GS} = 0V, V_{DS} = -25V$
Coss	Output Capacitance		350	_	pF	f = 1.0MHz
C <sub>rss</sub>	Reverse Transfer Capacitance		125	_		

## **Source-Drain Diode Ratings and Characteristics**

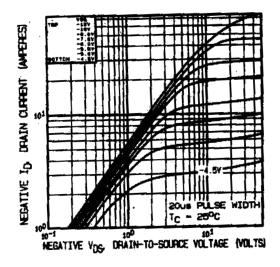
	Parameter		Min	Тур	Max	Units	Test Conditions
Is	Continuous Source Current (Body	inuous Source Current (Body Diode)11.2					
ISM	Pulse Source Current (Body Diode) ①		_	_	-44	Α	
VSD	Diode Forward Voltage		_	_	-4.7	V	$T_j = 25$ °C, $I_S = -11.2$ A, $V_{GS} = 0$ V ④
t <sub>rr</sub>	Reverse Recovery Time		_	_	250	nS	Tj = 25°C, IF = -11.2A, di/dt $\leq$ -100A/μs
QRR	Reverse Recovery Charge		_	_	3.0	μC	V <sub>DD</sub> ≤ -50V ④
ton	Forward Turn-On Time Intrins	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$ .					

## **Thermal Resistance**

	Parameter	Min	Тур	Max	Units	Test Conditions
RthJC	Junction-to-Case	_	_	1.67		
R <sub>th</sub> CS	Case-to-sink	_	0.21	_	°C/W	
R <sub>th</sub> JA	Junction-to-Ambient	_	_	80		Typical socket mount

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

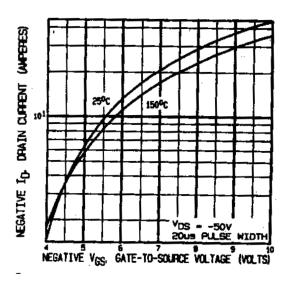


20US PULSE WIDTH
TC = 150°C

NEGATIVE VDS. OPAIN-70-SOURCE VOLTAGE (VOLTS)

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics



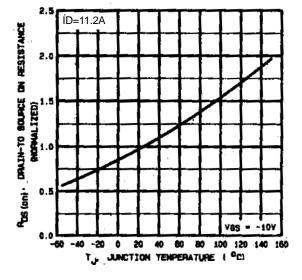
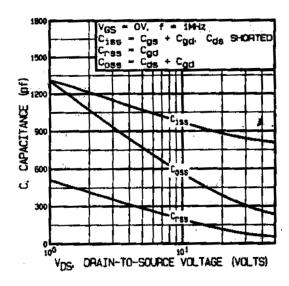


Fig 3. Typical Transfer Characteristics

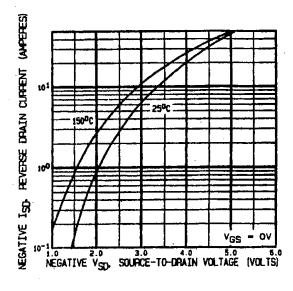
**Fig 4.** Normalized On-Resistance Vs. Temperature

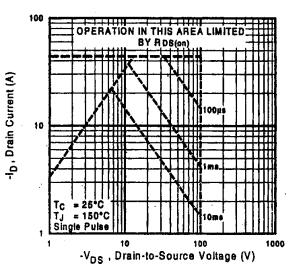


POR TEST CINCUIT SEE FIRMINE 13 CM d SO SO GO TOTAL BATE CHARGE (AC)

**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

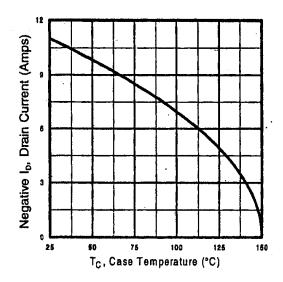
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage





**Fig 7.** Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature

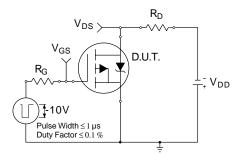


Fig 10a. Switching Time Test Circuit

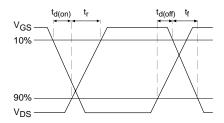


Fig 10b. Switching Time Waveforms

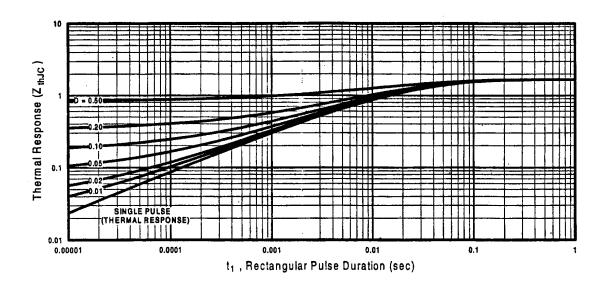


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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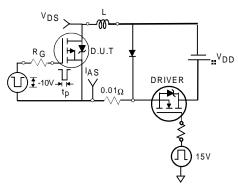


Fig 12a. Unclamped Inductive Test Circuit

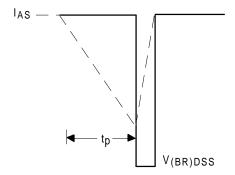


Fig 12b. Unclamped Inductive Waveforms

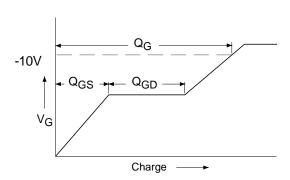


Fig 13a. Basic Gate Charge Waveform

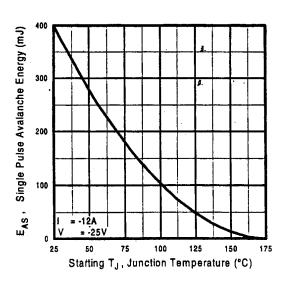


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

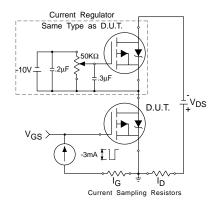


Fig 13b. Gate Charge Test Circuit

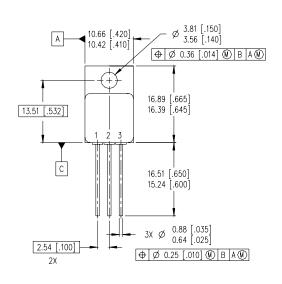
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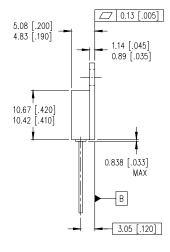


#### **Foot Notes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② VDD = -25V, starting TJ = 25°C, L = 6.4mH Peak  $I_L = -11.2$ A,  $V_{GS} = -10V$
- 3 ISD  $\leq$  -11.2A, di/dt  $\leq$  -140A/ $\mu$ s, VDD  $\leq$  -100V, TJ  $\leq$  150°C
- ④ Pulse width ≤ 300  $\mu$ s; Duty Cycle ≤ 2%

### Case Outline and Dimensions — TO-257AA



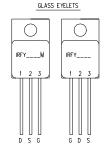


#### NOTES:

- 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.



G - GATE



# International TOR Rectifier

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TAC Fax: (310) 252-7903

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