

## Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Drain-Source Breakdown Voltage	$BV_{DSS}$	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	17	25	m $\Omega$	$V_{GS} = 4.5V, I_D = 7.0A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current	$I_{DSS}$	—	—	100	$\mu A$	$V_{DS} = 30V, V_{GS} = 0$
		—	—	20		$V_{DS} = 24V, V_{GS} = 0$
		—	—	100		$V_{DS} = 24V, V_{GS} = 0, T_J = 100^\circ C$
Gate-Source Leakage Current*	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20V$
Total Gate Charge*	$Q_G$	—	9.5	14	nC	$V_{GS} = 5V, I_D = 7.0A$ $V_{DS} = 16V$
Pre-Vth Gate-Source Charge	$Q_{GS1}$	—	2.3	—		
Post-Vth Gate-Source Charge	$Q_{GS2}$	—	1.0	—		
Gate-to-Drain Charge	$Q_{GD}$	—	2.4	—		
Switch Charge ( $Q_{GS2} + Q_{GD}$ )	$Q_{SW}$	—	3.4	5.2		
Output Charge*	$Q_{OSS}$	—	12	16.8		$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	$R_G$	0.9	—	2.8	$\Omega$	
Turn-On Delay Time	$t_{d(on)}$	—	6.3	—	ns	$V_{DD} = 16V$ $I_D = 7A$ $V_{GS} = 5V, R_G = 2\Omega$ Resistive Load
Rise Time	$t_r$	—	1.2	—		
Turn-Off Delay Time	$t_{d(off)}$	—	11	—		
Fall Time	$t_f$	—	2.2	—		

## Source-Drain Ratings and Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	$V_{SD}$	—	—	1.2	V	$I_S = 7.0A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge ④	$Q_{rr}$	—	64	—	nC	$di/dt = 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_S = 7.0A$
Reverse Recovery Charge (with Parallel Schottsky) ④	$Q_{rr(s)}$	—	41	—		$di/dt = 700A/\mu s$ , (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_S = 7.0A$

- Notes:**
- ① Repetitive rating; pulse width limited by max. junction temperature.
  - ② Pulse width  $\leq 400 \mu s$ ; duty cycle  $\leq 2\%$ .
  - ③ When mounted on 1 inch square copper board
  - ④ Typ = measured -  $Q_{oss}$
  - ⑤ Typical values of  $R_{DS(on)}$  measured at  $V_{GS} = 4.5V$ ,  $Q_G$ ,  $Q_{SW}$  and  $Q_{OSS}$  measured at  $V_{GS} = 5.0V$ ,  $I_F = 7.0A$ .
  - ⑥  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ C$

\* Device are 100% tested to these parameters.

## Power MOSFET Selection for DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the  $R_{ds(on)}$  of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left( I_{rms}^2 \times R_{ds(on)} \right) + \left( I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left( I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right) + (Q_g \times V_g \times f) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms  $Q_{gs2}$  and  $Q_{oss}$  which are new to Power MOSFET data sheets.

$Q_{gs2}$  is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements,  $Q_{gs1}$  and  $Q_{gs2}$ , can be seen from Fig 1.

$Q_{gs2}$  indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached (t1) and the time the drain current rises to  $I_{dmax}$  (t2) at which time the drain voltage begins to change. Minimizing  $Q_{gs2}$  is a critical factor in reducing switching losses in Q1.

$Q_{oss}$  is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure 2 shows how  $Q_{oss}$  is formed by the parallel combination of the voltage dependant (non-linear) capacitance's  $C_{ds}$  and  $C_{dg}$  when multiplied by the power supply input buss voltage.

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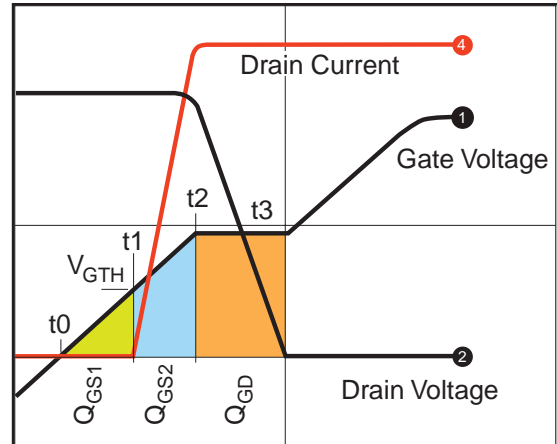


Figure 1: Typical MOSFET switching waveform

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^* \\ P_{loss} = \left( I_{rms}^2 \times R_{ds(on)} \right) + (Q_g \times V_g \times f) + \left( \frac{Q_{oss}}{2} \times V_{in} \times f \right) + (Q_{rr} \times V_{in} \times f)$$

\*dissipated primarily in Q1.

# IRF7807V

International  
IR Rectifier

For the synchronous MOSFET Q2,  $R_{ds(on)}$  is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge  $Q_{oss}$  and reverse recovery charge  $Q_{rr}$  both generate losses that are transferred to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to  $Cdv/dt$  turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and  $V_{in}$ . As Q1 turns on and off there is a rate of change of drain voltage  $dV/dt$  which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn

the MOSFET on, resulting in shoot-through current. The ratio of  $Q_{gd}/Q_{gs1}$  must be minimized to reduce the potential for  $Cdv/dt$  turn on.

Spice model for IRF7807V can be downloaded in machine readable format at [www.irf.com](http://www.irf.com).

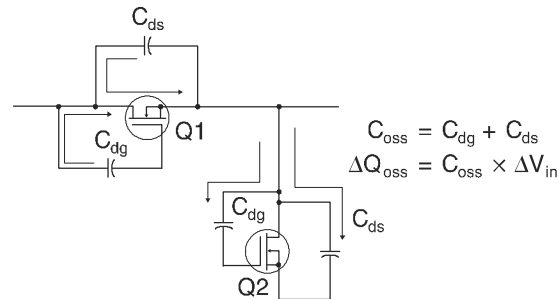


Figure 2:  $Q_{oss}$  Characteristic

## Typical Mobile PC Application

The performance of these new devices has been tested in circuit and correlates well with performance predictions generated by the system models. An advantage of this new technology platform is that the MOSFETs it produces are suitable for both control FET and synchronous FET applications. This has been demonstrated with the 3.3V and 5V converters. (Fig 3 and Fig 4). In these applications the same MOSFET IRF7807V was used for both the control FET (Q1) and the synchronous FET (Q2). This provides a highly effective cost/performance solution.

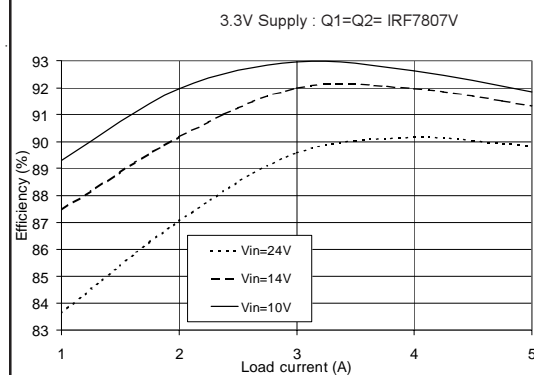


Figure 3

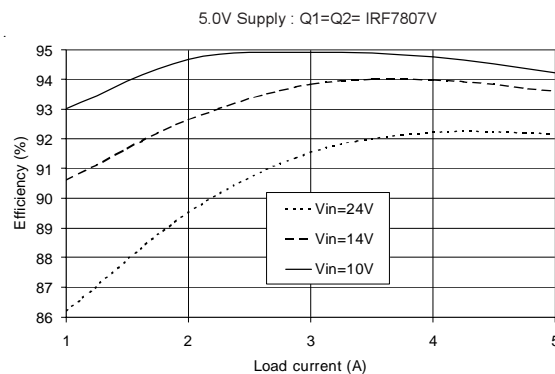
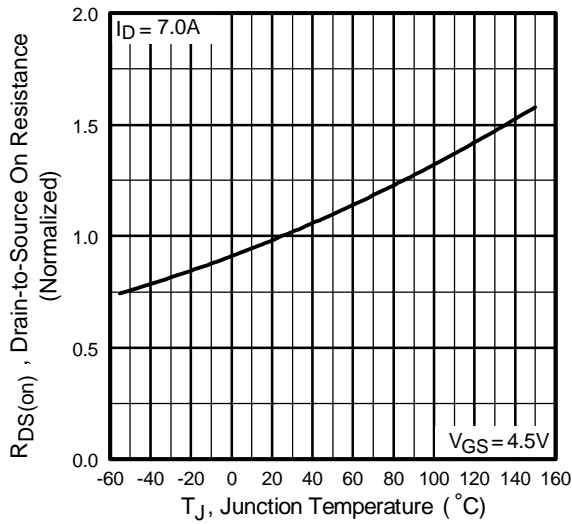
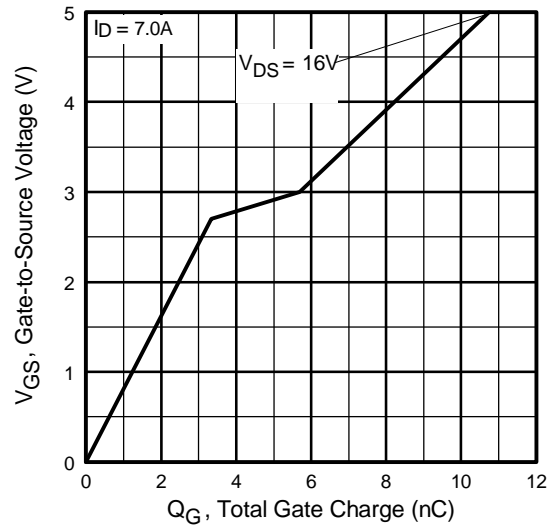


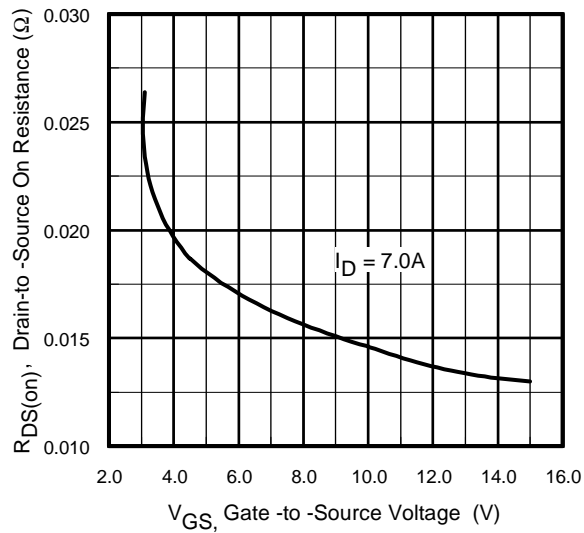
Figure 4



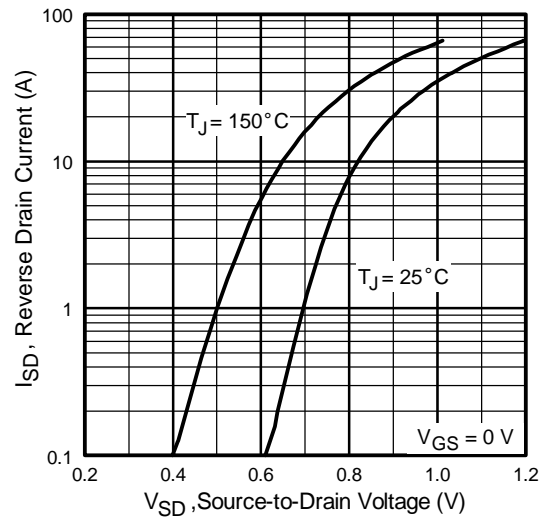
**Fig 5.** Normalized On-Resistance Vs. Temperature



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** On-Resistance Vs. Gate Voltage



**Fig 8.** Typical Source-Drain Diode Forward Voltage

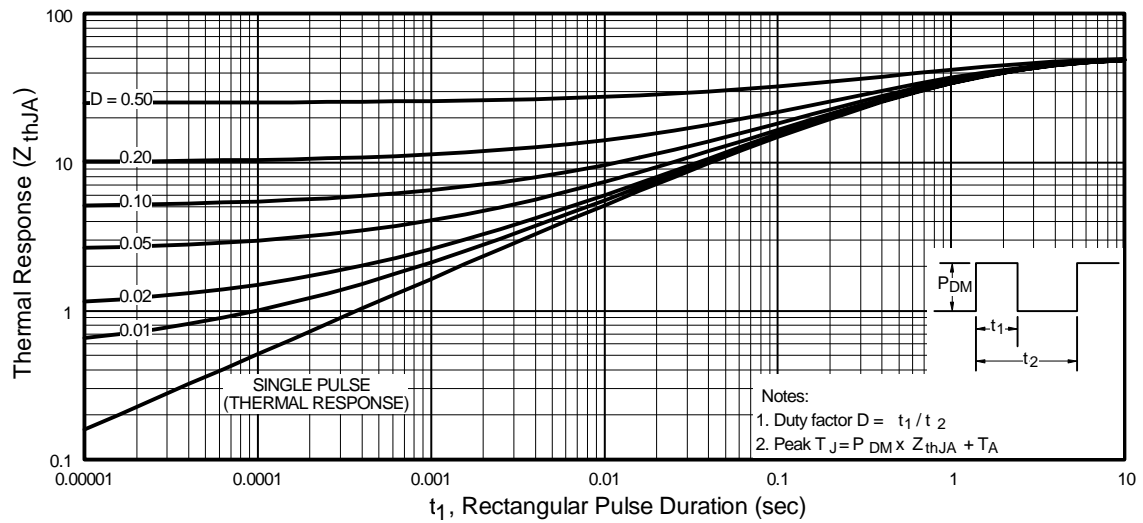
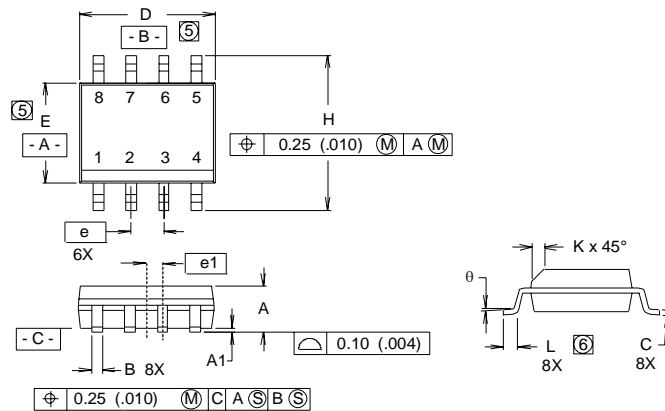


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

## SO-8 Package Details

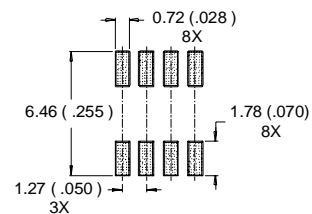


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS  
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- ⑥ DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

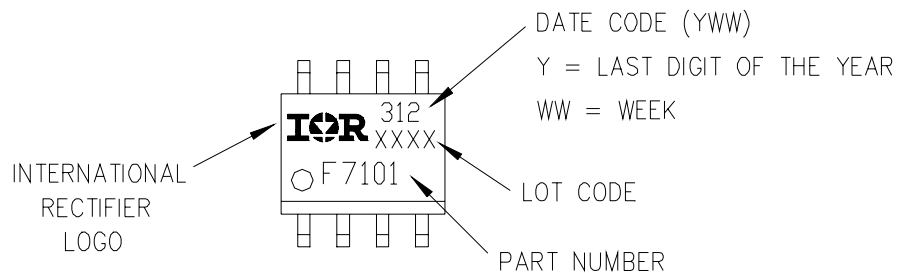
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

### RECOMMENDED FOOTPRINT



## SO-8 Part Marking

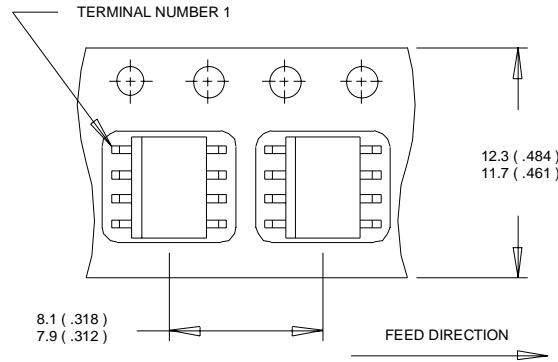
EXAMPLE: THIS IS AN IRF7101



# IRF7807V

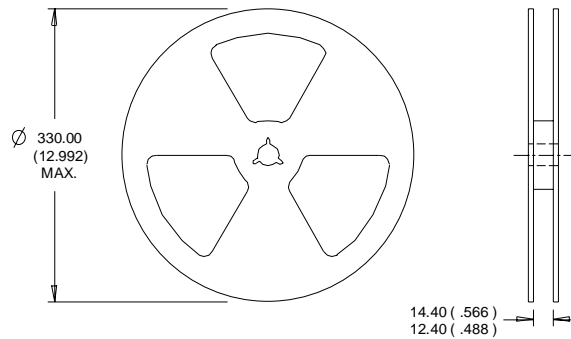
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## SO-8 Tape and Reel



### NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



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1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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