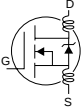


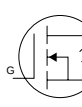
IRF7401

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.044	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.022	Ω	$V_{GS} = 4.5V, I_D = 4.1A$ ③
		—	—	0.030		$V_{GS} = 2.7V, I_D = 3.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	11	—	—	S	$V_{DS} = 15V, I_D = 4.1A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	25		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 12V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -12V$
Q_g	Total Gate Charge	—	—	48	nC	$I_D = 4.1A$
Q_{gs}	Gate-to-Source Charge	—	—	5.1		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		$V_{GS} = 4.5V$, See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 10V$ $I_D = 4.1A$ $R_G = 6.0\Omega$ $R_D = 2.4\Omega$, See Fig. 10 ③
t_r	Rise Time	—	72	—		
$t_{d(off)}$	Turn-Off Delay Time	—	65	—		
t_f	Fall Time	—	92	—		
L_D	Internal Drain Inductance	—	2.5	—	nH	Between lead tip and center of die contact 
L_S	Internal Source Inductance	—	4.0	—		
C_{iss}	Input Capacitance	—	1600	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	690	—		
C_{rss}	Reverse Transfer Capacitance	—	310	—		

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	35		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 2.0A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	39	59	ns	$T_J = 25^\circ\text{C}, I_F = 4.1A$
Q_{rr}	Reverse Recovery Charge	—	42	63	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② $I_{SD} \leq 4.1A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

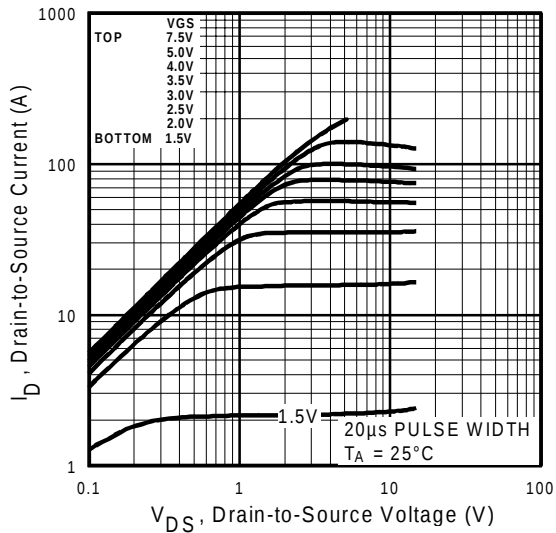


Fig 1. Typical Output Characteristics

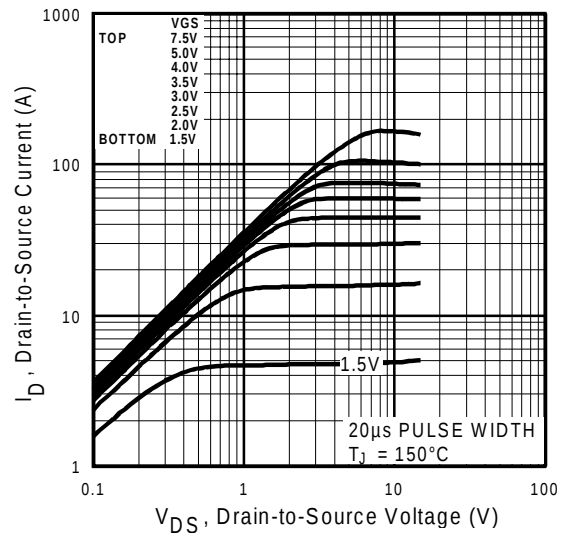


Fig 2. Typical Output Characteristics

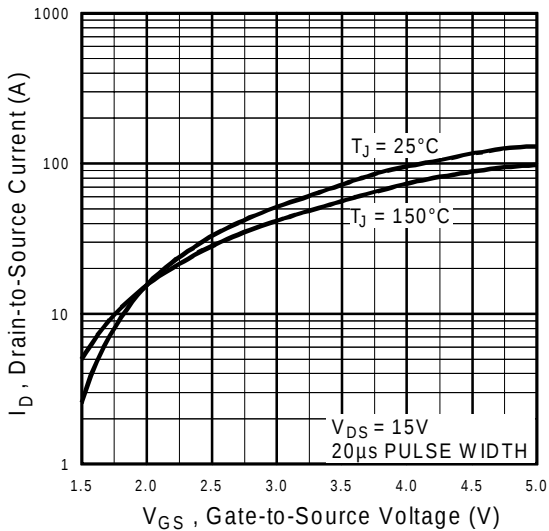


Fig 3. Typical Transfer Characteristics

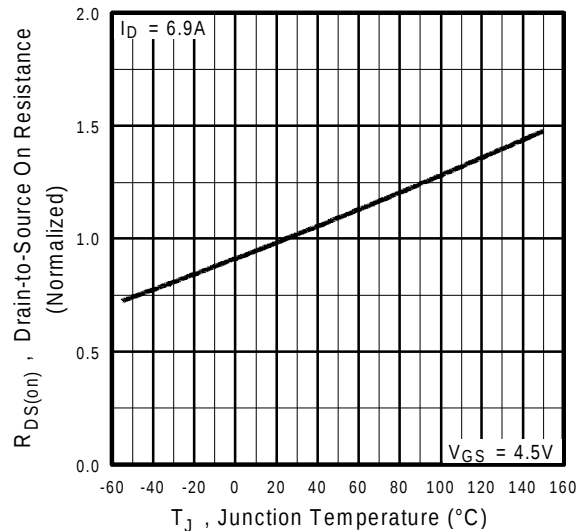


Fig 4. Normalized On-Resistance Vs. Temperature

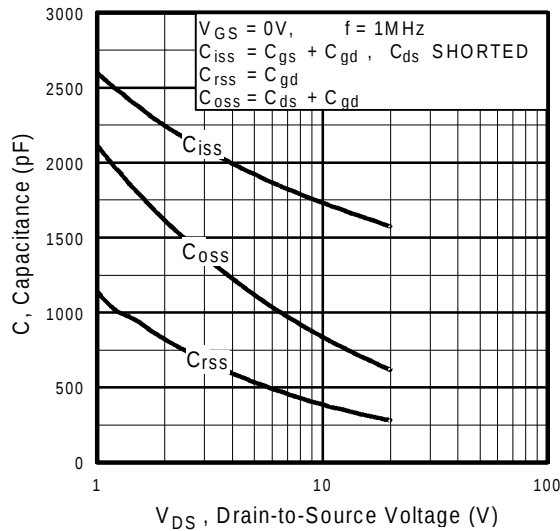


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

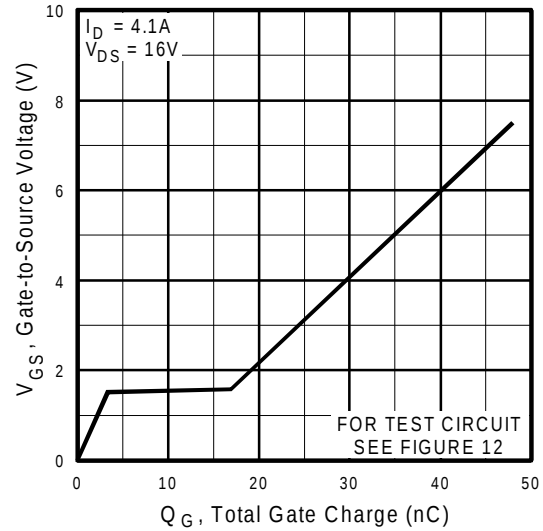


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

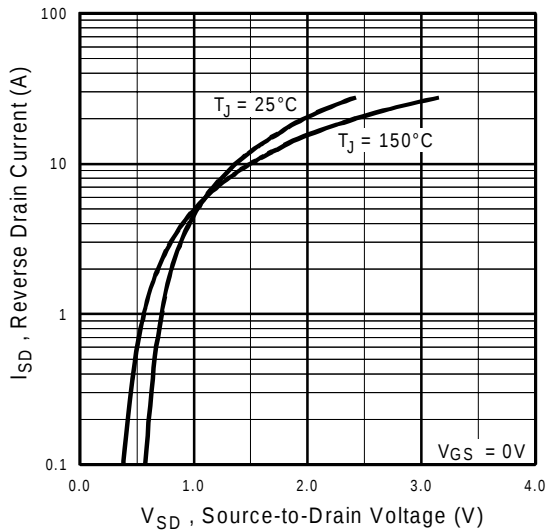


Fig 7. Typical Source-Drain Diode Forward Voltage

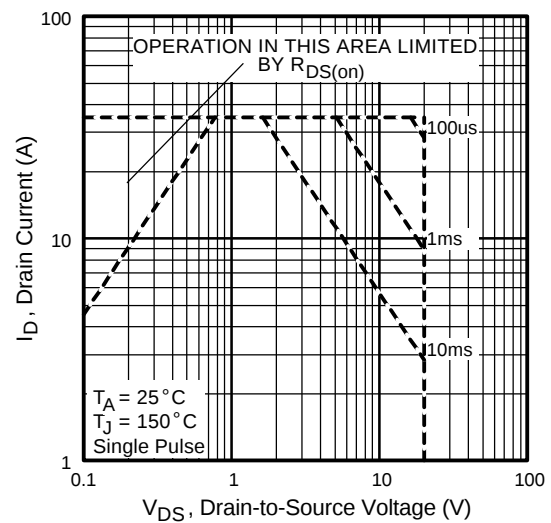


Fig 8. Maximum Safe Operating Area

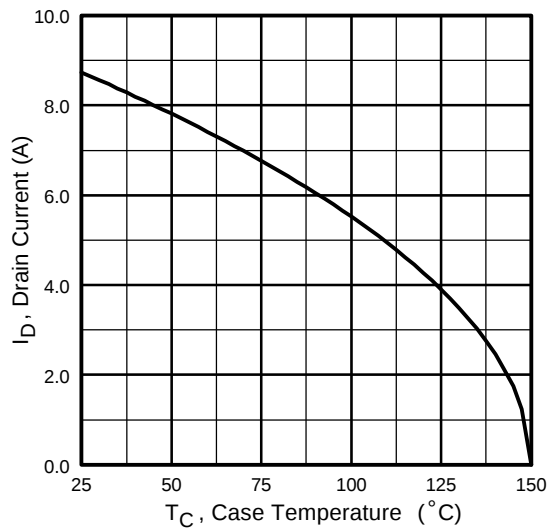


Fig 9. Maximum Drain Current Vs. Ambient Temperature

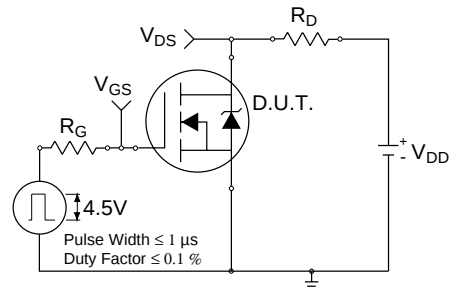


Fig 10a. Switching Time Test Circuit

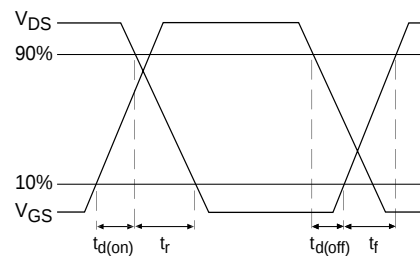


Fig 10b. Switching Time Waveforms

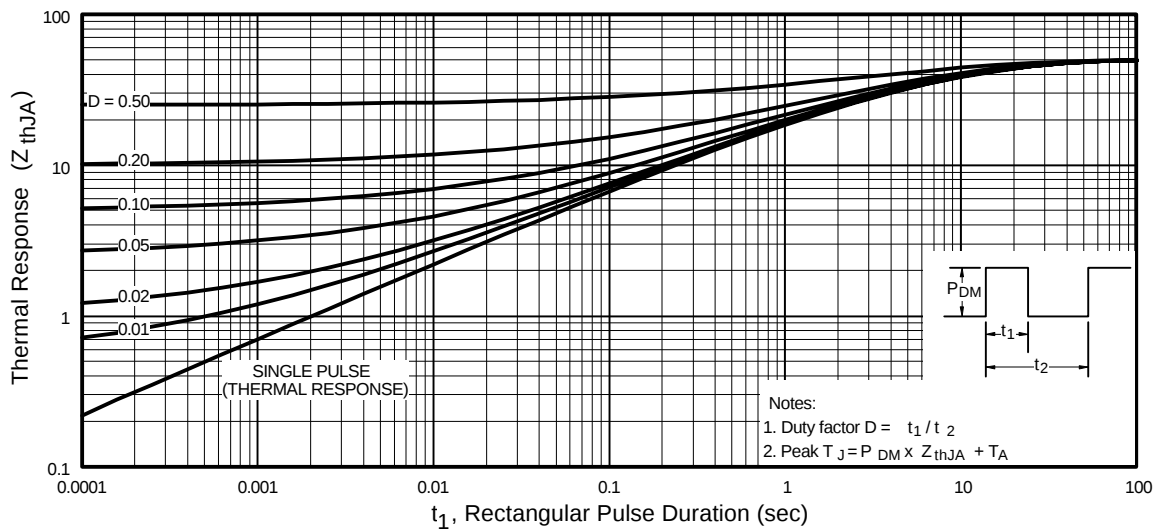


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

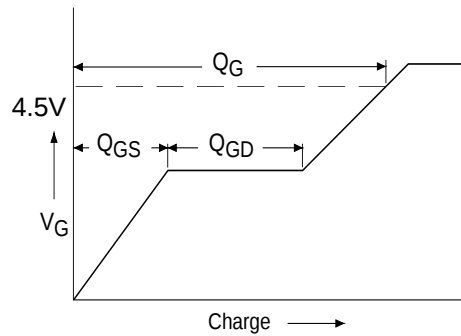


Fig 12a. Basic Gate Charge Waveform

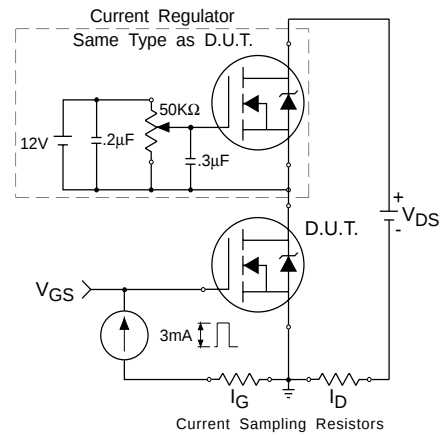
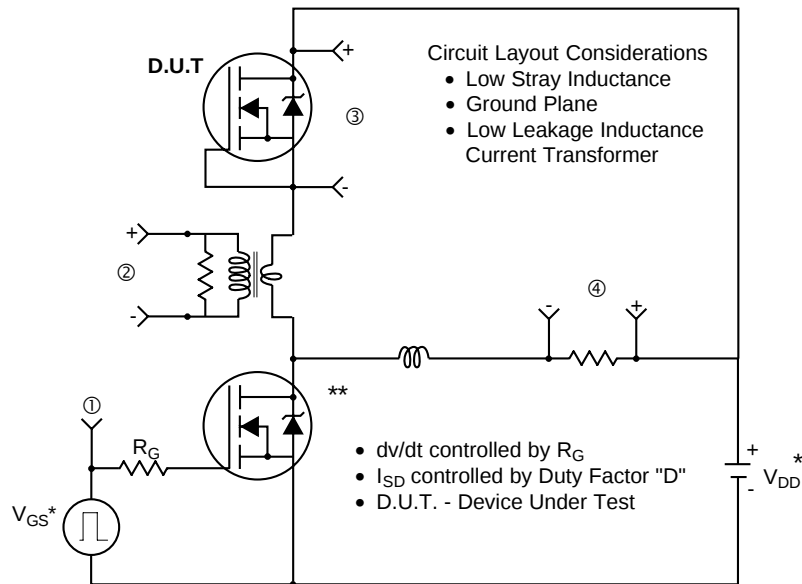


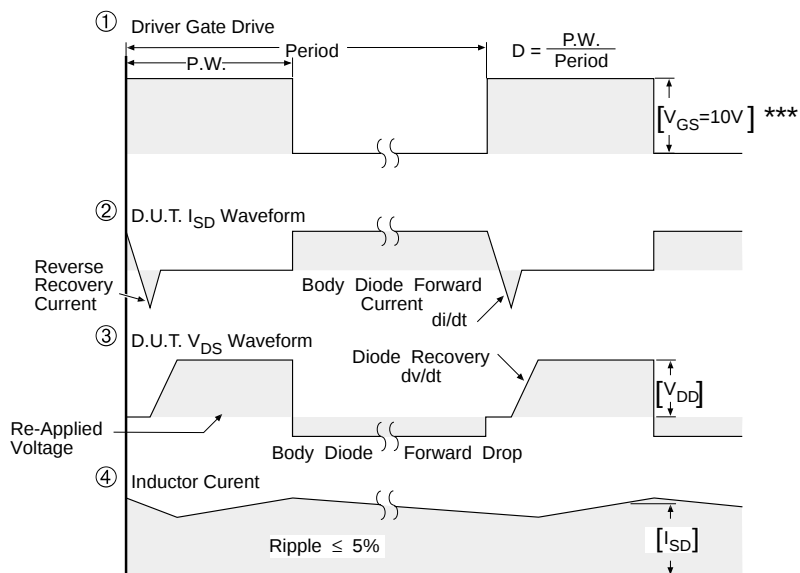
Fig 12b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 13. For N-Channel HEXFETS

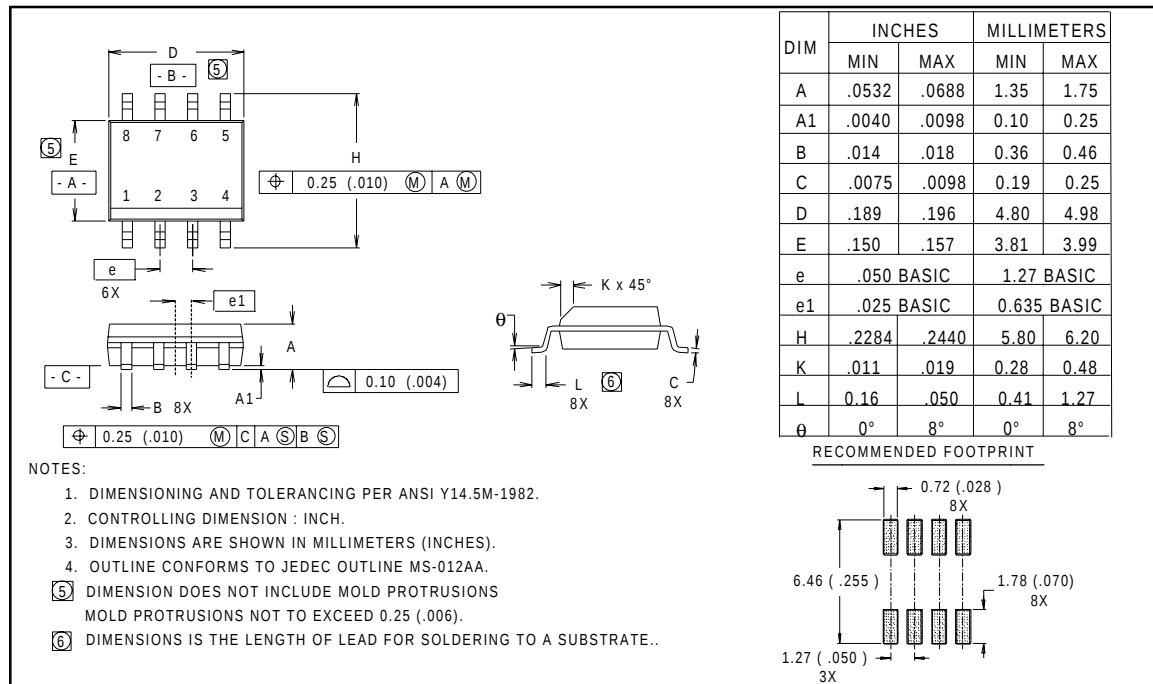
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Package Outline

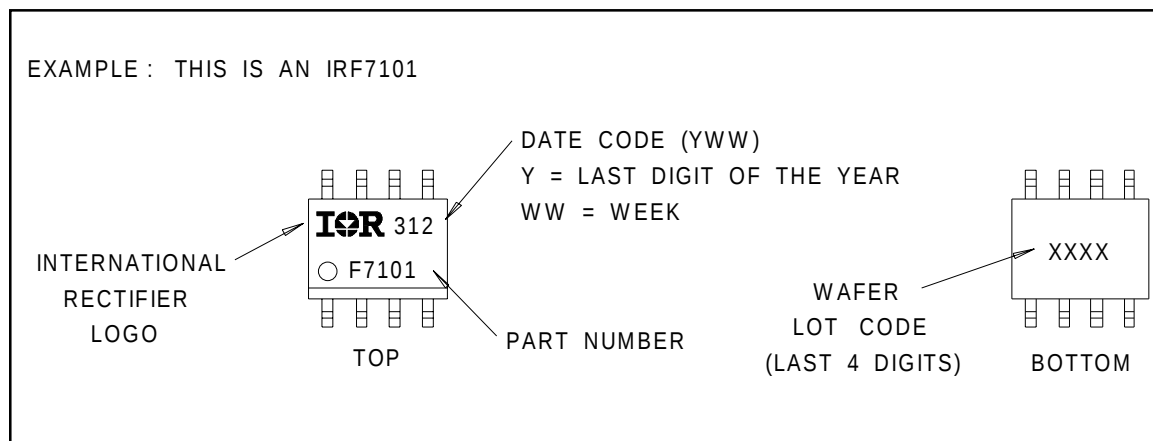
SO-8 Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

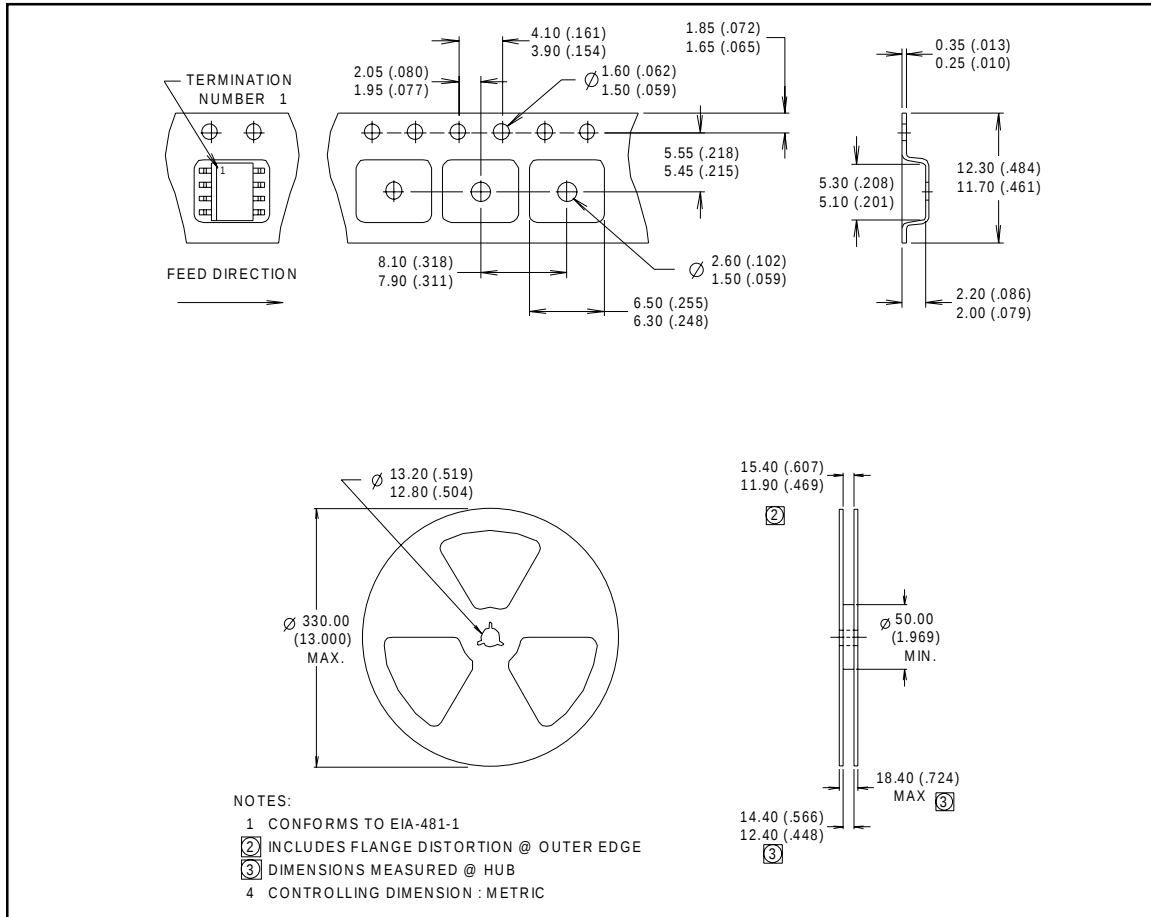
SO-8



Tape & Reel Information

SO-8

Dimensions are shown in millimeters (inches)



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Data and specifications subject to change without notice.

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