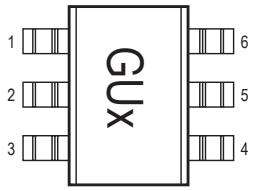
Pin Connections and Package Marking



Notes:
1. Package marking provides orientation and identification.
2. See "Electrical Specifications" for appropriate package marking.

Absolute Maximum Ratings[1] $T_C = 25°C$

Symbol	Parameter	Unit	SOT-23/SOT-143	SOT-323/SOT-363
I_f	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	15	15
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance[2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. T_C = +25°C, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications $T_C = 25°C$, Single Diode[3]

Part Number HSMS[4]	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	Maximum Forward Voltage V_F (V) @ I_F (mA)	Maximum Reverse Leakage I_R (nA) @ V_R (V)	Maximum Capacitance C_T (pF)	Typical Dynamic Resistance R_D (Ω)[5]
2820	C0	0	Single	15	340	0.5 10	100 1	1.0	12
2822	C2	2	Series						
2823	C3	3	Common Anode						
2824	C4	4	Common Cathode						
2825	C5	5	Unconnected Pair						
2827	C7	7	Ring Quad[4]						
2828	C8	8	Bridge Quad[4]						
2829	C9	9	Cross-over Quad						
282B	C0	B	Single						
282C	C2	C	Series						
282E	C3	E	Common Anode						
282F	C4	F	Common Cathode						
282K	CK	K	High Isolation Unconnected Pair						
282L	CL	L	Unconnected Trio						
282M	HH	M	Common Cathode Quad						
282N	NN	N	Common Anode Quad						
282P	CP	P	Bridge Quad						
282R	OO	R	Ring Quad						
Test Conditions				I_R = 100 mA	I_F = 1 mA[1]			V_R = 0V[2] f = 1 MHz	I_F = 5 mA

Notes:
1. ΔV_F for diodes in pairs and quads in 15 mV maximum at 1 mA.
2. ΔC_{TO} for diodes in pairs and quads is 0.2 pF maximum.
3. Effective Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 5 mA.
4. See section titled "Quad Capacitance."
5. $R_D = R_S + 5.2\Omega$ at 25°C and I_f = 5 mA.

Quad Capacitance

Capacitance of Schottky diode quads is measured using an HP4271 LCR meter. This instrument effectively isolates individual diode branches from the others, allowing accurate capacitance measurement of each branch or each diode. The conditions are: 20 mV R.M.S. voltage at 1 MHz. Avago defines this measurement as "CM", and it is equivalent to the capacitance of the diode by itself. The equivalent diagonal and adjacent capaci-tances can then be calculated by the formulas given below.

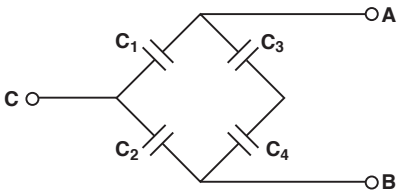
In a quad, the diagonal capacitance is the capacitance between points A and B as shown in the figure below. The diagonal capacitance is calculated using the following formula

$$C_{DIAGONAL} = \frac{C_1 \times C_2}{C_1 + C_2} + \frac{C_3 \times C_4}{C_3 + C_4}$$

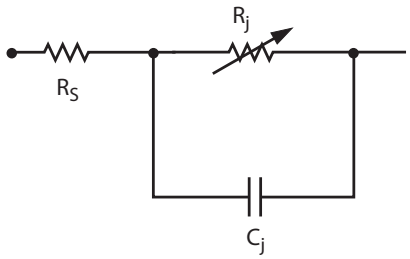
The equivalent adjacent capacitance is the capacitance between points A and C in the figure below. This capacitance is calculated using the following formula

$$C_{ADJACENT} = C_1 + \frac{1}{\frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4}}$$

This information does not apply to cross-over quad diodes.



Linear Equivalent Circuit Model Diode Chip



R_S = series resistance (see Table of SPICE parameters)

C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\ nT}{I_b + I_s}$$

where

I_b = externally applied bias current in amps

I_s = saturation current (see table of SPICE parameters)

T = temperature, K

n = ideality factor (see table of SPICE parameters)

Note:
To effectively model the packaged HSMS-282x product, please refer to Application Note AN1124.

ESD WARNING: **Handling Precautions Should Be Taken To Avoid Static Discharge.**

SPICE Parameters

Parameter	Units	HSMS-282x
B_V	V	15
C_{J0}	pF	0.7
E_G	eV	0.69
I_{BV}	A	1E-4
I_S	A	2.2E-8
N		1.08
R_S	Ω	6.0
P_B	V	0.65
P_T		2
M		0.5

Typical Performance, T_C = 25°C (unless otherwise noted), Single Diode

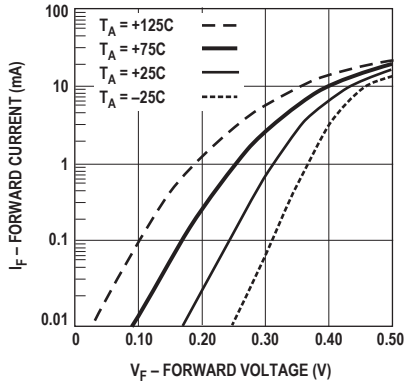


Figure 1. Forward Current vs. Forward Voltage at Temperatures.

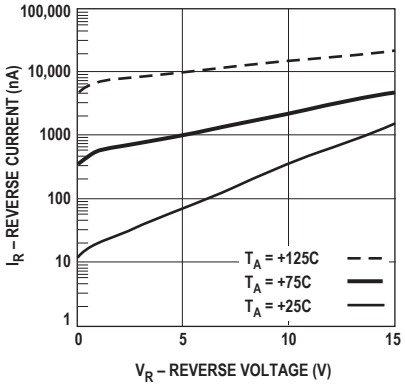


Figure 2. Reverse Current vs. Reverse Voltage at Temperatures.

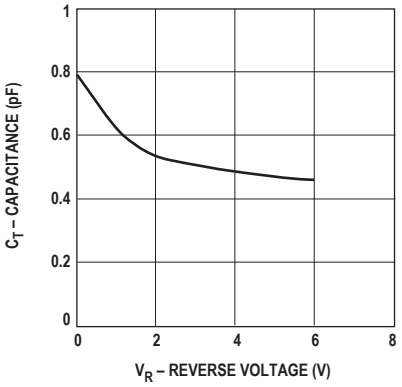


Figure 3. Total Capacitance vs. Reverse Voltage.

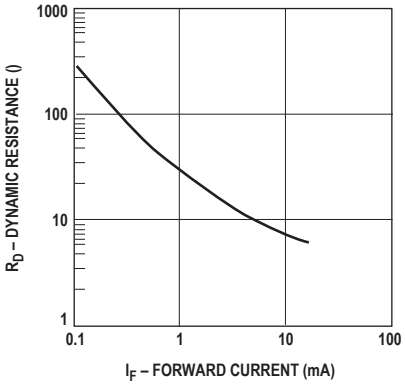


Figure 4. Dynamic Resistance vs. Forward Current.

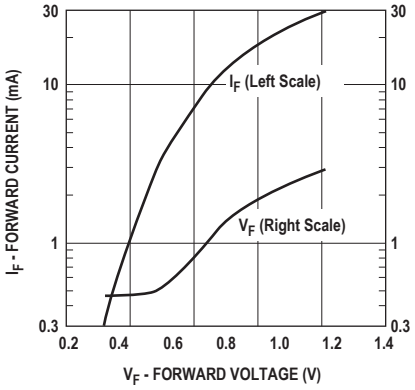


Figure 5. Typical V_f Match, Series Pairs and Quads at Mixer Bias Levels.

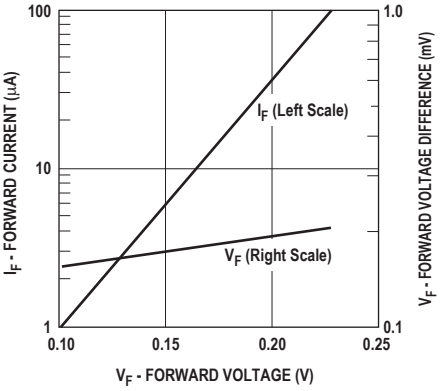


Figure 6. Typical V_f Match, Series Pairs at Detector Bias Levels.

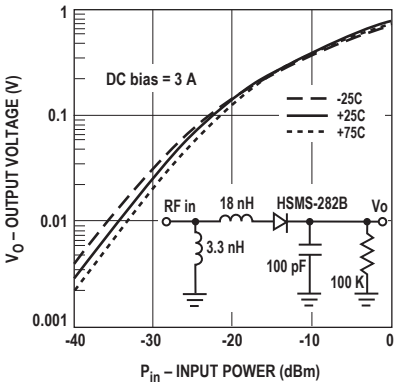


Figure 7. Typical Output Voltage vs. Input Power, Small Signal Detector Operating at 850 MHz.

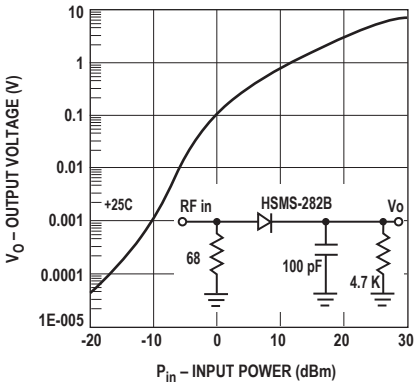


Figure 8. Typical Output Voltage vs. Input Power, Large Signal Detector Operating at 915 MHz.

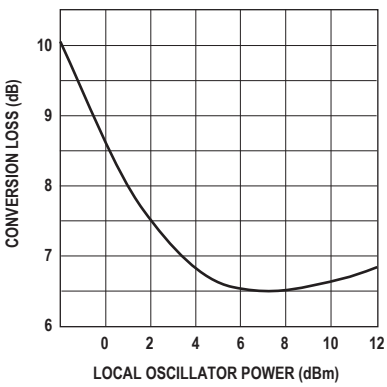


Figure 9. Typical Conversion Loss vs. L.O. Drive, 2.0 GHz (Ref AN997).

Applications Information

Product Selection

Avago's family of surface mount Schottky diodes provide unique solutions to many design problems. Each is optimized for certain applications.

The first step in choosing the right product is to select the diode type. All of the products in the HSMS-282x family use the same diode chip – they differ only in package configuration. The same is true of the HSMS-280x, -281x, 285x, -286x and -270x families. Each family has a different set of characteristics, which can be compared most easily by consulting the SPICE parameters given on each data sheet.

The HSMS-282x family has been optimized for use in RF applications, such as

- DC biased small signal detectors to 1.5 GHz.
- Biased or unbiased large signal detectors (AGC or power monitors) to 4 GHz.
- Mixers and frequency multipliers to 6 GHz.

The other feature of the HSMS-282x family is its unit-to-unit and lot-to-lot consistency. The silicon chip used in this series has been designed to use the fewest possible processing steps to minimize variations in diode characteristics. Statistical data on the consistency of this product, in terms of SPICE parameters, is available from Avago.

For those applications requiring very high breakdown voltage, use the HSMS-280x family of diodes. Turn to the HSMS-281x when you need very low flicker noise. The HSMS-285x is a family of zero bias detector diodes for small signal applications. For high frequency detector or mixer applications, use the HSMS-286x family. The HSMS-270x is a series of specialty diodes for ultra high speed clipping and clamping in digital circuits.

Schottky Barrier Diode Characteristics

Stripped of its package, a Schottky barrier diode chip consists of a metal-semiconductor barrier formed by deposition of a metal layer on a semiconductor. The most common of several different types, the passivated diode, is shown in Figure 10, along with its equivalent circuit.

R_S is the parasitic series resistance of the diode, the sum of the bondwire and leadframe resistance, the resistance of the bulk layer of silicon, etc. RF energy coupled into R_S is lost as heat—it does not contribute to the rectified output of the diode. C_J is parasitic junction capacitance of the diode, controlled by the thick-ness of the epitaxial layer and the diameter of the Schottky contact. R_j is the junction resistance of the diode, a function of the total current flowing through it.

$$R_j = \frac{8.33 \times 10^{-5} nT}{I_S + I_b} = R_V - R_s$$

$$\approx \frac{0.026}{I_S + I_b} \text{ at } 25\,^{\circ}C$$

where

n = ideality factor (see table of SPICE parameters)
T = temperature in °K
I_S = saturation current (see table of SPICE parameters)
I_b = externally applied bias current in amps
R_v = sum of junction and series resistance, the slope of the V-I curve

I_S is a function of diode barrier height, and can range from picoamps for high barrier diodes to as much as 5 µA for very low barrier diodes.

The Height of the Schottky Barrier

The current-voltage characteristic of a Schottky barrier diode at room temperature is described by the following equation:

$$I = I_S \left(e^{\frac{V - IR_S}{0.026}} - 1\right)$$

On a semi-log plot (as shown in the Avago catalog) the current graph will be a straight line with inverse slope 2.3 X 0.026 = 0.060 volts per cycle (until the effect of R_S is seen in a curve that droops at high current). All Schottky diode curves have the same slope, but not necessarily the same value of current for a given voltage. This is determined by the saturation current, I_S, and is related to the barrier height of the diode.

Through the choice of p-type or n-type silicon, and the selection of metal, one can tailor the characteristics of a Schottky diode. Barrier height will be altered, and at the same time C_J and R_S will be changed. In general, very low barrier height diodes (with high values of I_S, suitable for zero bias applications) are realized on p-type silicon. Such diodes suffer from higher values of R_S than do the n-type.

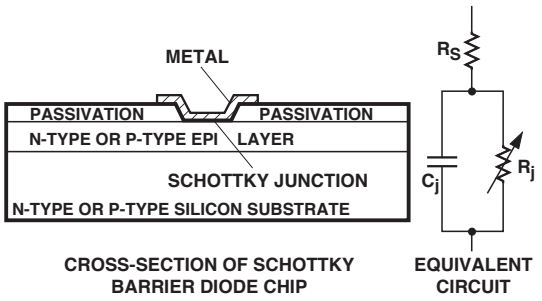


Figure 10. Schottky Diode Chip.

Thus, p-type diodes are generally reserved for detector applications (where very high values of R_V swamp out high R_S) and n-type diodes such as the HSMS-282x are used for mixer applications (where high L.O. drive levels keep R_V low). DC biased detectors and self-biased detectors used in gain or power control circuits.

Detector Applications

Detector circuits can be divided into two types, large signal (P_{in} > -20 dBm) and small signal (P_{in} < -20 dBm). In general, the former use resistive impedance matching at the input to improve flatness over frequency — this is possible since the input signal levels are high enough to produce adequate output voltages without the need for a high Q reactive input matching network. These circuits are self-biased (no external DC bias) and are used for gain and power control of amplifiers.

Small signal detectors are used as very low cost receivers, and require a reactive input impedance matching network to achieve adequate sensitivity and output voltage. Those operating with zero bias utilize the HSMS- 285x family of detector diodes. However, superior performance over temperature can be achieved with the use of 3 to 30 µA of DC bias. Such circuits will use the HSMS-282x family of diodes if the operating frequency is 1.5 GHz or lower.

Typical performance of single diode detectors (using HSMS-2820 or HSMS-282B) can be seen in the transfer curves given in Figures 7 and 8. Such detectors can be realized either as series or shunt circuits, as shown in Figure 11.

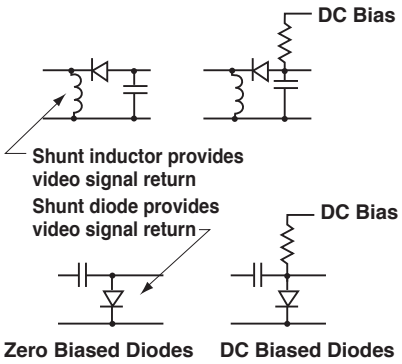


Figure 11. Single Diode Detectors.

The series and shunt circuits can be combined into a voltage doubler[1], as shown in Figure 12. The doubler offers three advantages over the single diode circuit.

- The two diodes are in parallel in the RF circuit, lowering the input impedance and making the design of the RF matching network easier.
- The two diodes are in series in the output (video) circuit, doubling the output voltage.
- Some cancellation of even-order harmonics takes place at the input.

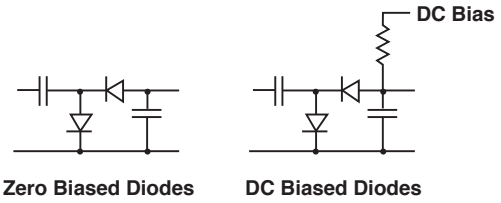


Figure 12. Voltage Doubler.

The most compact and lowest cost form of the doubler is achieved when the HSMS-2822 or HSMS-282C series pair is used.

Both the detection sensitivity and the DC forward voltage of a biased Schottky detector are temperature sensitive. Where both must be compensated over a wide range of temperatures, the differential detector[2] is often used. Such a circuit requires that the detector diode and the reference diode exhibit identical characteristics at all DC bias levels and at all temperatures. This is accomplished through the use of two diodes in one package, for example the HSMS-2825 in Figure 13. In the Avago assembly facility, the two dice in a surface mount package are taken from adjacent sites on the wafer (as illustrated in Figure 14). This assures that the characteristics of the two diodes are more highly matched than would be possible through individual testing and hand matching.

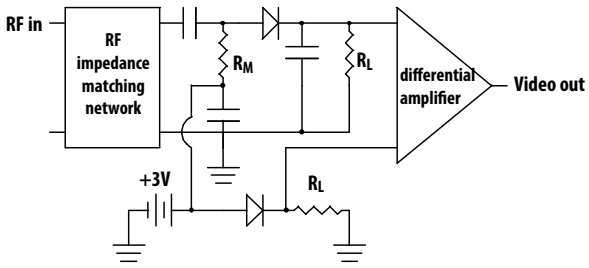


Figure 13. Differential Detector.

Notes:
1. Avago Application Note 956-4, "Schottky Diode Voltage Doubler."
2. Raymond W. Waugh, "Designing Large-Signal Detectors for Handsets and Base Stations," *Wireless Systems Design,* Vol. 2, No. 7, July 1997, pp 42 – 48.

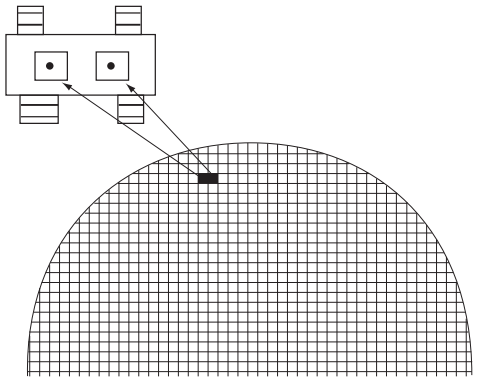


Figure 14. Fabrication of Avago Diode Pairs.

In high power applications, coupling of RF energy from the detector diode to the reference diode can introduce error in the differential detector. The HSMS-282K diode pair, in the six lead SOT-363 package, has a copper bar between the diodes that adds 10 dB of additional isolation between them. As this part is manufactured in the SOT-363 package it also provides the benefit of being 40% smaller than larger SOT-143 devices. The HSMS-282K is illustrated in Figure 15 — note that the ground connections must be made as close to the package as possible to minimize stray inductance to ground.

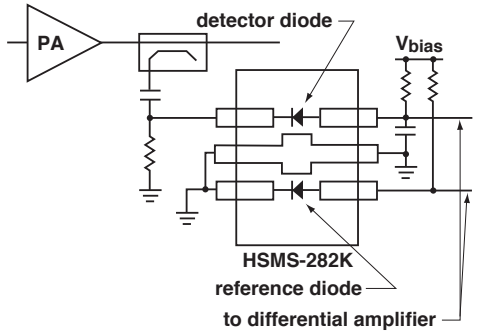


Figure 15. High Power Differential Detector.

The concept of the voltage doubler can be applied to the differential detector, permitting twice the output voltage for a given input power (as well as improving input impedance and suppressing second harmonics).

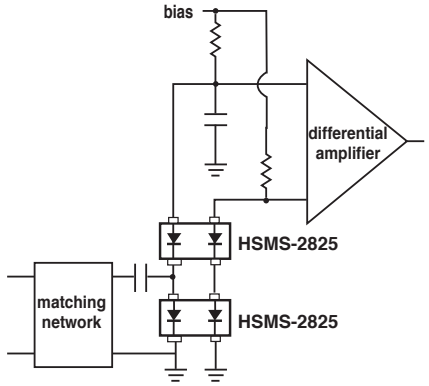


Figure 16. Voltage Doubler Differential Detector.

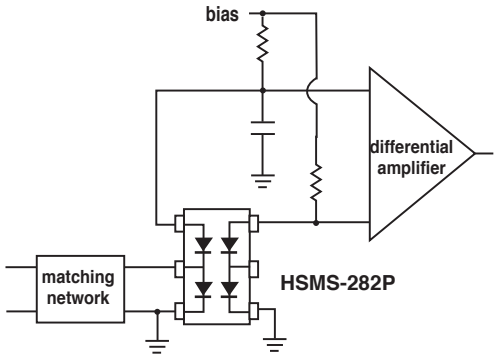


Figure 17. Voltage Doubler Differential Detector.

However, care must be taken to assure that the two reference diodes closely match the two detector diodes. One possible configuration is given in Figure 16, using two HSMS-2825. Board space can be saved through the use of the HSMS-282P open bridge quad, as shown in Figure 17.

While the differential detector works well over temperature, another design approach[3] works well for large signal detectors. See Figure 18 for the schematic and a physical layout of the circuit. In this design, the two 4.7 KΩ resistors and diode D2 act as a variable power divider, assuring constant output voltage over temperature and improving output linearity.

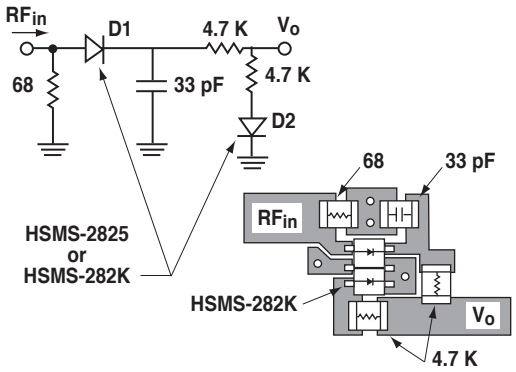
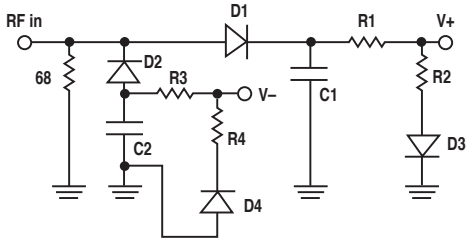


Figure 18. Temperature Compensated Detector.

In certain applications, such as a dual-band cellphone handset operating at both 900 and 1800 MHz, the second harmonics generated in the power control output detector when the handset is working at 900 MHz can cause problems. A filter at the output can reduce unwanted emissions at 1800 MHz in this case, but a lower cost solution is available[4]. Illustrated schematically in Figure 19, this circuit uses diode D2 and its associated passive components to cancel all even order harmonics at the detector's RF input. Diodes D3 and D4 provide temperature compensation as described above. All four diodes are contained in a single HSMS- 282R package, as illustrated in the layout shown in Figure 20.

Note 3. Hans Eriksson and Raymond W. Waugh, "A Temperature Compensated Linear Diode Detector," to be published.



C1 = C2 [a] 100 pF
R1 = R2 = R3 = R4 = 4.7 K
D1 & D2 & D3 & D4 = HSMS-282R

Figure 19. Schematic of Suppressed Harmonic Detector.

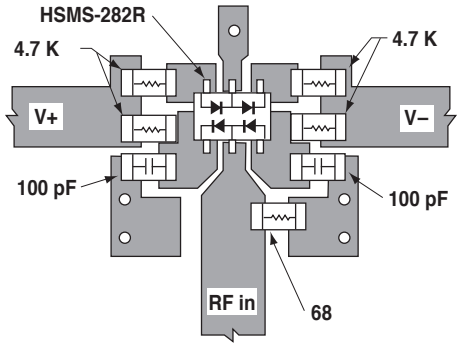


Figure 20. Layout of Suppressed Harmonic Detector.

Note that the forgoing discussion refers to the output voltage being extracted at point V+ with respect to ground. If a differential output is taken at V+ with respect to V-, the circuit acts as a voltage doubler.

Mixer applications

The HSMS-282x family, with its wide variety of packaging, can be used to make excellent mixers at frequencies up to 6 GHz.

The HSMS-2827 ring quad of matched diodes (in the SOT-143 package) has been designed for double balanced mixers. The smaller (SOT-363) HSMS-282R ring quad can similarly be used, if the quad is closed with external connections as shown in Figure 21.

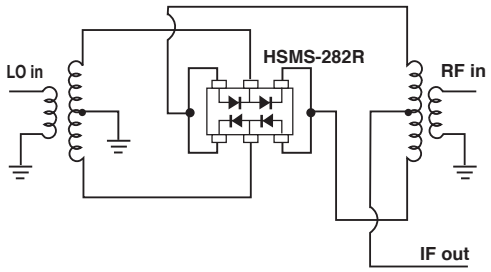


Figure 21. Double Balanced Mixer.

Both of these networks require a crossover or a three dimensional circuit. A planar mixer can be made using the SOT-143 crossover quad, HSMS-2829, as shown in Figure 22. In this product, a special lead frame permits the crossover to be placed inside the plastic package itself, eliminating the need for via holes (or other measures) in the RF portion of the circuit itself.

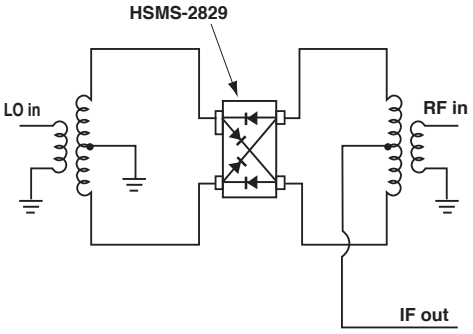


Figure 22. Planar Double Balanced Mixer.

A review of Figure 21 may lead to the question as to why the HSMS-282R ring quad is open on the ends. Distortion in double balanced mixers can be reduced if LO drive is increased, up to the point where the Schottky diodes are driven into saturation. Above this point, increased LO drive will not result in improvements in distortion. The use of expensive high barrier diodes (such as those fabricated on GaAs) can take advantage of higher LO drive power, but a lower cost solution is to use a eight (or twelve) diode ring quad. The open design of the HSMS-282R permits this to easily be done, as shown in Figure 23.

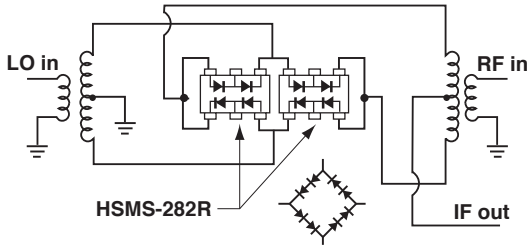


Figure 23. Low Distortion Double Balanced Mixer.

This same technique can be used in the single-balanced mixer. Figure 24 shows such a mixer, with two diodes in each spot normally occupied by one. This mixer, with a sufficiently high LO drive level, will display low distortion.

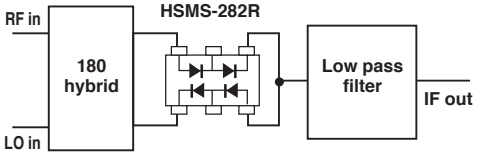


Figure 24. Low Distortion Balanced Mixer.

Note 4. Alan Rixon and Raymond W. Waugh, "A Suppressed Harmonic Power Detector for Dual Band 'Phones," to be published.

Sampling Applications

The six lead HSMS-282P can be used in a sampling circuit, as shown in Figure 25. As was the case with the six lead HSMS-282R in the mixer, the open bridge quad is closed with traces on the circuit board. The quad was not closed internally so that it could be used in other applications, such as illustrated in Figure 17.

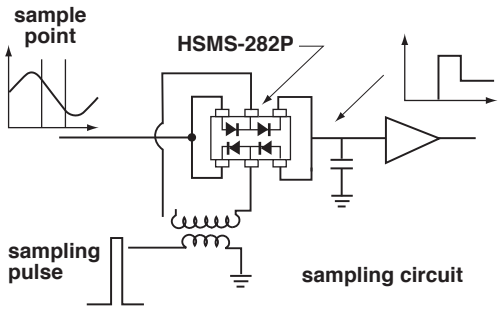


Figure 25. Sampling Circuit.

Thermal Considerations

The obvious advantage of the SOT-323 and SOT-363 over the SOT-23 and SOT-142 is combination of smaller size and extra leads. However, the copper leadframe in the SOT-3x3 has a thermal conductivity four times higher than the Alloy 42 leadframe of the SOT-23 and SOT-143, which enables the smaller packages to dissipate more power.

The maximum junction temperature for these three families of Schottky diodes is 150°C under all operating conditions. The following equation applies to the thermal analysis of diodes:

$$Tj = (V_f I_f + P_{RF})\,\theta_{jc} + T_a \qquad (1)$$

where

T_j = junction temperature
T_a = diode case temperature
θ_{jc} = thermal resistance
$V_f I_f$ = DC power dissipated
P_{RF} = RF power dissipated

Note that θ_{jc}, the thermal resistance from diode junction to the foot of the leads, is the sum of two component resistances,

$$\theta_{jc} = \theta_{pkg} + \theta_{chip} \qquad (2)$$

Package thermal resistance for the SOT-3x3 package is approximately 100°C/W, and the chip thermal resistance for the HSMS-282x family of diodes is approximately 40°C/W. The designer will have to add in the thermal resistance from diode case to ambient — a poor choice of circuit board material or heat sink design can make this number very high.

Equation (1) would be straightforward to solve but for the fact that diode forward voltage is a function of temperature as well as forward current. The equation for V_f is:

$$I_f = I_S \left[e^{\frac{11600\,(V_f - I_f R_s)}{nT}} - 1 \right]$$

where n = ideality factor
T = temperature in °K
R_s = diode series resistance
and I_S (diode saturation current) is given by

$$I_s = I_0 \left(\frac{T}{298} \right)^{\frac{2}{n}} e^{-4060\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Equation (4) is substituted into equation (3), and equations (1) and (3) are solved simultaneously to obtain the value of junction temperature for given values of diode case temperature, DC power dissipation and RF power dissipation.

Note 5. Avago Application Note 1050, "Low Cost, Surface Mount Power Limiters."

Diode Burnout

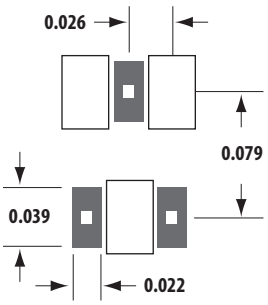
Any Schottky junction, be it an RF diode or the gate of a MESFET, is relatively delicate and can be burned out with excessive RF power. Many crystal video receivers used in RFID (tag) applications find themselves in poorly controlled environments where high power sources may be present. Examples are the areas around airport and FAA radars, nearby ham radio operators, the vicinity of a broadcast band transmitter, etc. In such environments, the Schottky diodes of the receiver can be protected by a device known as a limiter diode.[5] Formerly available only in radar warning receivers and other high cost electronic warfare applications, these diodes have been adapted to commercial and consumer circuits.

Avago offers a complete line of surface mountable PIN limiter diodes. Most notably, our HSMP-4820 (SOT-23) can act as a very fast (nanosecond) power-sensitive switch when placed between the antenna and the Schottky diode, shorting out the RF circuit temporarily and reflecting the excessive RF energy back out the antenna.

Assembly Instructions

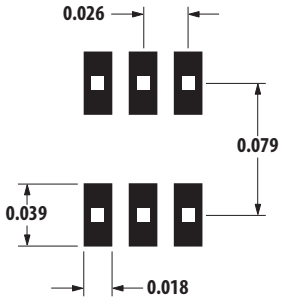
SOT-3x3 PCB Footprint

Recommended PCB pad layouts for the miniature SOT-3x3 (SC-70) packages are shown in Figures 26 and 27 (dimensions are in inches). These layouts provide ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.



Dimensions in inches

Figure 26. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.



Dimensions in inches

Figure 27. Recommended PCB Pad Layout for Avago's SC70 6L/SOT-363 Products.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT packages, will reach solder reflow temperatures faster than those with a greater mass.

Avago's diodes have been qualified to the time-temperature profile shown in Figure 28. This profile is representative of an IR reflow type of surface mount assembly process.

After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

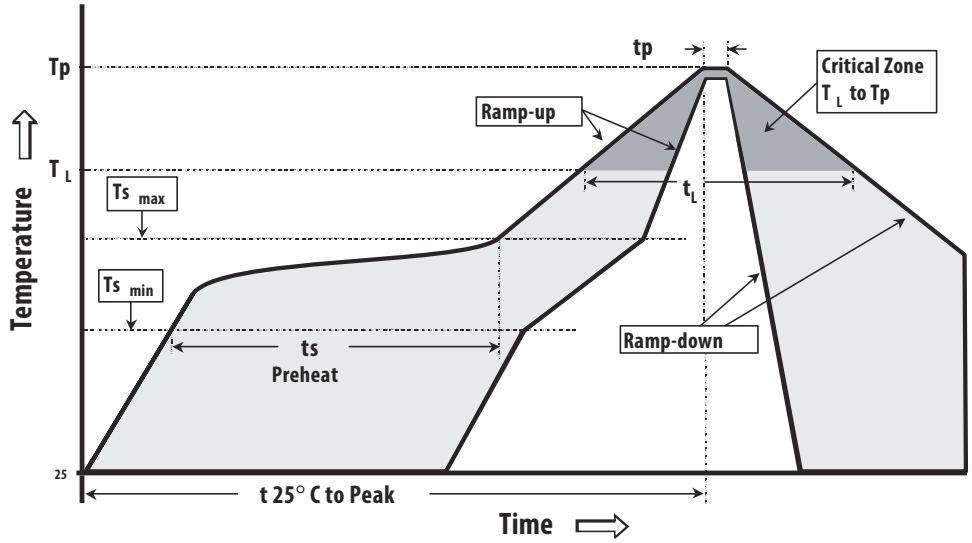


Figure 28. Surface Mount Assembly Profile.

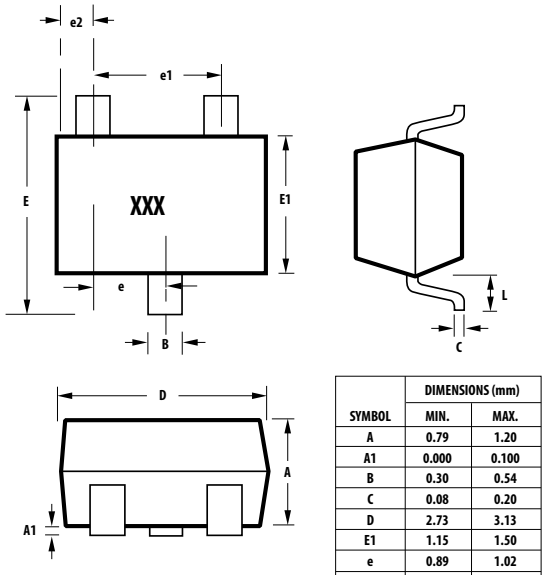
Lead-Free Reflow Profile Recommendation (IPC/JEDEC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature ($T_{S(max)}$ to Peak)		3°C/ second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 seconds
Ts(max) to TL Ramp-up Rate		3°C/second max
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak Temperature (T_P)		260 +0/-5°C
Time within 5 °C of actual Peak temperature (t_P)		20-40 seconds
Ramp-down Rate		6°C/second max
Time 25 °C to Peak Temperature		8 minutes max

Note 1: All temperatures refer to topside of the package, measured on the package body surface

Package Dimensions

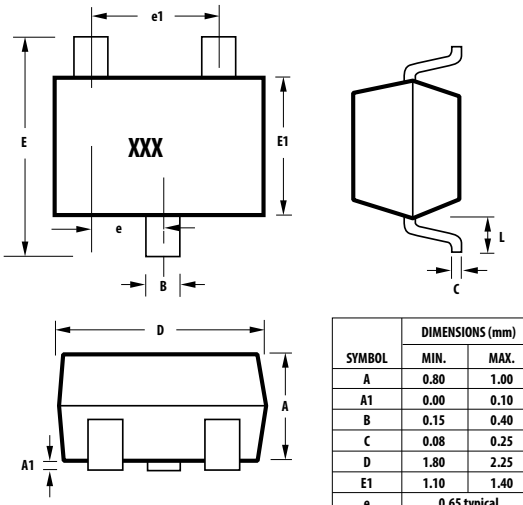
Outline 23 (SOT-23)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

Notes:
XXX-package marking
Drawings are not to scale

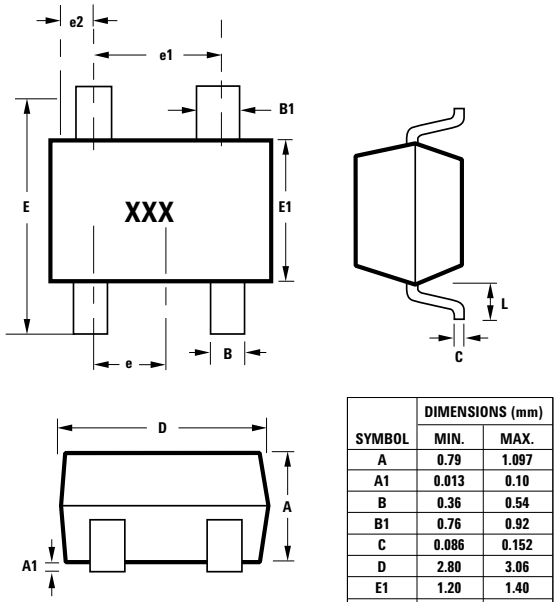
Outline SOT-323 (SC-70 3 Lead)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

Notes:
XXX-package marking
Drawings are not to scale

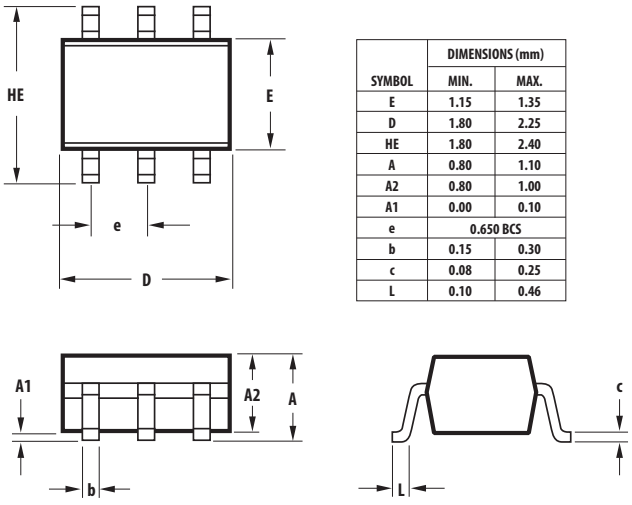
Outline 143 (SOT-143)



SYMBOL	DIMENSIONS (mm) MIN.	MAX.
A	0.79	1.097
A1	0.013	0.10
B	0.36	0.54
B1	0.76	0.92
C	0.086	0.152
D	2.80	3.06
E1	1.20	1.40
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.65
L	0.45	0.69

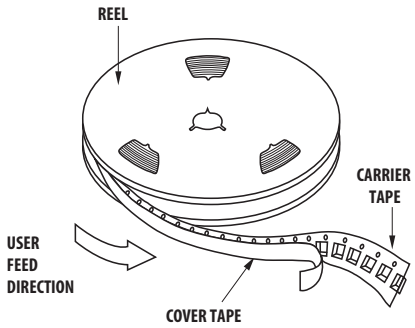
Notes:
XXX-package marking
Drawings are not to scale

Outline SOT-363 (SC-70 6 Lead)

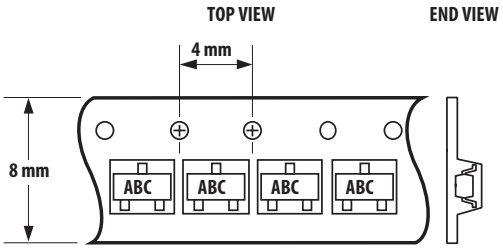


SYMBOL	DIMENSIONS (mm) MIN.	MAX.
E	1.15	1.35
D	1.80	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.650 BCS	
b	0.15	0.30
c	0.08	0.25
L	0.10	0.46

Device Orientation

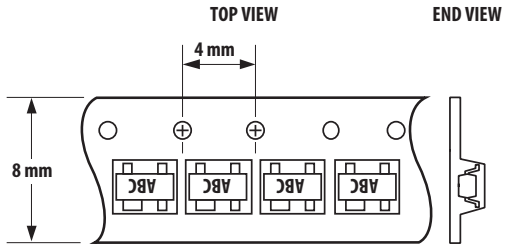


For Outlines SOT-23, -323



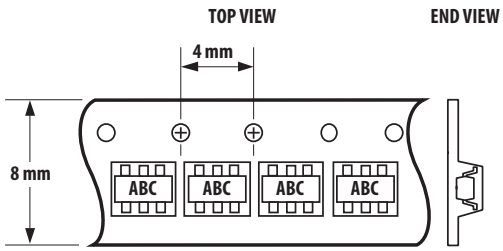
Note: "AB" represents package marking code.
"C" represents date code.

For Outline SOT-143



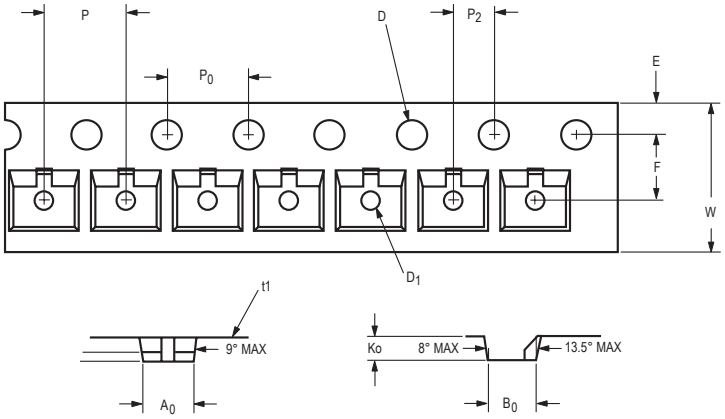
Note: "AB" represents package marking code.
"C" re presents date code.

For Outline SOT-363



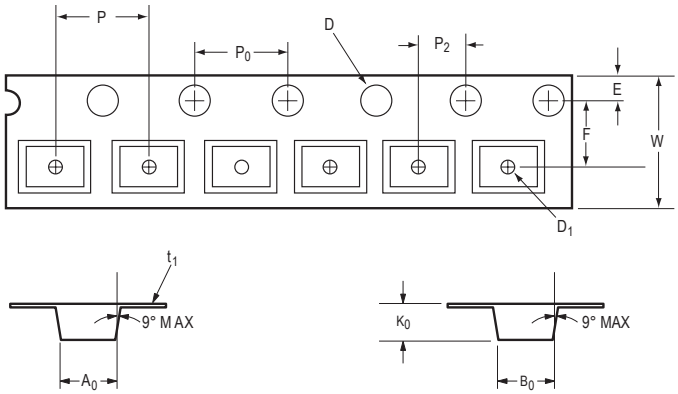
Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation
For Outline SOT-23



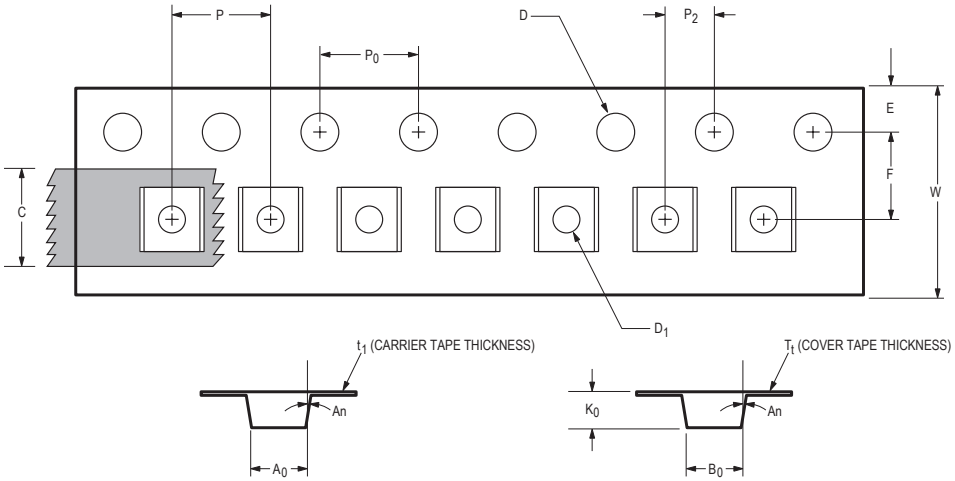
DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 −0.10	0.315 +0.012 −0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

For Outline SOT-143



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.19 ± 0.10	0.126 ± 0.004
	WIDTH	B_0	2.80 ± 0.10	0.110 ± 0.004
	DEPTH	K_0	1.31 ± 0.10	0.052 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 −0.10	0.315+0.012 −0.004
	THICKNESS	t1	0.254 ± 0.013	0.0100 ± 0.0005
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation
For Outlines SOT-323, -363



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8 °C MAX	
	FOR SOT-363 (SC70-6 LEAD)		10 °C MAX	

Part Number Ordering Information

Part Number	No. of Devices	Container
HSMS-282x-TR2G	10000	13" Reel
HSMS-282x-TR1G	3000	7" Reel
HSMS-282x-BLKG	100	antistatic bag

x = 0, 2, 3, 4, 5, 7, 8, 9, B, C, E, F, K, L, M, N, P or R

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-1320EN - November 26, 2014