Contents

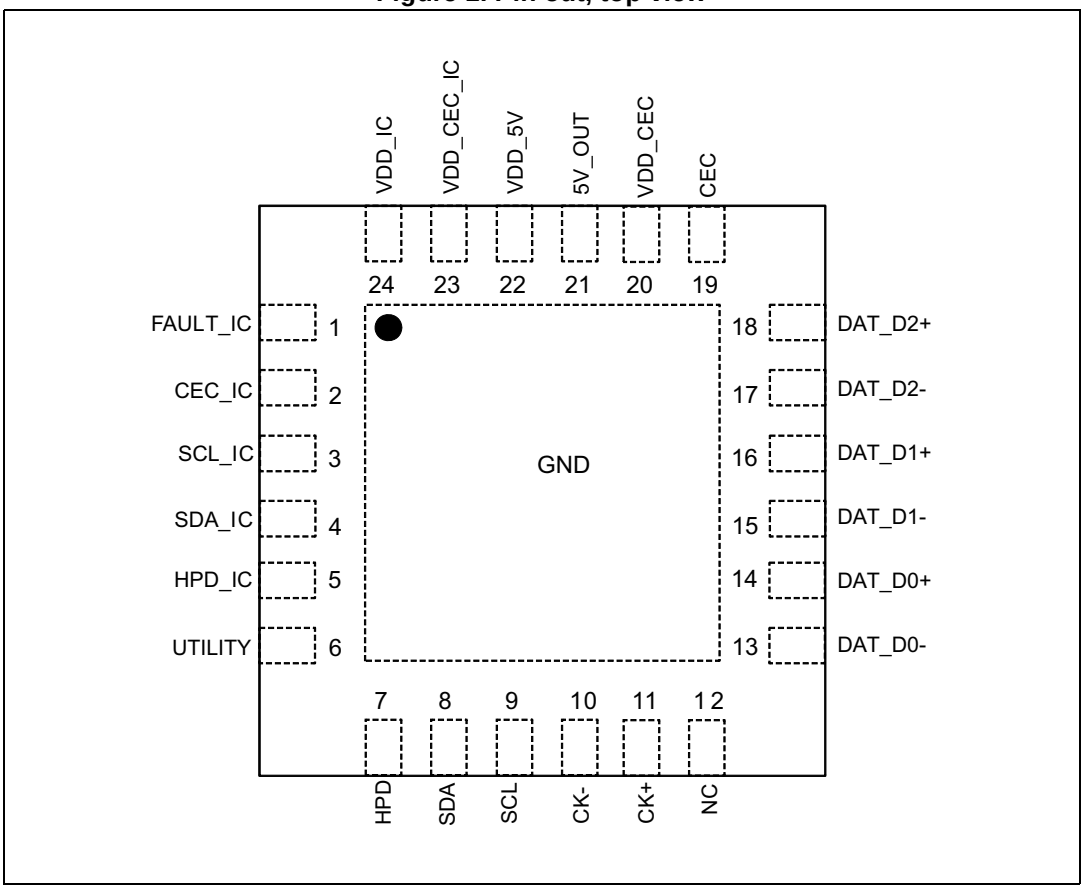
1 Functional description

The HDMI2C1-14HDS is a fully integrated ESD protection and signal conditioning device for control links and TMDS data video channels of HDMI transmitters (Source).

The control stage provides a bidirectional buffer, integrating signal conditioning and dynamic pull-up on DDC bus for maximum system robustness and signal integrity. The HEAC (HDMI Ethernet and Audio return Channels) function is supported, making the component fully compliant with HDMI version. A bidirectional CEC block is integrated, able to wake-up the application from stand-by mode (all power supply off, except the CEC power supply). The integrated TMDS links ESD protection allows a video data rate up to 10.2 Gbps, corresponding to the maximal speed specified by the HDMI standard. All video format specified by HDMI standard (up to 1080p60) are supported, giving maximal flexibility to designers. The +5 V supplied to the cable is protected against accidental surge current and short circuit. All these features are provided in a single 24 leads QFN package saving space on the board.

The HDMI2C1-14HDS is a simple solution that provides HDMI designers with an easy and fast way to reach full compliancy with the stringent HDMI CTS on a wide temperature range.

Figure 1. Pin out, top view



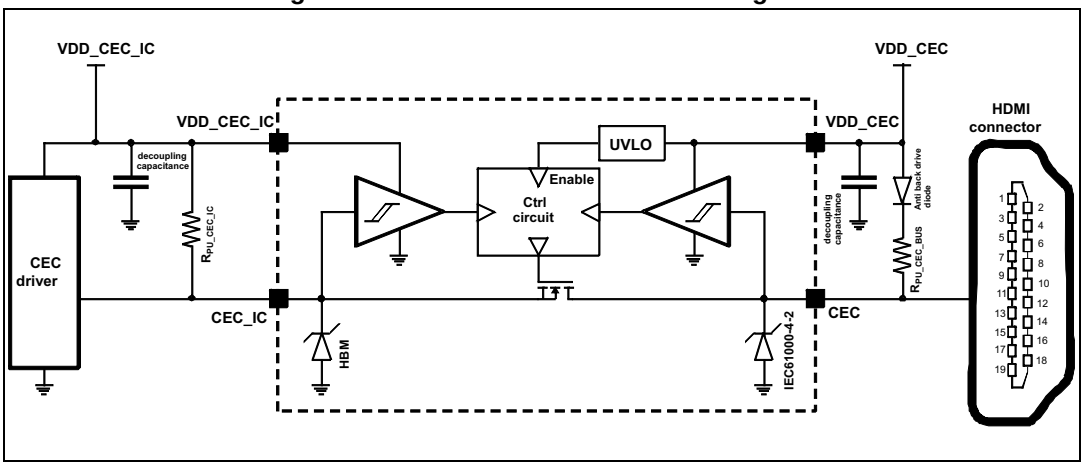
2 Application information

2.1 CEC line description

The CEC bus is described in the HDMI standards as the consumer electronics control. It provides control functions between all the various audiovisual equipment chained in the user's environment.

The CEC block integrated in the HDMI2C1-14HDS implements a level shifter, shifting the cable CEC line from +3.3 V CEC voltage (V_{DD_CEC}) down to the ASIC power supply voltage (V_{DD_IC}) that can be as low as 1.8 V. The *Figure 2* shows the functional diagram of the integrated CEC block.

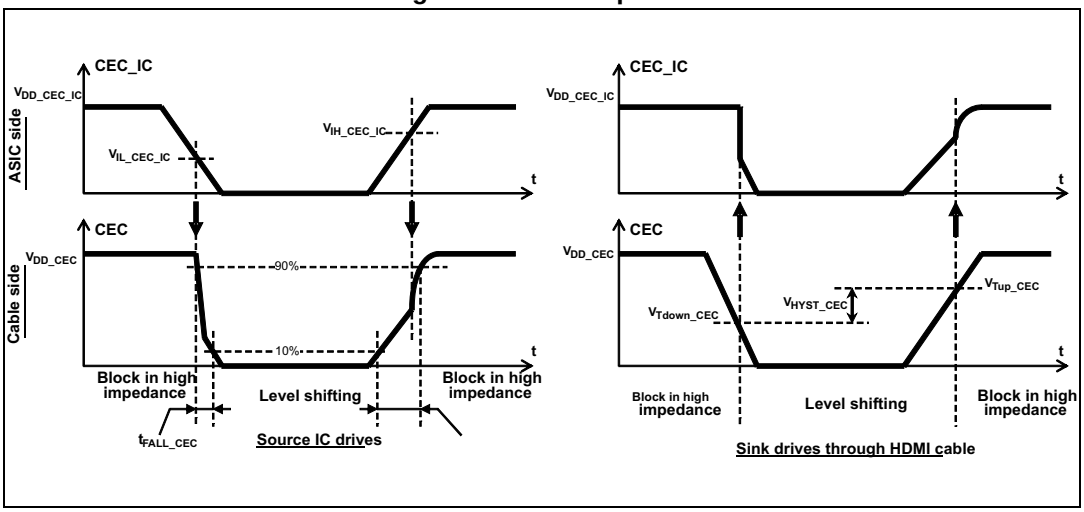
Figure 2. CEC link functional block diagram



In case of no activity on the CEC bus, or if the CEC driver is off (V_{DD_CEC} = 0), the output CEC pin is put in high impedance mode (open circuit) protecting the circuitry and the application against hazardous backdrive.

The *Figure 3* illustrates the normal operating mode of the CEC functional block when either the IC from the source on the sink drives the communication.

Figure 3. CEC simplified



In case the application is set in stand-by mode, the +5 V main supply of the application is generally powered off in order to reduce as much as possible the global power consumption. The CEC driver can be the only device still working in low power mode, allowing a wake up of the whole application through the CEC line. When the main power supply +5 V is switched off, and if the CEC bus is still active (V_{DD_CEC} power in on state), the HDMI2C1-14HDS keeps the CEC bus working properly while all other outputs of the component are put in high impedance mode.

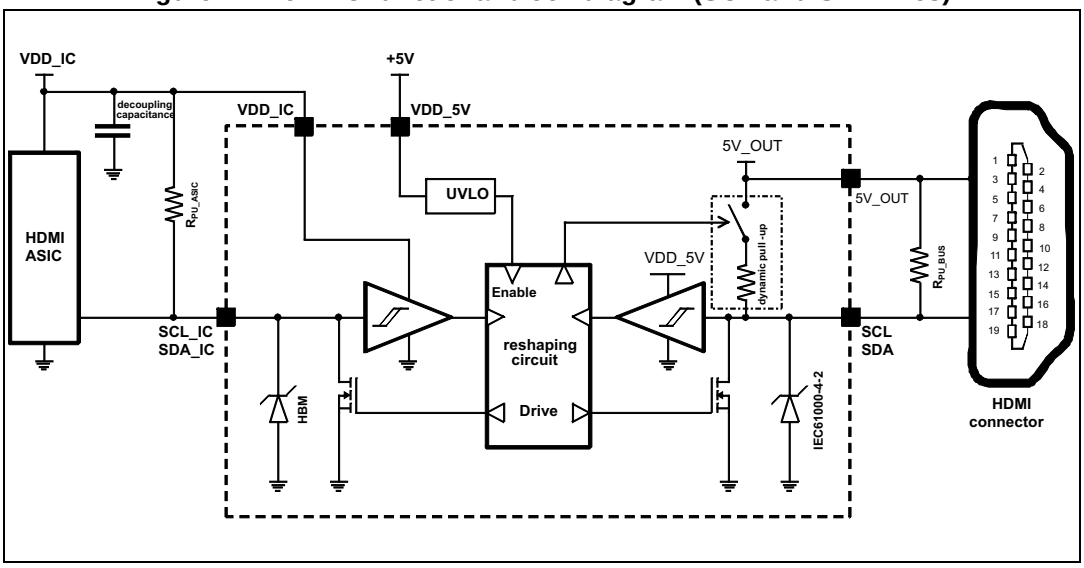
The CEC output (cable side) integrates a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact).

2.2 DDC bus description

The DDC bus is described in the HDMI standards as the Display Data Channel. The topology corresponds to an I2C bus that must be compliant with the I2C bus specification version 2.1 (January 2000). The DDC bus is made of 2 lines: data line (SDA) and clock line (SCL). It is used to create a point to point communication link from the Source to the Sink. EEDID and HDCP protocols are especially flowing through this link, making this I2C communication channel a key element in the HDMI application.

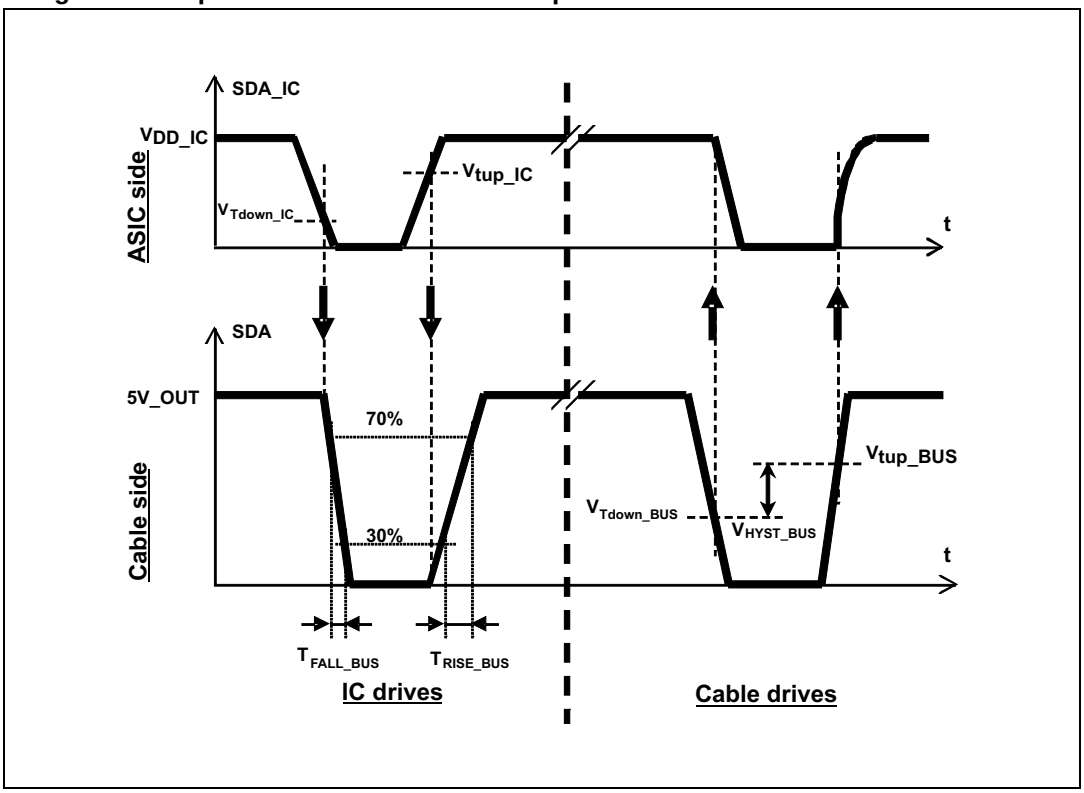
The DDC block integrated in the HDMI2C1-14HDS allows a bidirectional communication between the cable and the ASIC. It is fully compliant with the HDMI standard and its CTS, and with the I2C bus specification version 2.1. It is shifting the 5 V voltage from the cable (V_{5V_OUT}) down to the ASIC voltage level (V_{DD_IC}) that can be as low as 1.8 V. The *Figure 4* shows the functional diagram of the DDC block integrated in the HDMI2C1-14HDS device.

Figure 4. The DDC functional block diagram (SCL and SDA lines)



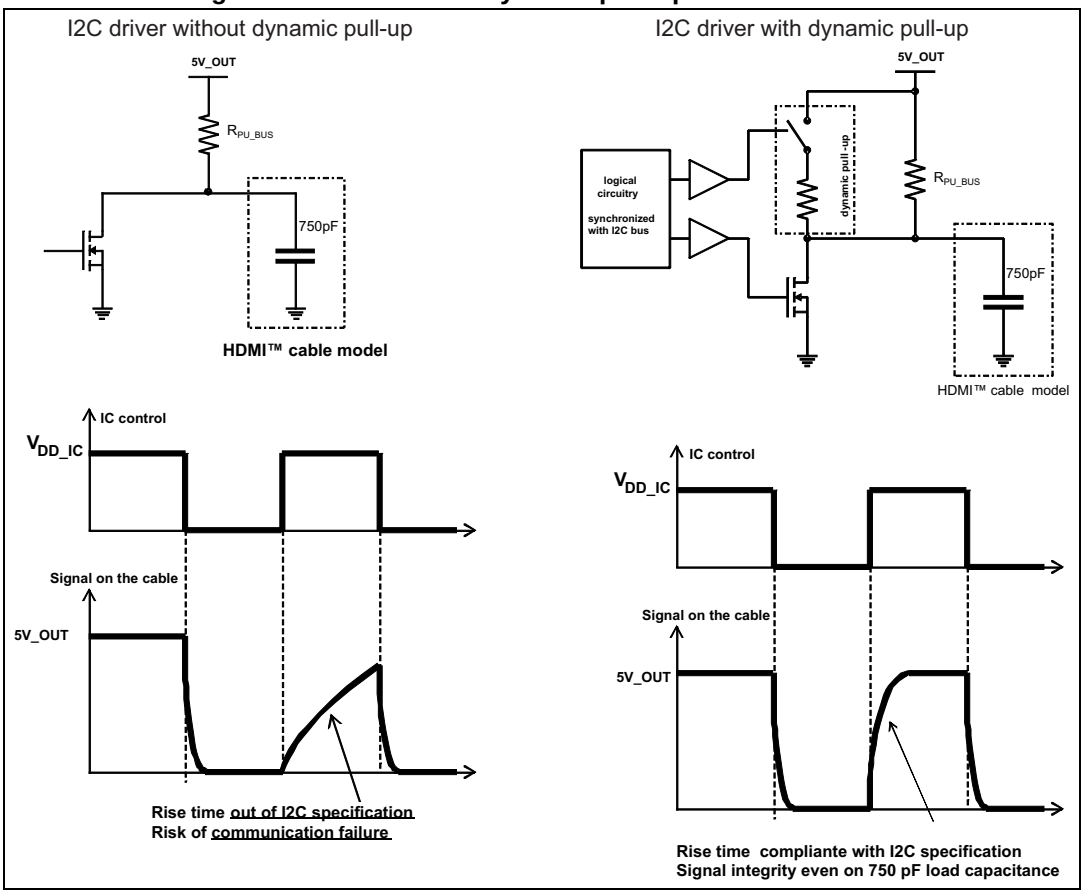
The *Figure 5* illustrates the electrical parameters of the DDC block specified in *Table 8*.

Figure 5. Simplified view of the electrical parameters of the DDC functional block



The HDMI standard specifies that the max capacitance of the cable can reach up to 700 pF. Knowing that the max capacitance of the sink input can reach up to 50 pF, this means that the I2C driver must be able to drive a load capacitance up to 750 pF. On the other hand, the I2C standard specifies a maximum rise time of the signal must be lower than 1 µs in order to keep the signal integrity. Taking into account the max cable capacitance of 750 pF, it is not possible to guarantee a rise time lower than 1 µs in worst case. Therefore, a dynamic pull-up has been integrated at the output of SDA and SCL lines and synchronized with the I2C driver. This signal booster accelerates for a short period the charging time of the equivalent cable capacitance, allowing driving any HDMI cable. The *Figure 6* illustrates the benefit of the dynamic pull-up integrated in the HDMI2C1-14HDS device.

Figure 6. Benefit of the dynamic pull-up on the DDC bus



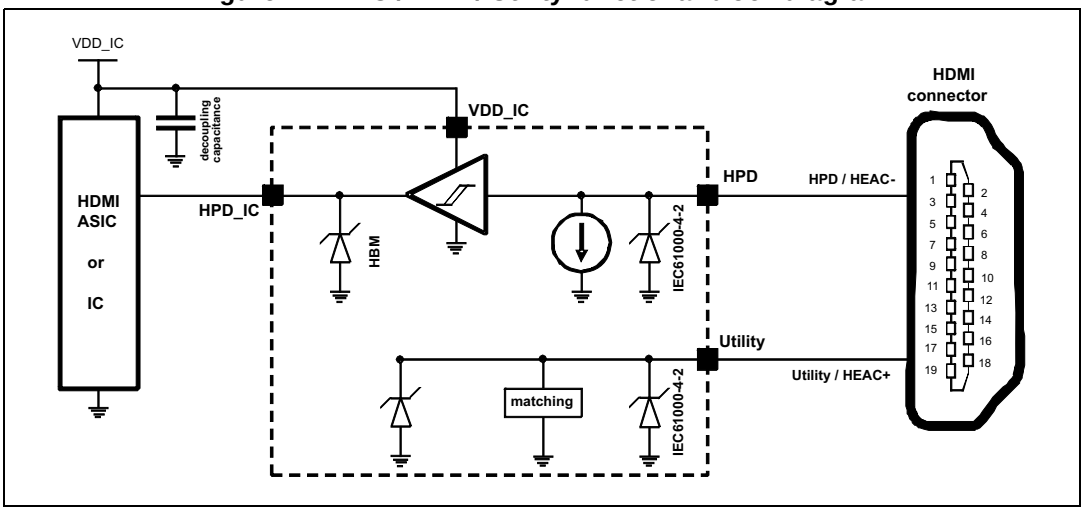
In order to activate the DDC lines, the V_{DD_5V} has to reach the V_{DD_ON} threshold (see *Table 4*). The inputs and outputs of the bidirectional level shifters (SDA, SCL, SDA_IC, SCL_IC) must be set to a high level after the power-on, and the HPD line has to be activated on time.

The DDC outputs (SCL and SDA on cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8kV contact).

2.3 HEAC link and HPD line description

The HDMI2C1-14HDS proposes a unique solution in order to manage and protect both the HEAC and the HPD links. The *Figure 7* shows an overview of the function diagram of the integrated block.

Figure 7. HEAC / HPD / Utility functional block diagram



This block simplifies the design and the PCB layout of the HPD and HEAC functions.

Both HPD and Utility inputs (cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact).

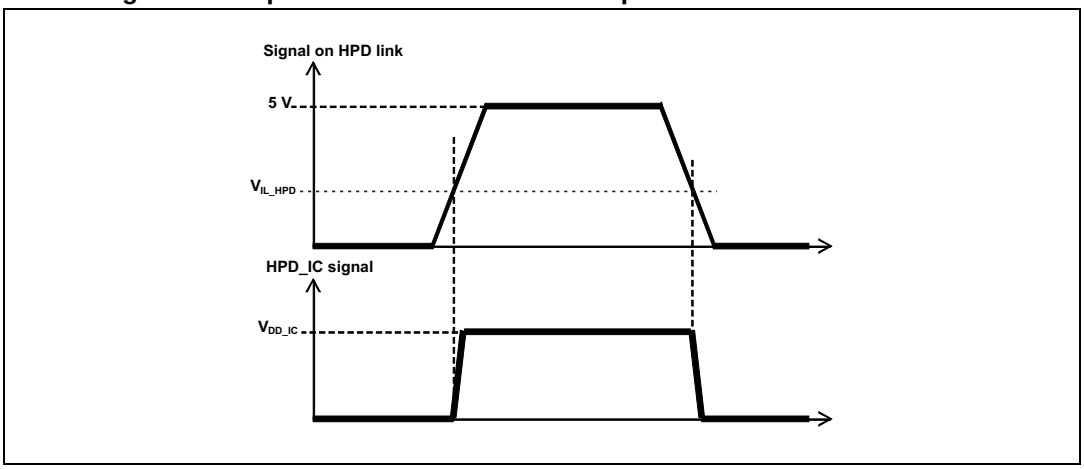
2.3.1 HPD line description

The HPD line is described in the HDMI standard as the hot plug detect function. This line is used by the source device in order to detect if a sink device is connected through an HDMI cable.

The integrated HPD block is pulling down the line via a current source. When the input voltage is detected to be higher than a threshold level V_{TH_HPD}, the signal is converted into a high state level on the ASIC side, at the voltage level of the ASIC power supply V_{DD_IC}. Otherwise, CEC_IC pin remains in low state.

The electrical parameters relevant to the HPD block and specified by the*Table 7* are illustrated in the *Figure 8*.

Figure 8. Simplified view of the electrical parameters of the HPD block



2.3.2 HEAC link

The HEAC link is described in the HDMI 1.4 standards as the HDMI ethernet and audio return channel. It corresponds physically to one differential wired pair made of the Utility line and the HPD line. Two signals are transmitted through this link.

The first signal corresponds to the HDMI ethernet channel (HEC). The signal is transmitted in differential mode (bidirectional) through the HEAC link. It is specified by the 100Base-TX IEEE 802.3 standard (fast ethernet 100Mbps over twisted pair). Therefore, the HEC integrates an ethernet link into the video cable, enabling IP-based applications over the HDMI cable.

The second signal corresponds to the audio return channel (ARC). The signal is transmitted in common mode (unidirectional, from sink to source) through the HEAC link. It is specified by the IEC 60958-1 standard. The ARC function integrates an upstream audio capability, simplifying the cabling of the audiovisual equipment. It is no more necessary to use a coaxial cable from TV to audio amplifier.

The HDMI2C1-14HDS helps the designer to implement this high added value HEAC function in the application, protecting the link against the ESD with no disturbance of the signal.

2.4 +5V protection and fault line

The +5 V power supply that the source device has to provide to the HDMI cable is described by the HDMI standard. It must be protected against accidental short circuit that could occur on the cable side.

The HDMI2C1-14HDS device embeds a low drop current limiter. If an overcurrent is detected, the HDMI2C1-14HDS limits the current through the +5 V power supply. If the current is too high (short circuit), the device opens the +5 V.

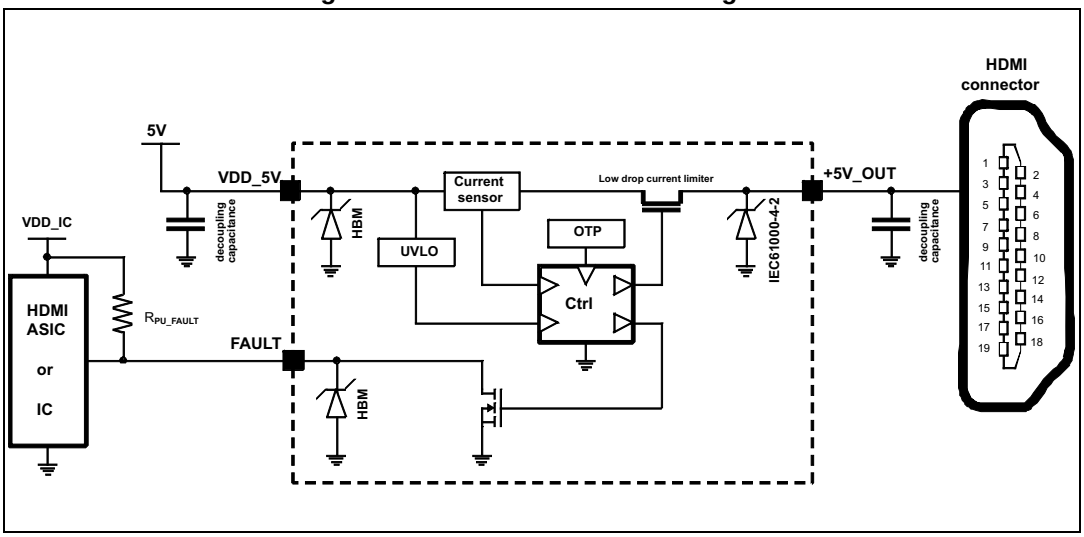
Furthermore, the HDMI2C1-14HDS device embeds also an over temperature protection (OTP). If the internal temperature of the device is reaching a too high value, the +5 V supply is even opened in order to protect the application.

In case either the current limiter or the OTP is triggered, the fault pin switches down to a low state level (open drain topology) in order to inform the HDMI ASIC that an abnormal situation has been detected (option).

An under voltage lockout (UVLO) is also integrated in the block. It checks the main +5 V power supply state, and enable the +5V_OUT only if the main power supply has reach a minimal value $V_{DD\_5V\_ON}$.

The *Figure 9* shows the functional diagram of the current limiter block.

Figure 9. +5V functional block diagram



To summarize, the short circuit protection and the over temperature protection features are providing a high robustness level of the application. On top of this, the fault line feature can be used in order to improve the user experience.

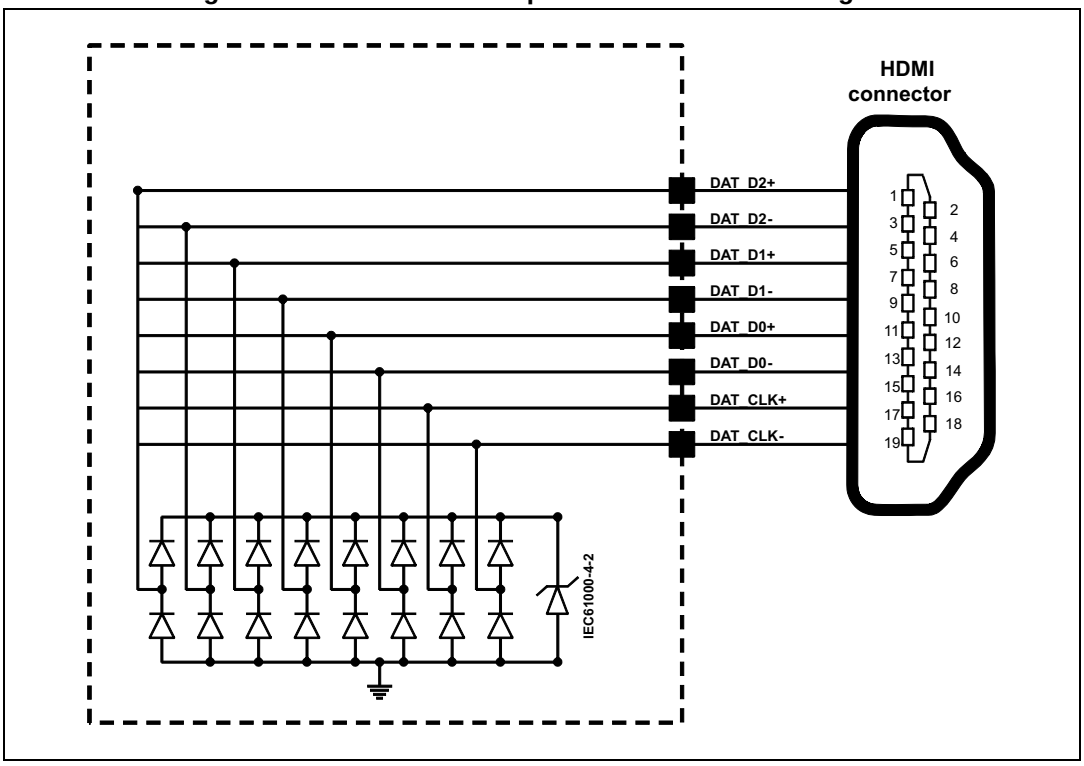
The 5V_OUT pin integrates a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact). The decoupling capacitance is mandatory, according to the power management state of the art.

2.5 TMDS channels

The TMDS (Transient Minimized Differential Signaling) channels are described by the HDMI standard. A total of 4 unidirectional differential pairs are used to transmit the video data to the Sink device. There are 3 channels dedicated to the video data, and 1 channel dedicated to the clock. The frequency of the TMDS clock is 1/10 of the video data frequency.

The HDMI2C1-14HDS provides a simple PCB layout solution, directly compliant with HDMI connector type A. It protects the application against the ESD according the IEC61000-4-2 level 4 standard (+/-8 kV contact). The high bandwidth of this ESD protection allows to transmit HD video data with no disturbance of the signal up to 3.4Gbps per channel.

Figure 10. TMDS lines ESD protection functional diagram



2.6 Application block diagrams

The *Figure 11* shows an application block diagram proposal implementing all the possible options. The diagram shows that the CEC driver can be totally independent from the HDMI ASIC. By this way, even if the +5 V power supply and/or if the HDMI ASIC is sleeping in stand-by mode, the CEC bus is still active in low power mode. By this way, the designer has then the tools to optimize the power consumption of the global application in stand-by mode, and in the same time, has the possibility to implement a smart wake-up through the CEC bus enhancing the final user experience.

Figure 11. Application block diagram

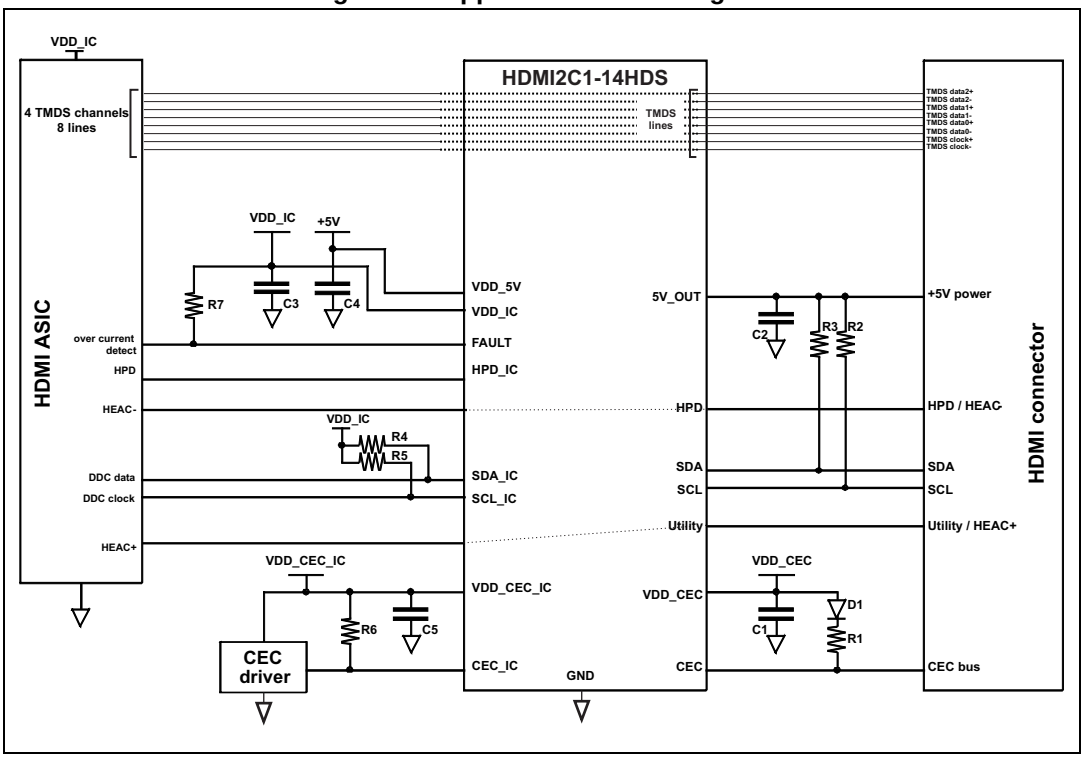


Table 1. Block diagrams references

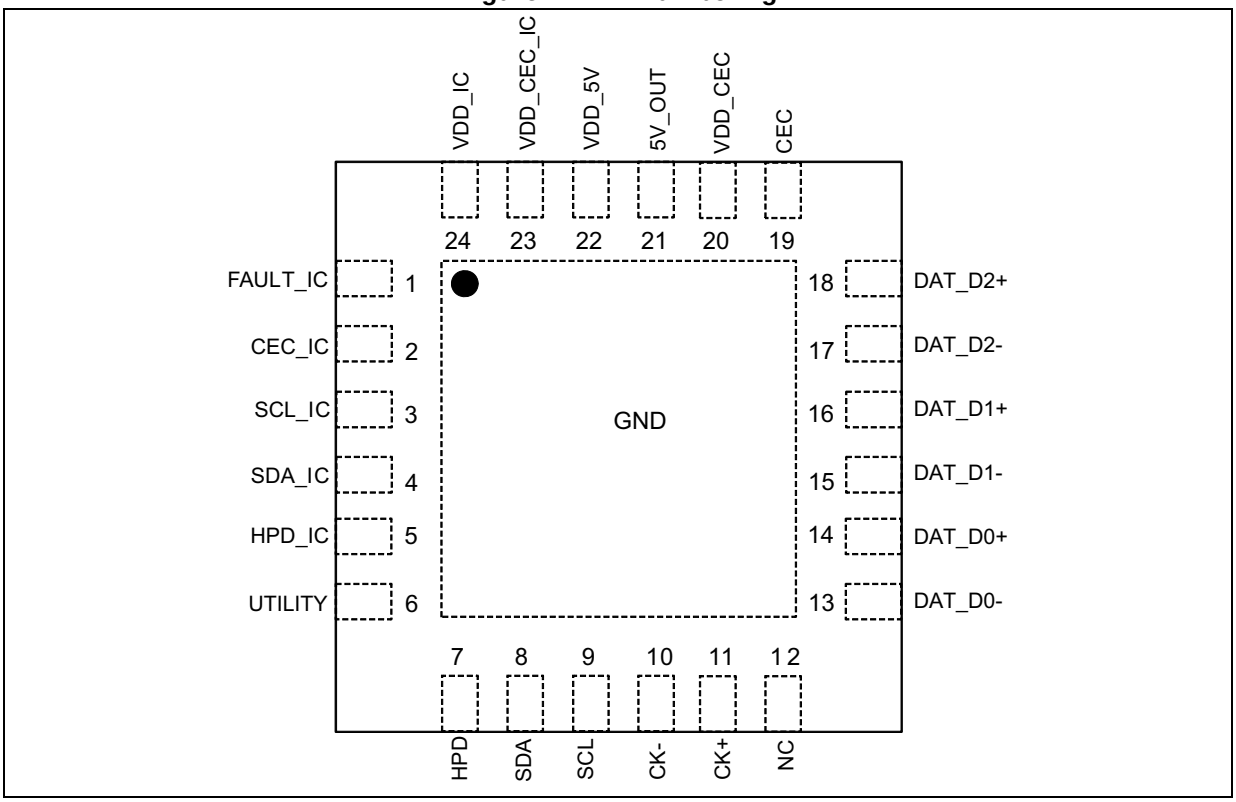
Ref.	Typical values	Comment
R1	27 kΩ	Pull-up resistance on CEC bus, specified by the HDMI standard
R2, R3	1.8 kΩ	Pull-up resistances on DDC bus, specified by the HDMI standard
R4, R5	10 kΩ	Pull-up resistance on DDC bus, ASIC side, value selected to be compliant with I2C levels
R6	270 kΩ to 1 MΩ	Pull-up resistance on CEC line, ASIC side
R7	10 kΩ	Pull-up resistance on FAULT line (option)
D1	BAT54	Small schottky diode blocking backdrive current flowing toward the V_{DD_CEC} supply
C1 to C5	100 nF	Decoupling capacitance on power supplies

Note: SCL_IC, SDA_IC, and CEC_IC have to be driven with an ASIC working with open drain outputs.

Table 2. Pin description

Pin	Name	Description	Pin	Name	Description
1	FAULT_IC	Fault line output ASIC side	13	DAT_D0-	TMDS data D0-
2	CEC_IC	CEC output ASIC side	14	DAT_D0+	TMDS data D0+
3	SCL_IC	DDC output ASIC side	15	DAT_D1-	TMDS data D1-
4	SDA_IC	SDA output ASIC side	16	DAT_D1+	TMDS data D1+
5	HPD_IC	HPD output ASIC side	17	DAT_D2-	TMDS data D2-
6	Utility	Utility/HEAC+ input HDMI cable side	18	DAT_D2+	TMDS data D2+
7	HPD	HPD/HEAC- input HDMI cable side	19	CEC	CEC output HDMI cable side
8	SDA	DDC output HDMI cable side	20	VDD_CEC	CEC supply HDMI cable side
9	SCL	DDC output HDMI cable side	21	5V_OUT	+5 V power supply HDMI cable side
10	CK-	TMDS CK+	22	VDD_5V	+5 V main power supply
11	CK+	TMDS CK-	23	VDD_CEC_IC	CEC supply ASIC side
12	NC	None connected	24	VDD_IC	HDMI ASIC power supply

Figure 12. Pin numbering



3 Electrical characteristics

Table 3. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value	Unit
V_{pp_BUS}	ESD discharge on HDMI cable side (pin 6 to 11, pin 13 to 19 and pin 21), IEC 61000-4-2 level 4	Contact discharge	±8(1)	kV
V_{pp_IC}	ESD discharge (all pins), HBM JESD22-A114D level 2	Contact discharge	±2	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_{op}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature		260	°C
V_{DD_5V} V_{DD_IC} V_{DD_CEC} $V_{DD\_CEC\_IC}$	Supply voltages		6	V
Inputs	Logical input min/max voltage range		-0.3 to 6	V

1. With a 100 nF capacitor connected to the 5V_OUT pin.

Table 4. Power supply characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD_CEC}	CEC supply voltage, bus side		2.97	3.3	3.63	V
$V_{DD\_CEC\_IC}$	CEC supply voltage, IC side		1.62		3.63	V
V_{DD_IC}	Low-voltage ASIC supply voltage		1.62		3.63	V
V_{DD_5V}	5 V input supply voltage range		4.9	5.0	5.3	V
$V_{DD\_5V\_ON}$(1)	+5 V power on reset		3.5	3.8	4.1	V
$V_{DD\_CEC\_ON}$	CEC power on reset		2.6	2.8	2.95	V
I_{QS_5V}	Quiescent currents on V_{DD_5V}, V_{DD_IC}, V_{DD_CEC}, $V_{DD\_CEC\_IC}$	V_{DD_5V} = 5V, V_{DD_IC} = 1.8V, V_{DD_CEC} = 3.3V $V_{DD\_CEC\_IC}$ = 1.8V Idle-state on CEC and DDC links, HPD and 5V_OUT links open			600	µA
I_{QS_IC}					75	
I_{QS_CEC}					200	
$I_{QS\_CEC\_IC}$					40	
Rth	Junction to ambient thermal resistance	Copper heatsink as shown by *Figure 18*		75		°C/W
T_{SD}	Thermal Shutdown threshold		120		150	°C
P_{TOTAL_SB}	Standby conditions	V_{DD_5V} = V_{DD_IC} = 0V V_{DD_CEC} = 3.3V $V_{DD\_CEC\_IC}$ = 3.3V			0.8	mW

1. In order to activate the DDC functional block, the 3 following conditions have to be met:

- V_{DD_5V} has to reach the V_{DD_ON} threshold
- The inputs and outputs of the bidirectional level shifter must be set to a high level after the power-on
- The HPD line has to be activated one time

Table 5. CEC electrical characteristics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{Tup_CEC}	Upward input voltage threshold on bus side				2.0	V
V_{Tdown_CEC}	Downward input voltage threshold on bus side		0.8			V
V_{HYST_CEC}	Input hysteresis on bus side			0.4		V
T_{RISE_CEC}	Output rise-time (10% to 90%)	RUP_CEC = 14.1 k Ω(2)			250	µs
T_{FALL_CEC}	Output fall-time (90% to 10%)	C_{CEC_CABLE} = 7.9 nF(2)			50	µs
I_{OFF_CEC}	Leakage current in powered-off state	V_{DD_5V} = 0 V V_{DD_IC} = 0 V, V_{DD_CEC} = 3.3 V			1.8	µA
$V_{IL\_CEC\_IC}$	Input low level on IC side		0.5			V
$V_{IH\_CEC\_IC}$	Input high level on IC side	$V_{IH\_CEC\_IC}$ = 1.8 V			1.5	V
		$V_{IH\_CEC\_IC}$ = 3.3 V			1.9	
R_{ON_CEC}	On resistance across CEC and CEC_IC pins	CEC pin to 0 V			100	Ω
C_{IN_CEC}	Input capacitance on CEC link	V_{DD_5V} = 0 V V_{DD_CEC} = 0 V V_{DD_IC} = 0 V V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		25	30(3)	pF

1. T_{amb} = 25 °C, V_{DD_CEC} = 3.3 V, $V_{DD\_CEC\_IC}$ = 1.8 V, unless otherwise specified
2. Test conditions are compliant with worst case CEC specification:

- pull up resistance 2 times 27 k Ω +5% in parallel
- Max capacitance corresponding to 9 equipment chained on the CEC bus

3. Maximum capacitance allowed at connector output is 200 pF in HDMI specification

Table 6. HDMI 5V_out current limiter electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DROP}	Drop-out voltage	I_{5V_OUT} = 55 mA	20	50	95(2)	mV
I_{5V_OUT}	Output current(3)	V_{5V_OUT} = 0 V	55		115	mA
V_{L_FAULT}	Low level on FAULT pin	R_{PU_FAULT} = 10 k Ω			0.3	V

1. T_{amb} = 25°C, V_{DD_5V} = 5 V, unless otherwise specified
2. HDMI specification requires a maximum of 100 mV voltage-drop
3. Maximum allowed output current is 500 mA when a sink is powered off in HDMI specification

Table 7. HPD, HEAC, and utility line electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{PULL_DOWN}	Pull-down current in HPD block			15	25	µA
V_{TH_HPD}	HPD input threshold level		1.0		1.7	V
C_{IN_HPD} $C_{IN\_UTILITY}$	Input capacitance	V_{DD_5V} = 0 V, V_{BIAS} = 0 V f = 1 MHz, V_{OSC} = 30 mV		21	25	pF
f_{CUT_HEAC}	Cut-off frequency of HEAC bus			500		MHz

1. Tamb = 25°C, V_{DD_5V} = 5 V, unless otherwise specified.

Table 8. DDC bus (SDA and SCL lines) electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side				3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side		1.5			V
V_{HYST_BUS}	Input hysteresis on bus side		1.0		1.3	V
V_{OL_BUS}	Output low level	Current sunk by SDA and SCL pin is 3 mA			0.35	V
T_{RISE_BUS}	Output rise-time (30% to 70%)	C_{BUS} = 750 pF(2) R_{UP} = 2 K Ω //47 K Ω + 10%(3)			500	ns
T_{FALL_BUS}	Output fall-time (30% to 70%)				50	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55	60	65	$\%V_{DD\_IC}$
V_{Tdown_IC}	Downward input voltage thresholds IC side		35	40	45	$\%V_{DD\_IC}$
V_{OL_IC}	Output low level on IC side	Current sunk by SDA_IC or SCL_IC pins is 500 µA			20	$\%V_{DD\_IC}$
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V V_{DD_IC} = 0 V V_{DD_CEC} = 0 V V_{BIAS} = 0 V, f = 1 MHz V_{OSC} = 30 mV		27	32(4)	pF

1. T_{amb} = 25 °C, V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified
2. Maximum load capacitance allowed on I2C entire link (cable + connector) is 750 pF in HDMI specification.
3. Two pull-up resistors in parallel (sink + source). Typical value is 47 k Ω and maximum value is 47 k Ω + 10% in HDMI specification.
4. Maximum capacitance allowed at connector output is 50 pF in HDMI specification

Table 9. TMDS links electrical characteristics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{CUT_TMDS}	Bandwidth at -3 dB	Single ended mode		8.7(2)		GHz
		Differential mode		6		
V_{BR}	Breakdown voltage	I_{RM} = 1 mA	4.5			V
I_{RM}	Leakage current	V_{RM} = 3.3 V			100	nA
C_{I/O_GND}	Capacitance I/O to ground	$V_{I/O}$ = 0 V, f = 1 MHz, V_{OSC} = 30 mV		0.6	1.0	pF
$C_{I/O\_I/O}$	Capacitance I/O to I/O	$V_{I/O}$ = 0 V, f = 1 MHz, V_{OSC} = 30 mV		0.3		pF
Z_{DIFF}	Differential impedance	tr = 200 ps (10%-90%) $Z0_{DIFF}$ = 100 Ω	85	100	115	Ω

1. T_{amb} = 25 °C, V_{DD_CEC} = 3.3 V, $V_{DD\_CEC\_IC}$ = 1.8 V, unless otherwise specified
2. The bandwidth is enough large to operate up to 340 MHz for HDMI clock frequency (10.2Gbps total data rate)

Figure 13. CEC typical waveforms (IC to cable communication)

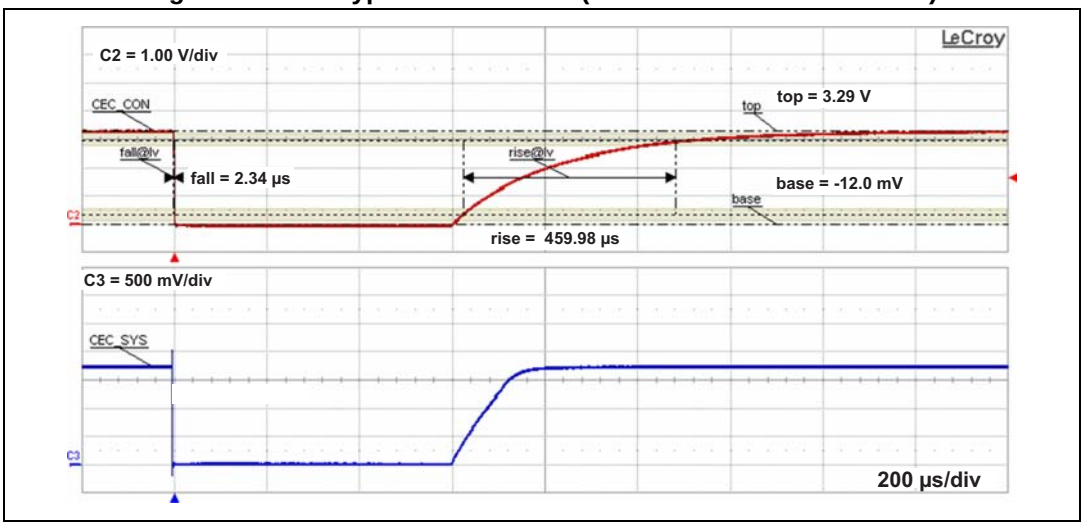


Figure 14. CEC typical waveforms (cable to IC communication)

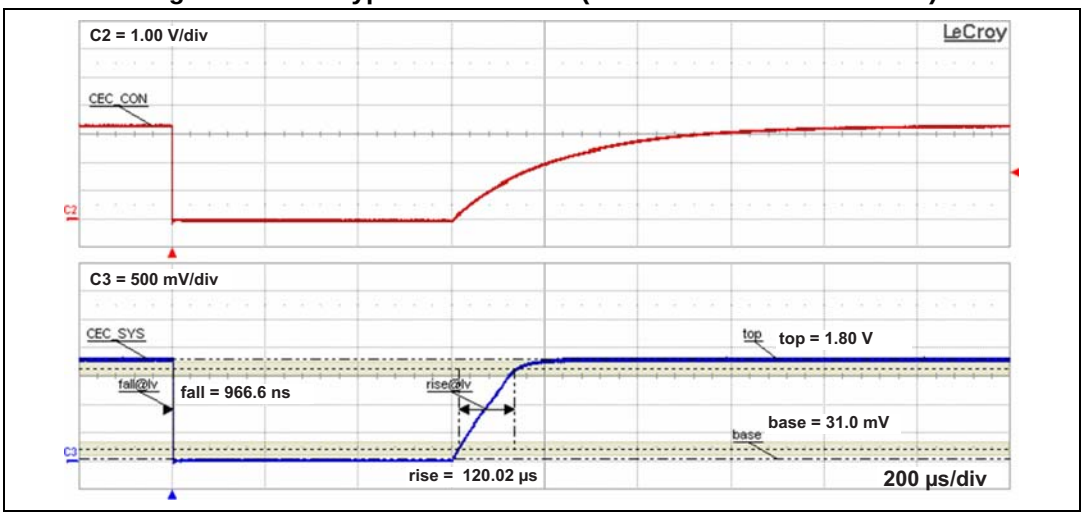


Figure 15. DDC typical waveforms (IC to cable communication)

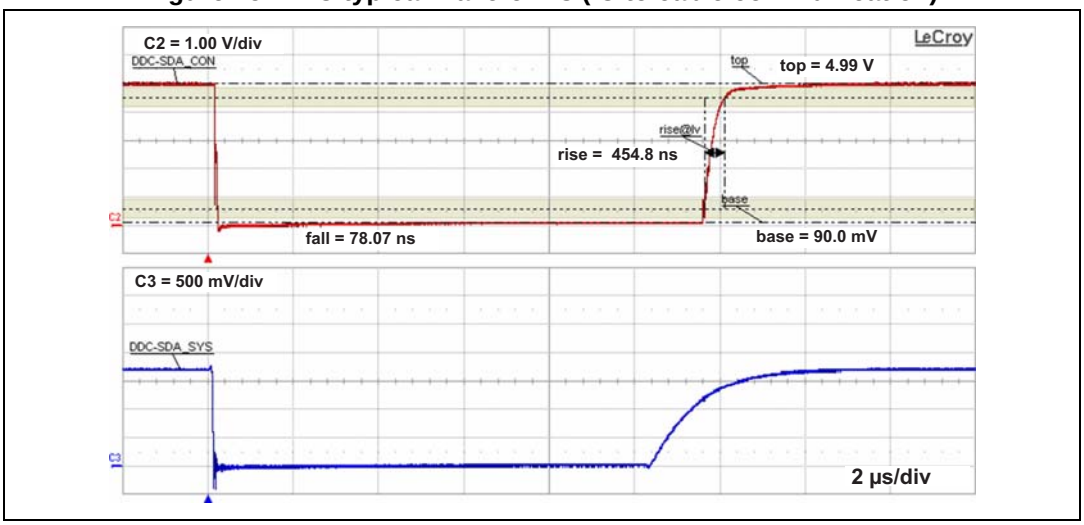


Figure 16. DDC typical waveforms (cable to IC communication)

Figure 17. HPD typical waveforms (timing)

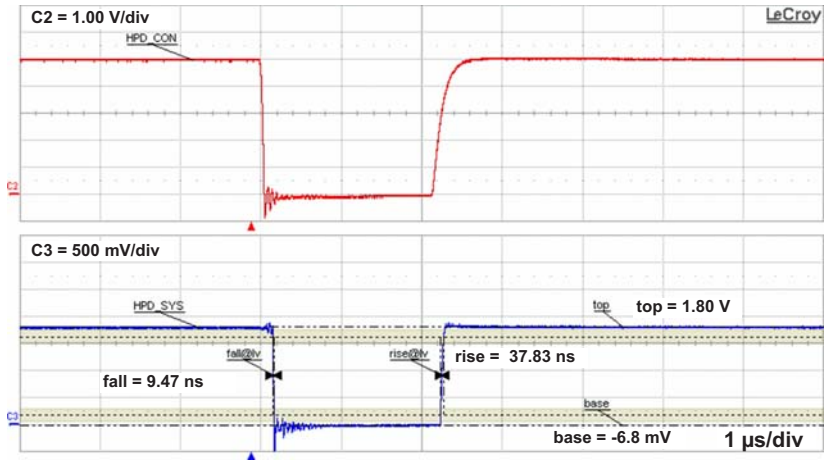


Figure 18. HEAC single ended mode typical bandwidth

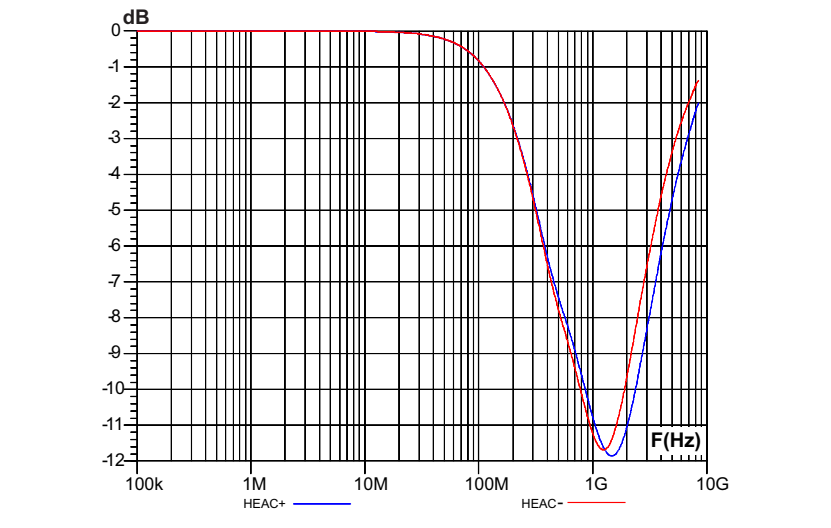


Figure 19. TMDS line S_{21} frequency response

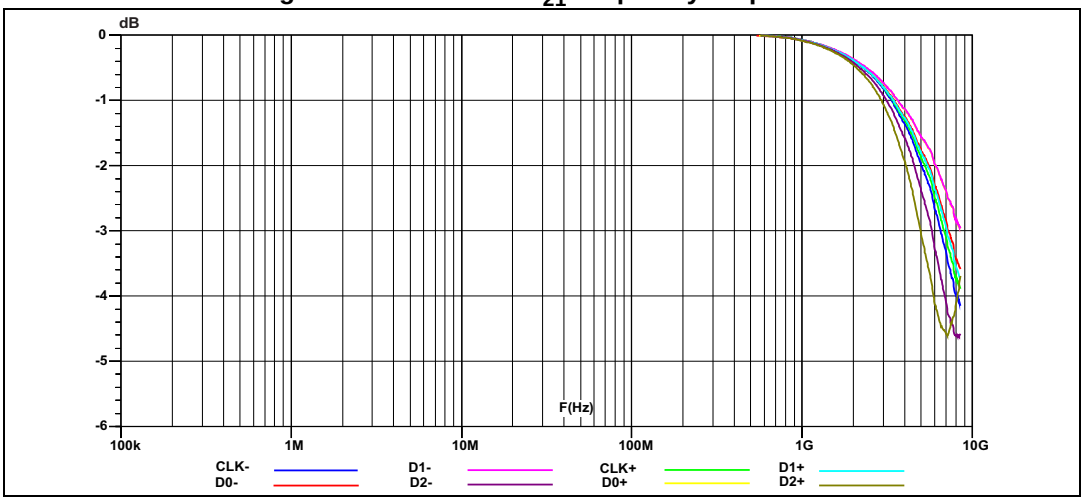


Figure 20. TDR of TMDS lines

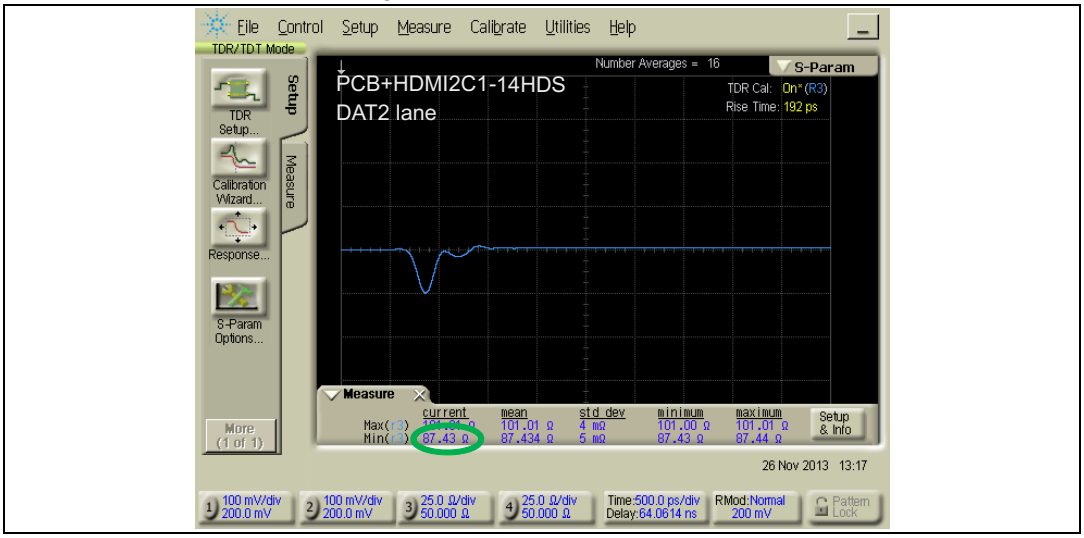


Figure 21. Eye diagram of TMDS line: D0, D1, D2 and CLK lanes at 3.35Gbps

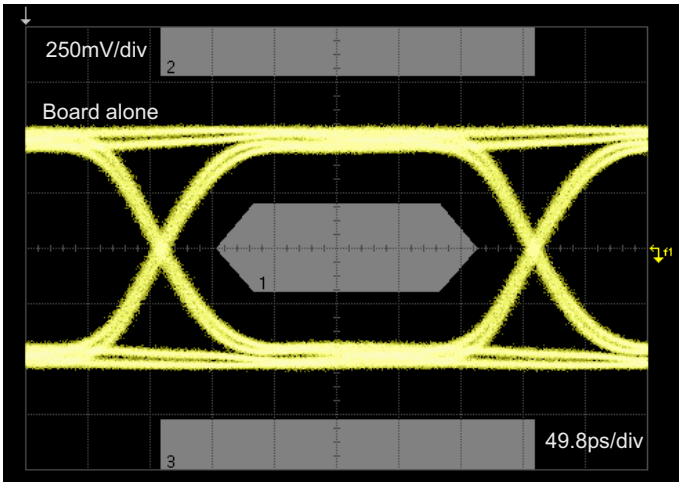


Figure 22. Eye diagram of TMDS line: D0, D1, D2 and CLK lanes at 3.35Gbps

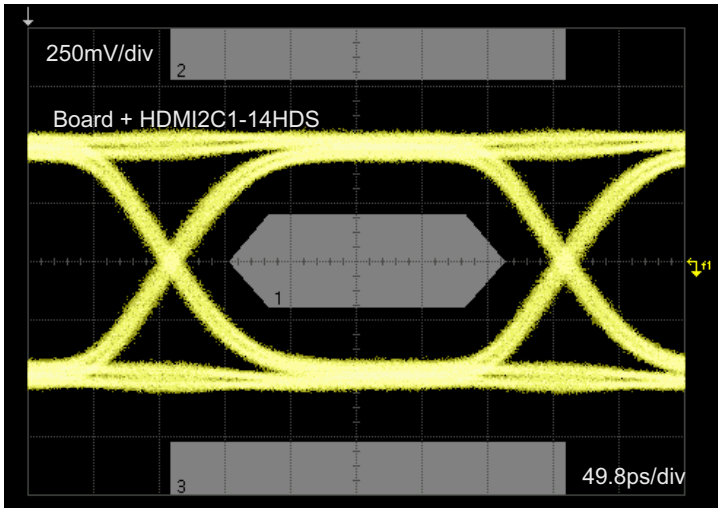


Figure 23. TMDS line: remaining voltage when positive 8 kV ESD applies

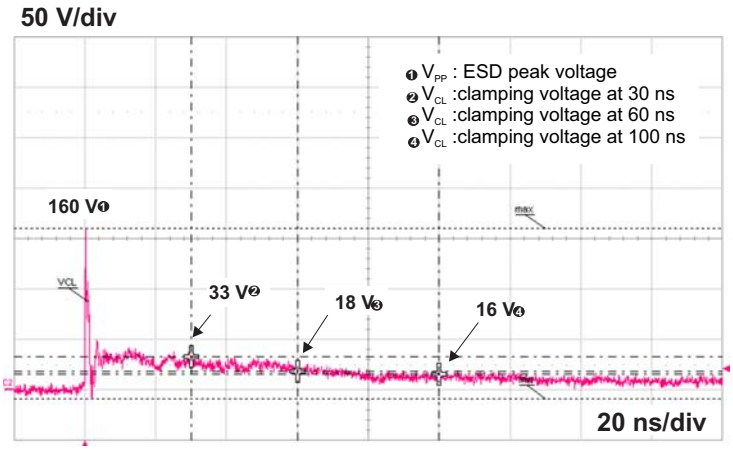
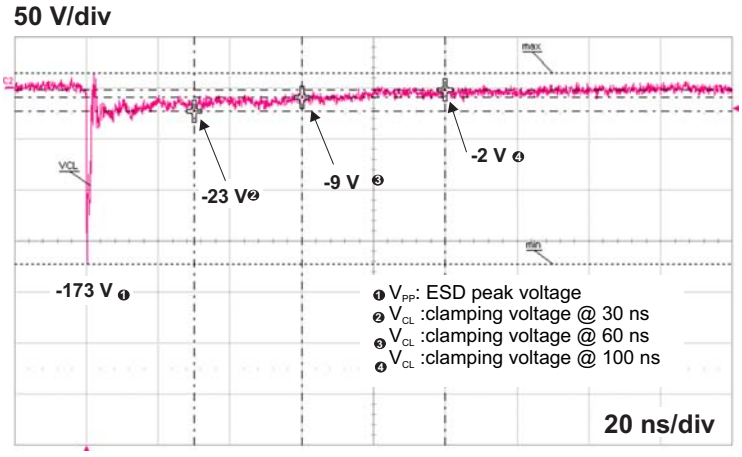


Figure 24. TMDS line: remaining voltage when negative ESD applies



4 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 QFN package information

Figure 25. QFN package outline

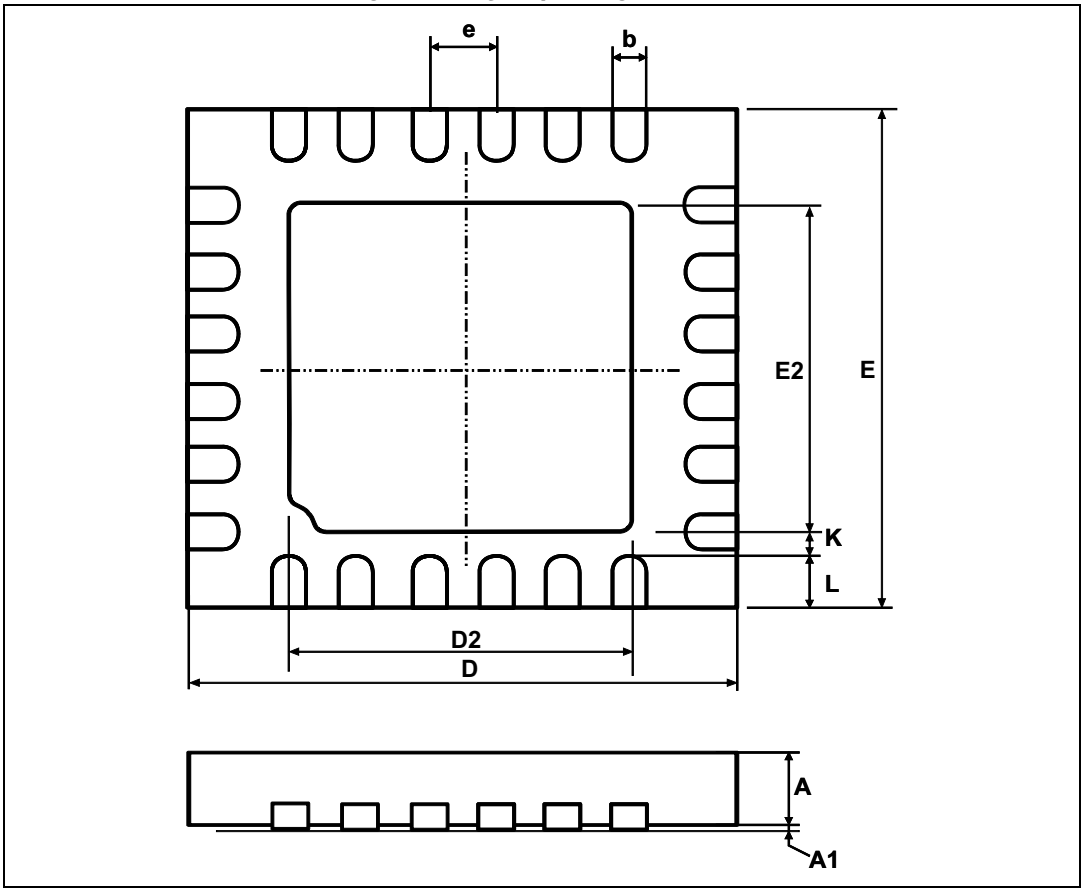
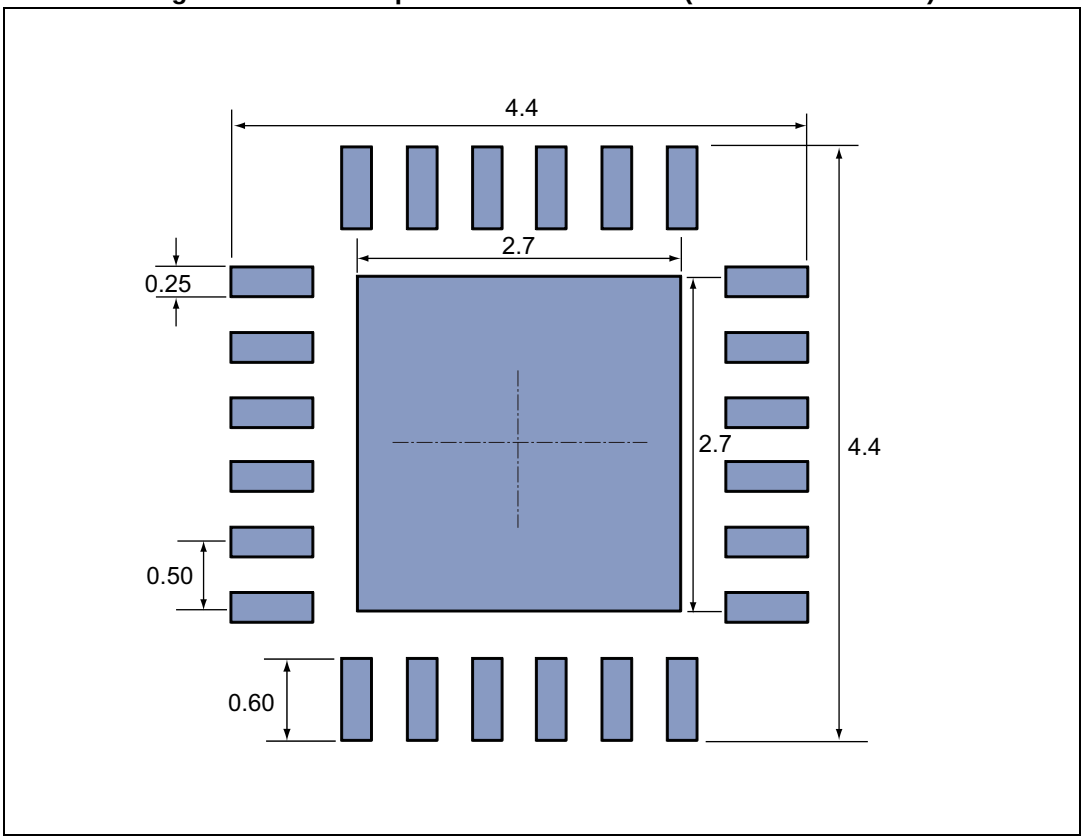


Table 10. QFN package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.000	0.002
b	0.18	0.25	0.30	0.007	0.009	0.011
D		4.00 BSC			0.157	
E		4.00 BSC			0.157	
e		0.50 BSC			0.020	
K	0.15			0.100	0.106	0.110
D2	2.55	2.70	2.80	0.100	0.106	0.110
E2	2.55	2.70	2.80	0.006		
L	0.30	0.40	0.50	0.011	0.0157	0.0196

Figure 26. PCB footprint recommendation (dimensions in mm)



4.2 Packing information

Figure 27. Marking specification

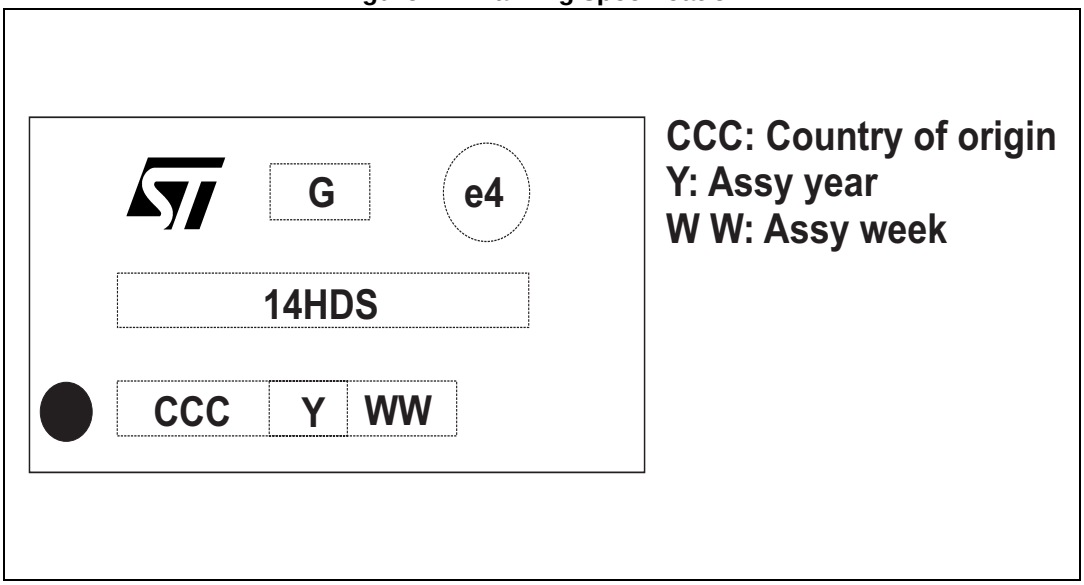
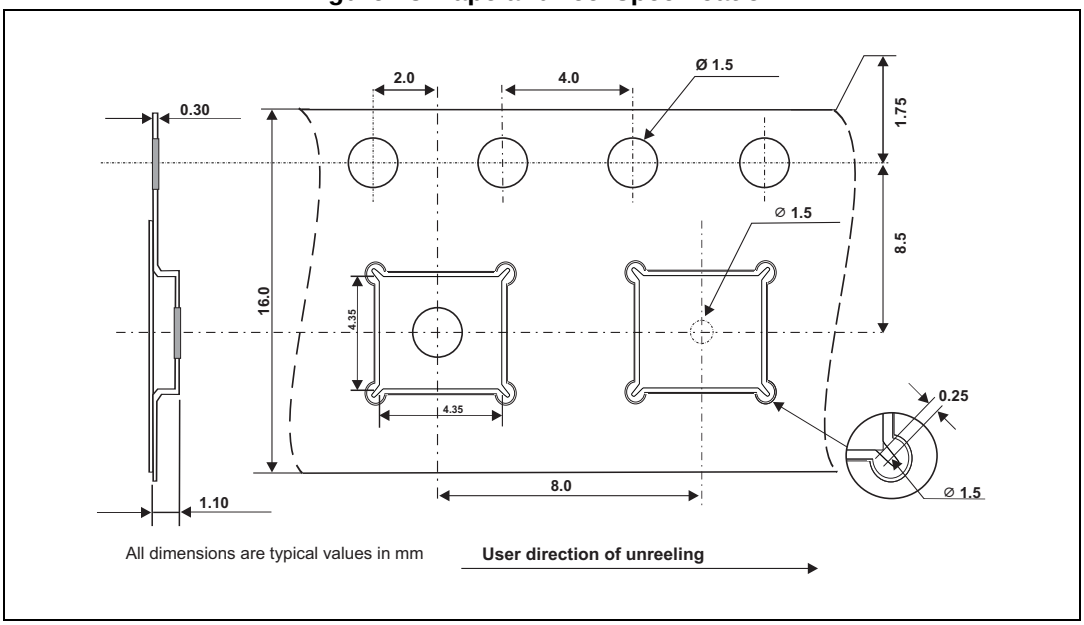


Figure 28. Tape and reel specification

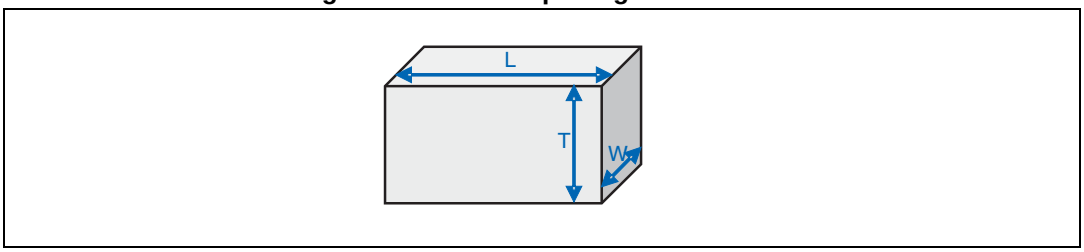


5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 29. Stencil opening dimensions



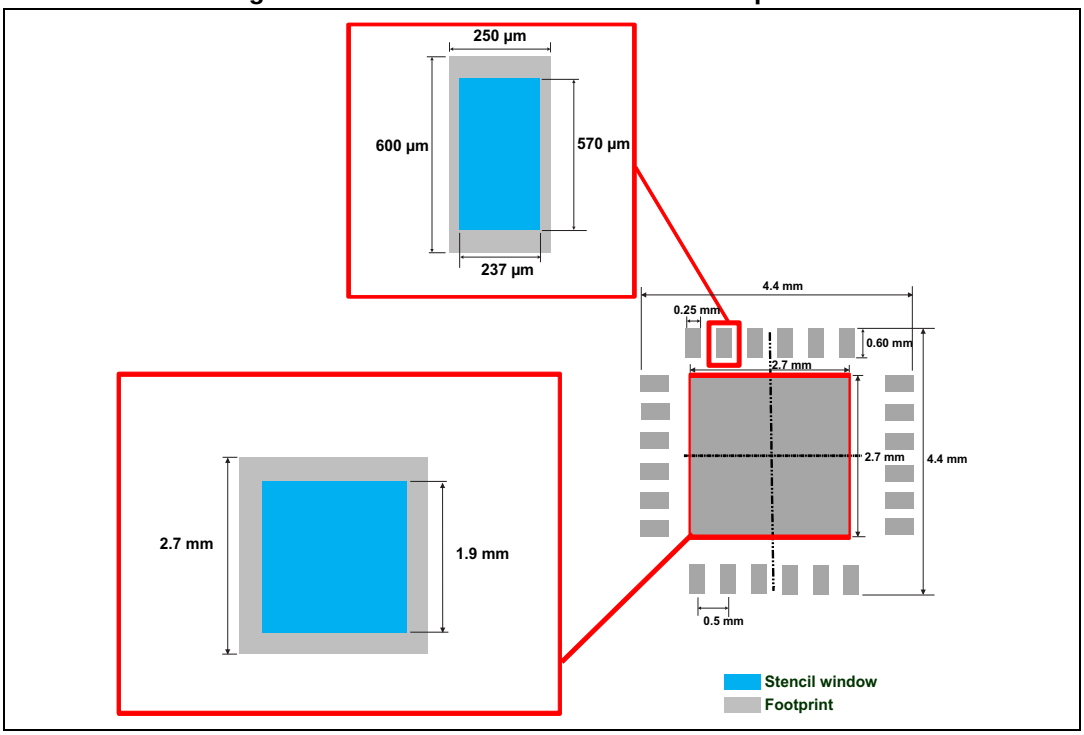
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 30. Recommended stencil window position



5.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

5.3 Placement

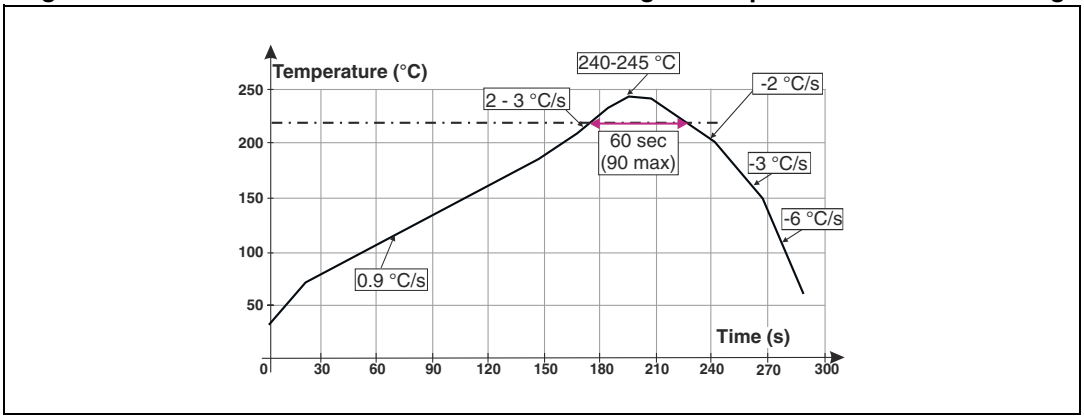
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, closed vias are recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. Symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 31. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Figure 32. Ordering information scheme

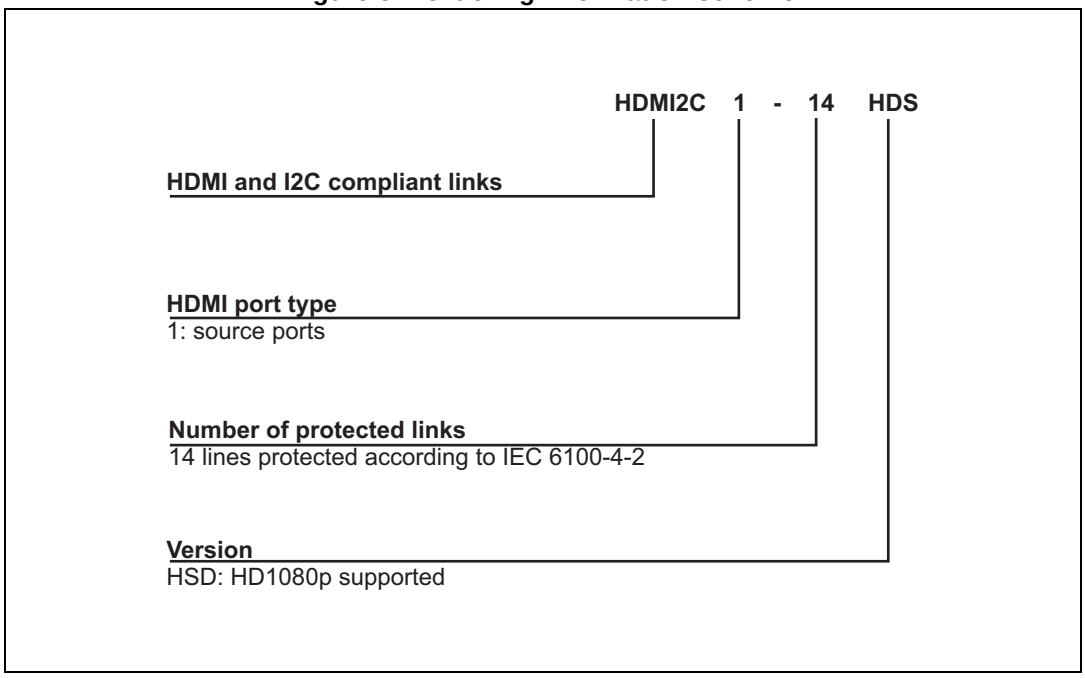


Table 11. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HDMI2C1-14HDS	14HDS	QFN_24L	44 mg	4,000	Tape and Reel

7 Revision history

Table 12. Document revision history

Date	Revision	Changes
25-Jul-2014	1	Initial release
10-Dec-2014	2	Updated *Figure 26*.
04-Sep-2015	3	Updated *Figure 1*, *Figure 12* and *Table 2*. Reformatted to current standards.