1 Application information

1.1 Power on reset

In order to activate the CEC and DDC lines, both following conditions must be respected:

- $V_{DD\_5V} > V_{DD\_ON}$ (see *Table 3*)
- Both inputs of the bi-directional level shifters must be set to a high level at the same time

1.2 CEC input and output levels in high-level

When the CEC signal is set to a high level (idle-state), pin 1 and pin 16 voltages can be different as the HDMI2C1-5DIJ works as a level-shifter. The line is then considered in open circuit between these two pins. Low levels are identical on both sides.

1.3 Schematics

Figure 2. Application schematic

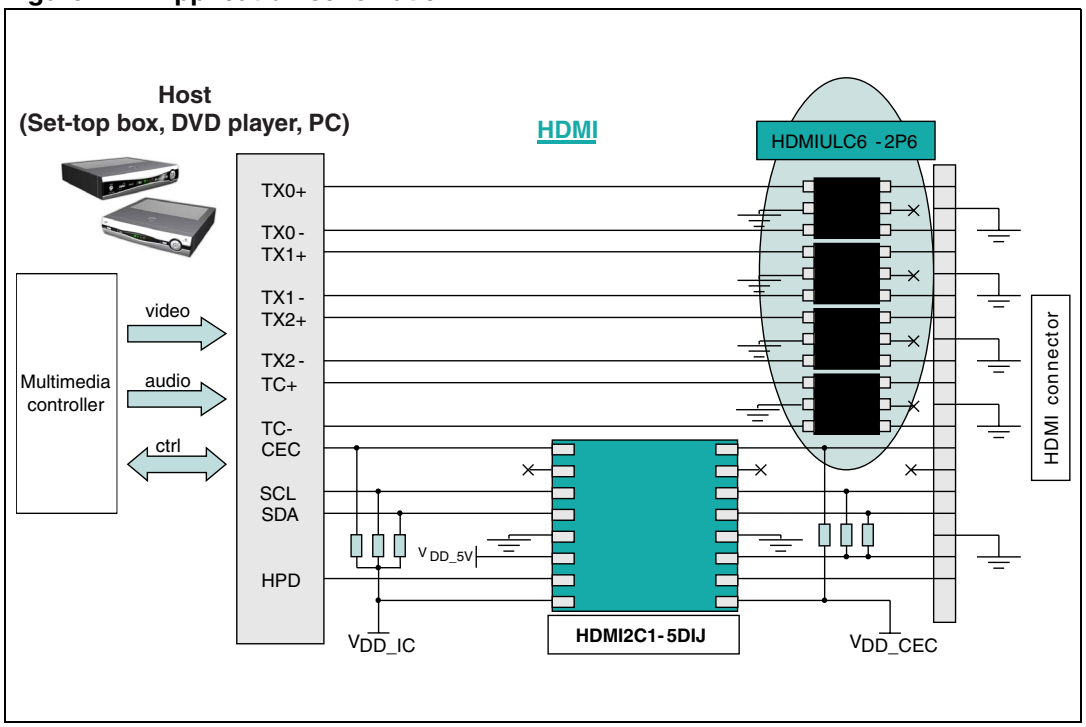
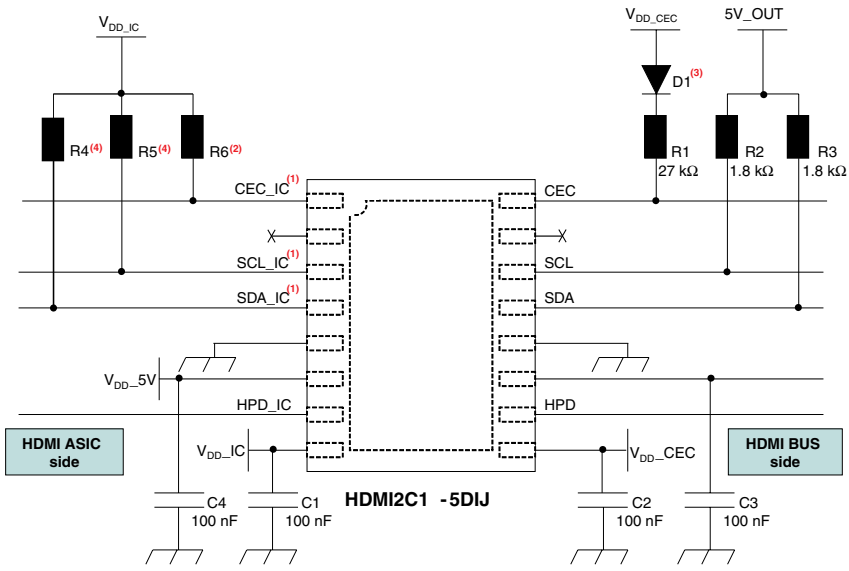


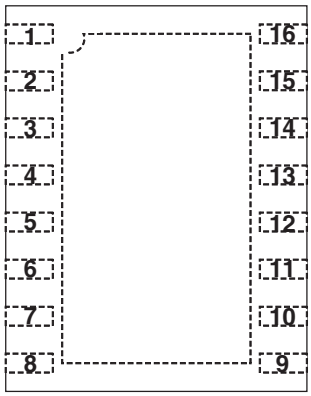
Figure 3. Electrical schematic



1. SCL_IC, SDA_IC and CEC_IC have to be driven with an ASIC working with open-drain outputs.
2. Possible values of R6 is typically in the range of 270 kΩ up to 1 MΩ
3. A small signal schottky diode D1 like BAT54 should be used to avoid any backdrive current flowing towards the V_{DD_CEC} supply.
4. Recommended value for R4 and R5 is typically 10 kΩ to be compliant with I²C levels.

Table 1. Pin descriptions

Pin	Name	Description
1	CEC_IC	Consumer electronic control (HDMI ASIC side)
2	N.C.	----
3	SLC_IC	DDC I²C clock line (HDMI ASIC side)
4	SDA_IC	DDC I²C data line (HDMI ASIC side)
5	GND	Ground
6	V_{DD_5V}	5 V supply
7	HPD_IC	Hot plug detect signal (HDMI ASIC side)
8	V_{DD_IC}	ASIC logic level reference voltage
9	V_{DD_CEC}	CEC line logic level reference voltage
10	HPD	Hot plug detect signal (HDMI bus side)
11	5V_OUT	Current limiter output (HDMI bus side)
12	GND	Ground
13	SDA	DDC I²C data line (HDMI Bus side)
14	SCL	DDC I²C clock line (HDMI Bus side)
15	N.C.	----
16	CEC	Consumer electronic control (HDMI Bus side)



QFN 5 X 4 16-lead
Top view

Figure 4. CEC link functional schematic

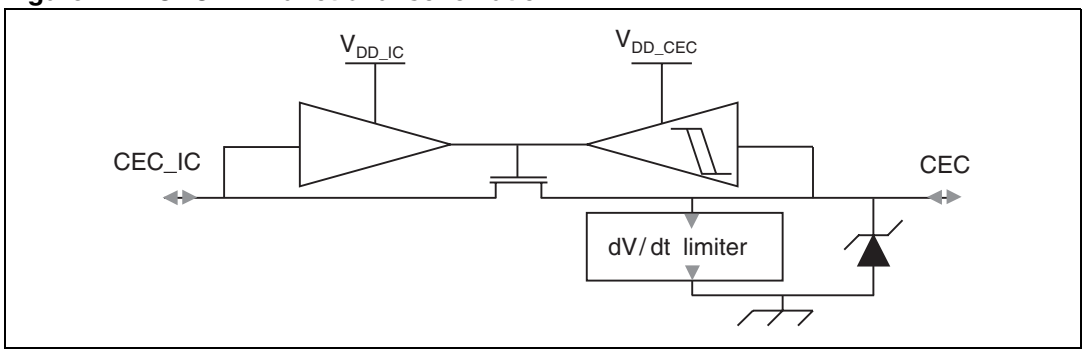


Figure 5. HPD link functional schematic

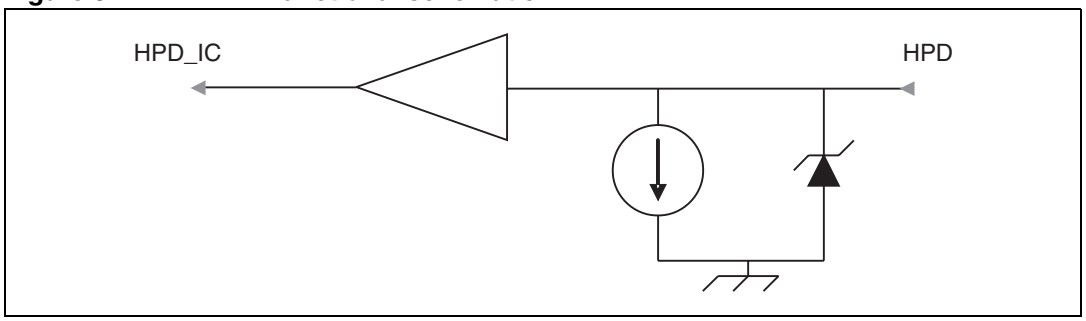


Figure 6. DDC link functional schematic

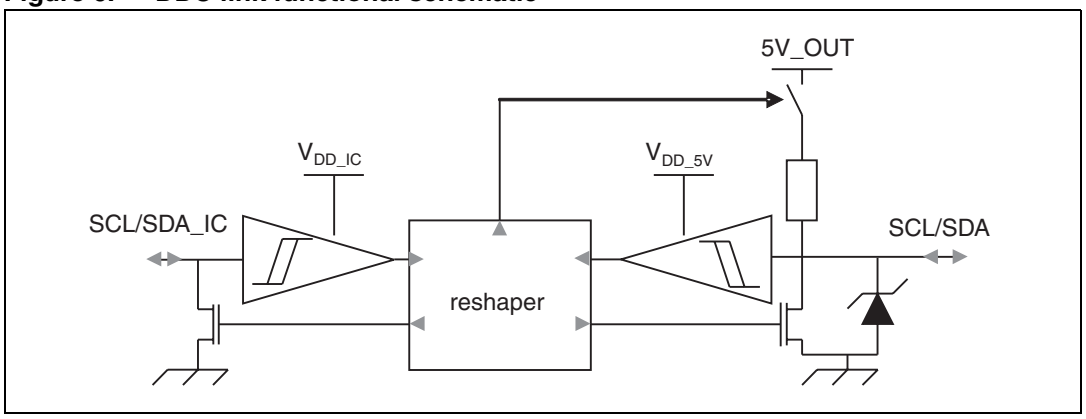
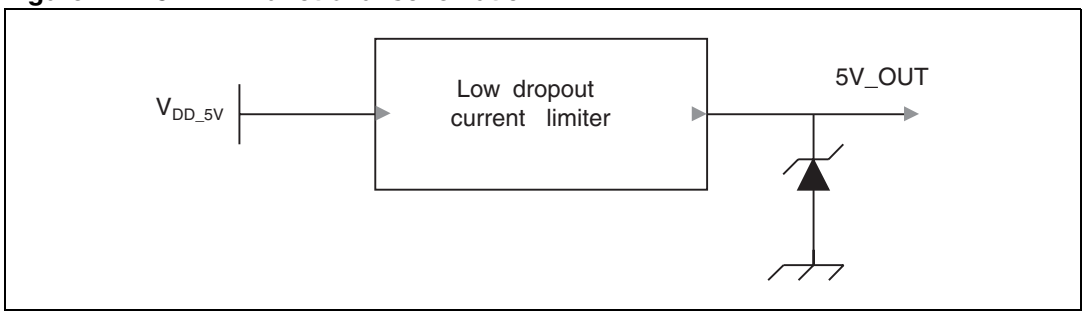


Figure 7. 5 V link functional schematic



2 Characteristics

Table 2. Absolute ratings

Symbol	Parameter	Test conditions	Value	Unit
V_{pp_BUS}	ESD discharge on HDMI BUS side (pin 10, 11, 13, 14,16), IEC 61000-4-2 level 4	Contact discharge	±8(1)	kV
V_{pp_IC}	ESD discharge (all pins), HBM JESD22-A114D level 2	Contact discharge	±2	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_{op}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
V_{DD_5V} V_{DD_IC} V_{DD_CEC}	Supply voltages		6	V
I_{DDC_IC}	Maximum allowed current sunk by SDA_IC or SCL_IC		1.5	mA

1. With a 100 nF capacitor connected to the 5 V output pin.

Table 3. Power supply characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD_CEC}	CEC supply voltage		2.97	3.3	3.63	V
V_{DD_IC}	Low-voltage supply		1.62		3.63	V
V_{DD_5V}	5 V input supply voltage range		4.9		5.3	V
V_{DD_ON}(1)	Power on reset				4.1	V
I_{QS_5V}	Quiescent currents on V_{DD_5V}, V_{DD_IC}, V_{DD_CEC}	V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, V_{DD_CEC} = 3.3 V Idle-state on CEC and DDC links, HPD and 5V_OUT links open			1000	µA
I_{QS_IC}					75	
I_{QS_CEC}					150	

1. In order to activate the CEC and DDC lines, both the following conditions must be respected:
   - $V_{DD\_5V} > V_{DD\_ON}$
   - Both inputs of the bi-directional level shifters must be set to a high level at the same time.

Table 4. CEC electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_CEC}	Upward input voltage threshold on bus side				2.0	V
V_{Tdown_CEC}	Downward input voltage threshold on bus side		0.8			V
V_{HYST_CEC}	Input hysteresis on bus side			0.4		V
T_{RISE_CEC}	Output rise-time	R_{UP} = 27 kΩ ± 5%	25(2)		250	µs
T_{FALL_CEC}	Output fall-time	R_{UP} = 27 kΩ ± 5%			50	µs
I_{OFF_CEC}	Leakage current in powered-off state	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{DD_CEC} = 3.3 V			1.8	µA
$V_{IL\_CEC\_IC}$	Input low level on IC side		30			$\%V_{DD\_IC}$
$V_{IH\_CEC\_IC}$	Input high level on IC side				70	$\%V_{DD\_IC}$
R_{ON_CEC}	On resistance across CEC and CEC_IC pins	CEC pin to 0 V		115	160	Ω
C_{in_CEC}	Input capacitance on CEC link	V_{DD_5V} = 0 V, V_{DD_CEC}=0 V, V_{DD_IC} = 0 V, V_{BIAS}=0 V, F = 100 kHz		17	25(3)	pF

1. T_{amb} = 25 °C, V_{DD_CEC} = 3.3 V, V_{DD_5V} = 5 V, unless otherwise specified.
2. The dV/dt limiter is used to ensure a minimum rise-time when a minimum load is connected to the link.
3. Maximum capacitance allowed at connector output is 200 pF in HDMI 1.3 specification.

Table 5. HDMI 5V_out current limiter electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DROP}	Drop-out voltage	I_{5V_OUT} = 55 mA	20	50	95(1)	mV
I_{5V_OUT}	Output current	V_{5V_OUT} = 0 V	55		115(2)	mA

1. HDMI 1.3 specification requires a maximum of 100 mV voltage-drop.
2. Maximum allowed output current is 500 mA when the sink is powered off in HDMI 1.3 specification.

Table 6. Hot-plug detect electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{PULL_DOWN}	Pull-down current			13	25	µA
V_{IL_HPD}	Input low-level		1			V
V_{IH_HPD}	Input high-level				1.7	V

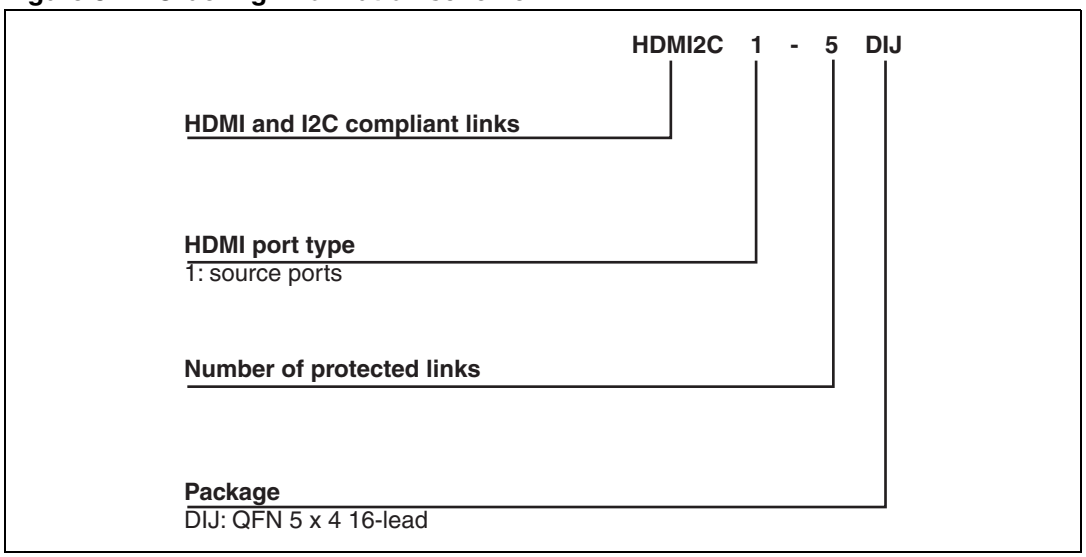
Table 7. DDC SDA/SCL electrical characteristics(1)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side				3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side		1.5			V
V_{HYST_BUS}	Input hysteresis on bus side		1		1.3	V
V_{OL_BUS}	Output low-level	Current sunk by SDA or SCL pin is 3 mA			350	mV
T_{RISE_BUS}	Output rise-time (30%-70%)	C_{BUS} = 750 pF(2), R_{UP} = 2 kΩ // 47 kΩ + 10 %(3)			900	ns
T_{FALL_BUS}	Output fall-time (30%-70%)				250	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55		65	$\%V_{DD\_IC}$
V_{Tdown_IC}	Downward input voltage threshold on IC side		35		45	$\%V_{DD\_IC}$
V_{OL_IC}	Output low-level on IC side	Current sunk by SDA_IC or SCL_IC pins is 500 µA			324(4)	mV
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{DD_CEC} = 0 V, V_{BIAS} = 0 V, F = 100 kHz		11	17(5)	pF

1. T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified.
2. Maximum load capacitance allowed on I2C entire link (cable plus connectors) is 750 pF in HDMI spec. 1.3.
3. Two pull-up resistors in parallel (sink + source). Typical value is 47 kΩ and maximum value is 47 kΩ + 10% in HDMI 1.3 specification.
4. V_{OL_IC} = 0.2* V_{DD_IC} (min).
5. Maximum capacitance allowed at connector output is 50 pF in HDMI spec. 1.3.

3 Ordering information scheme

Figure 8. Ordering information scheme

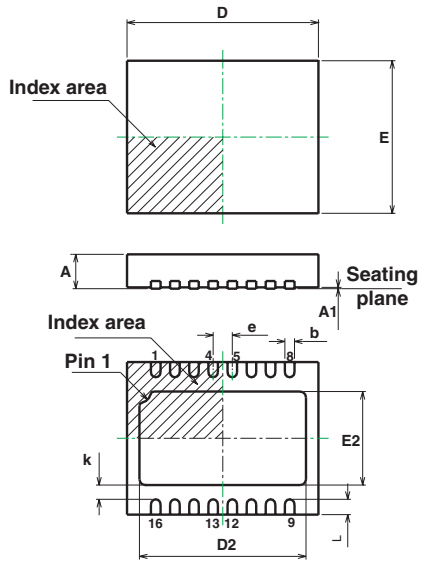


4 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. QFN 5 x 4 16 leads dimensions



Ref.	Dimensions					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	4.20	4.35	4.45	0.165	0.171	0.175
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.30	2.45	2.55	0.091	0.097	0.100
e		0.50			0.020	
k	0.20			0.008		
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 9. QFN 5 x 4 16-lead footprint (dimensions in mm)

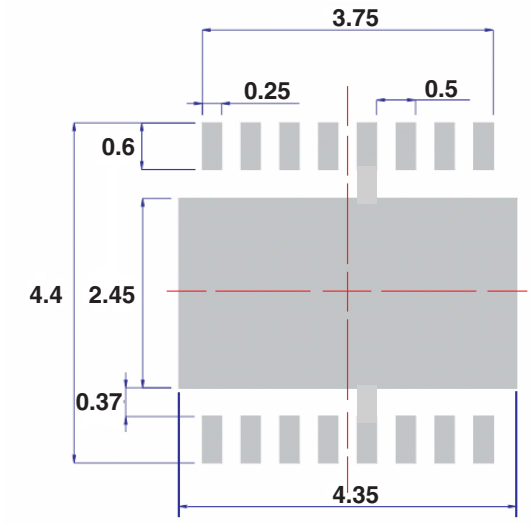
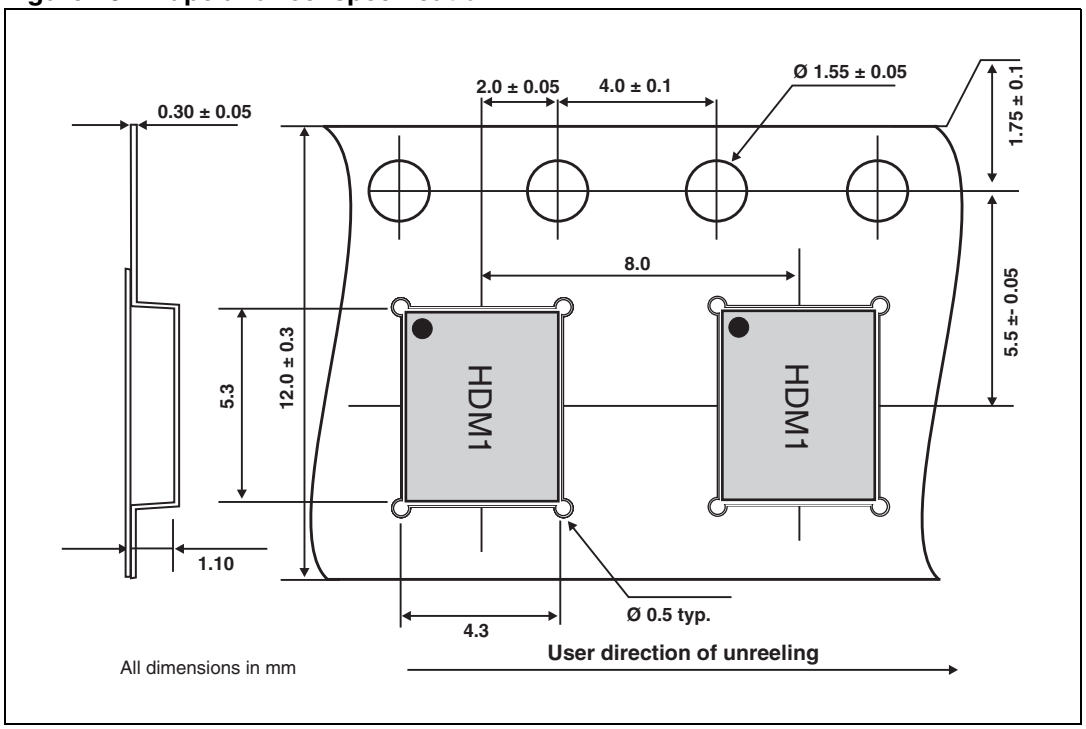


Figure 10. Tape and reel specification



5 Ordering information

Table 9. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HDMI2C1-5DIJ	HDM1	QFN 5x4 16-lead	60 mg	3000	Tape and reel

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Feb-2009	1	Initial release.
18-Mar-2009	2	Added *Table 1* Pin descriptions. Updated *Figure 2* and *Figure 3* for connection of resistor R4 to HPD.
19-May-2011	3	*Figure 1*: - add "NC" to not connected pins - change "GND" ref of the pad into "bulk" reference - add comment about the "bulk" on the bottom *Figure 9*: - connect "GND" pins to the heatsink copper surface. Updated *Figure 2* and *Figure 3.* *Table 2*: Updated $V_{pp_}$Bus parameter.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com