Devices

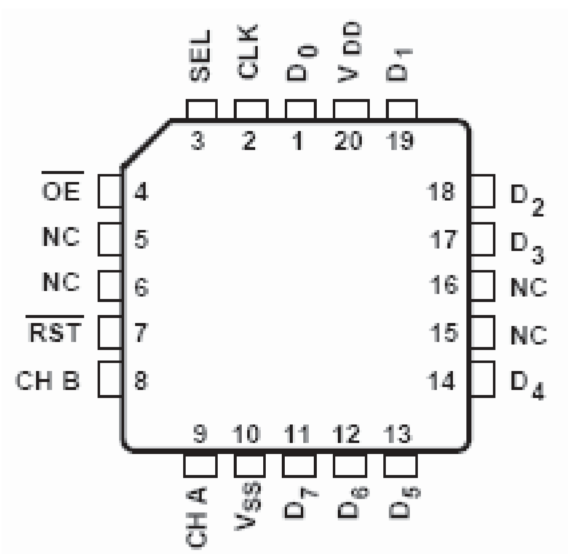
PINOUT A

Pin	Name	Name	Pin
1	D0	VDD	16
2	CLK	D1	15
3	SEL	D2	14
4	OE	D3	13
5	RST	D4	12
6	CH B	D5	11
7	CH A	D6	10
8	VSS	D7	9

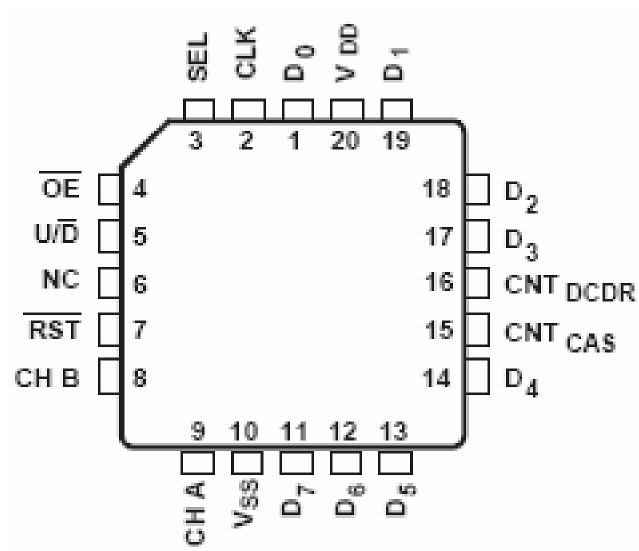
PINOUT B

Pin	Name	Name	Pin
1	D0	VDD	20
2	CLK	D1	19
3	SEL	D2	18
4	OE	D3	17
5	U/D	CNTdec	16
6	NC	CNTcas	15
7	RST	D4	14
8	CH B	D5	13
9	CH A	D6	12
10	VSS	D7	11

PINOUT C



PINOUT D



Package Dimensions

(dimension in mm)

See Appendix A.

Operating Characteristics

Table 1. Absolute Maximum Ratings

(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +6.0	V
Input Voltage	V_{IN}	-0.3 to (VDD +0.3)	V
Storage Temperature	T_S	-55 to +150	C
Operating Temperature [1]	T_A	-40 to +85	C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	4.5 to 5.5	V
Ambient Temperature [1]	T_A	-40 to +85	C

Table 3. DC Characteristics V_{DD} = 5V ± 5%; T_A = -40 to 85°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIL [2]	Low-Level Input Voltage				1.5	V
VIH [2]	High-Level Input Voltage		3.5			V
VT+	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
VT-	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
VH	Schmitt-Trigger Hysteresis		1.0	2.0		V
IIN	Input Current	VIN=VSS or VDD	-10	1	+10	µA
VOH [2]	High-Level Output Voltage	IOH = -3.75 mA	2.4	4.5		V
VOL [2]	Low-Level Output Voltage	IOL = +3.75mA		0.2	0.4	V
IOZ	High-Z Output Leakage Current	VO=VSS or VDD	-10	1	+10	µA
IDD	Quiescent Supply Current	VIN=Vss or VDD		1	100	µA
CIN [3]	Input Capacitance	Any Input		5		pF
COUT [3]	Output Capacitance	Any Output		5		pF

Notes:

1. Free Air
2. In general, for any V_{DD} between the allowable limits (+4.5V to +5.5V), $V_{IL} = 0.3V_{DD}$ and $V_{IH} = 0.7V_{DD}$; typical values are $V_{OH} = V_{DD} - 0.5V$ and $V_{OL} = V_{SS} + 0.2V$
3. Including package capacitance

Functional Pin Description

Table 4a. Functional Pin Descriptions (PDIP Package)

Symbol	Pin			Description
	HCTL-2001-A00	HCTL-2017-A00	HCTL-2021-A00	
VDD	16	16	20	Power Supply
VSS	8	8	10	Ground
CLK	2	2	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	7 6	7 6	9 8	CHA and CHB are Schmitt-trigger inputs that accept the outputs from a quadrature-encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
RST	5	5	7	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. RST is asynchronous with respect to any other input signals.
OE	4	4	4	This CMOS active low input enables the tri-state output buffers. The OE/ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	3	3	These CMOS inputs directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in OE/ above, SEL also control the internal inhibit logic. **SEL** / **BYTE SELECTED**: 0 – High; 1 – Low
CNT_{DCDR}	NA	NA	16	A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition. CNT
U/D	NA	NA	5	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNTDCDR and CNTCAS outputs. The proper signal U (high level) or D/ (low level) will be present before the rising edge of the CNTDCDR and CNTCAS outputs.
CNTCAS	NA	NA	15	A pulse is presented on this LSTTL-compatible output when the HCTL-2021-A00 internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
D0	1	1	1	These LSTTL-compatible tri-state outputs form an 8-bit output ports through which the contents of the 16-bit position latch may be read in 2 sequential bytes. The High byte is read first followed by the Low bytes.
D1	15	15	19	
D2	14	14	18	
D3	13	13	17	
D4	12	12	14	
D5	11	11	13	
D6	10	10	12	
D7	9	9	11	
NC	NA	NA	6	Not connected - this pin should be left floating.

Table 4b. Functional Pin Descriptions (PLCC Package)

Symbol	Pin		Description
	HCTL 2017-PLC	HCTL 2021-PLC	
VDD	20	20	Power Supply
VSS	10	10	Ground
CLK	2	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	9 8	9 8	CHA and CHB are Schmitt-trigger inputs that accept the outputs from a quadrature-encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
RST	7	7	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. RST is asynchronous with respect to any other input signals.
OE	4	4	This CMOS active low input enables the tri-state output buffers. The OE/ and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	3	These CMOS inputs directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in OE/ above, SEL also control the internal inhibit logic. SEL = 0: BYTE SELECTED High; SEL = 1: BYTE SELECTED Low
CNTDCDR	NA	16	A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition.
U/D	NA	5	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNTDCDR and CNTCAS outputs. The proper signal U (high level) or D/ (low level) will be present before the rising edge of the CNTDCDR and CNTCAS outputs.
CNTCAS	NA	15	A pulse is presented on this LSTTL-compatible output when the HCTL-2021-PLC internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
D0	1	1	These LSTTL-compatible tri-state outputs form an 8-bit output ports through which the contents of the 16-bit position latch may be read in 2 sequential bytes. The High byte is read first followed by the Low bytes.
D1	19	19	
D2	18	18	
D3	17	17	
D4	14	14	
D5	13	13	
D6	12	12	
D7	11	11	

SEL table:

SEL	BYTE SELECTED
0	High
1	Low

Switching Characteristics

Table 5. Switching Characteristics Max/Min specifications at V_{DD} = 5.0 ± 5%, T_A = -40 to +85 ^{0}C, C_L = 40 pf

Symbol		Description	Min.	Max.	Units
1	tCLK	Clock Period	70		ns
2	tCHH	Pulse width, clock high	28		ns
3	tCD	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	tODE	Delay time, OE fall to valid data		65	ns
5	tODZ	Delay time, OE rise to Hi-Z state on D0-7		40	ns
6	tSDV	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	tCLH	Pulse width, clock low	28		ns
8	tSS	Setup time, SEL before clock fall	20		ns
9	tOS	Setup time, OEN before clock fall	20		ns
10	tSH	Hold time, SEL after clock fall	0		ns
11	tOH	Hold time, OE after clock fall	0		ns
12	tRST	Pulse width, RST low	28		ns
13	tDCD	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	tDSD	Hold time, last data byte stable after next SEL state change	10		ns
15	tDOD	Hold time, data byte stable after OE rise	10		ns
16	tUDD	Delay time, U/D valid after clock rise		45	ns
17	tCHD	Delay time, CNTDCDR or CNTCAS high after clock rise		45	ns
18	tCLD	Delay time, CNTDCDRor CNTCAS low after clock fall		45	ns
19	tUDH	Hold time, U/D stable after clock rise	10		ns
20	tUDCS	Setup time, U/D valid before CNTDCDR or CNTCAS rise	tCLK-45		ns
21	tUDCH	Hold time, U/D stable after CNTDCDR or CNTCAS rise	tCLK-45		ns

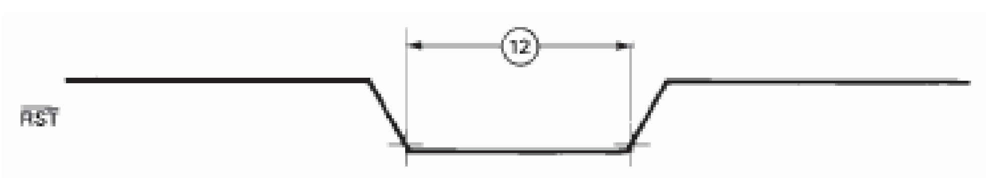


Figure 1. Reset Waveform

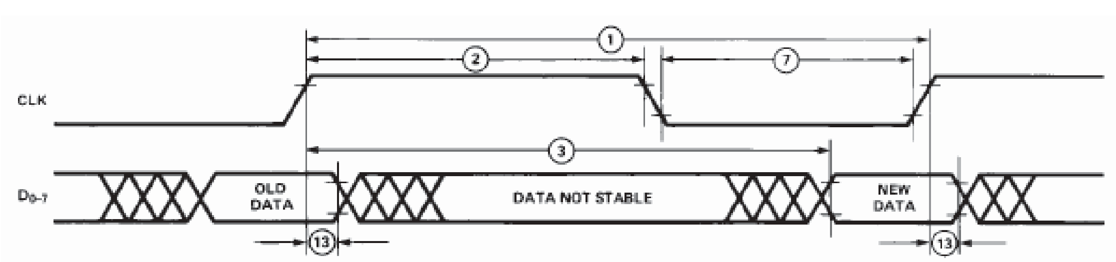


Figure 2: Waveforms for Positive Clock Edge Related Delays

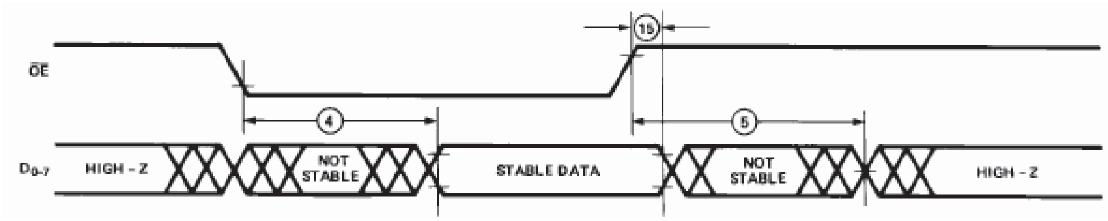


Figure 3: Tri-State Output Timing

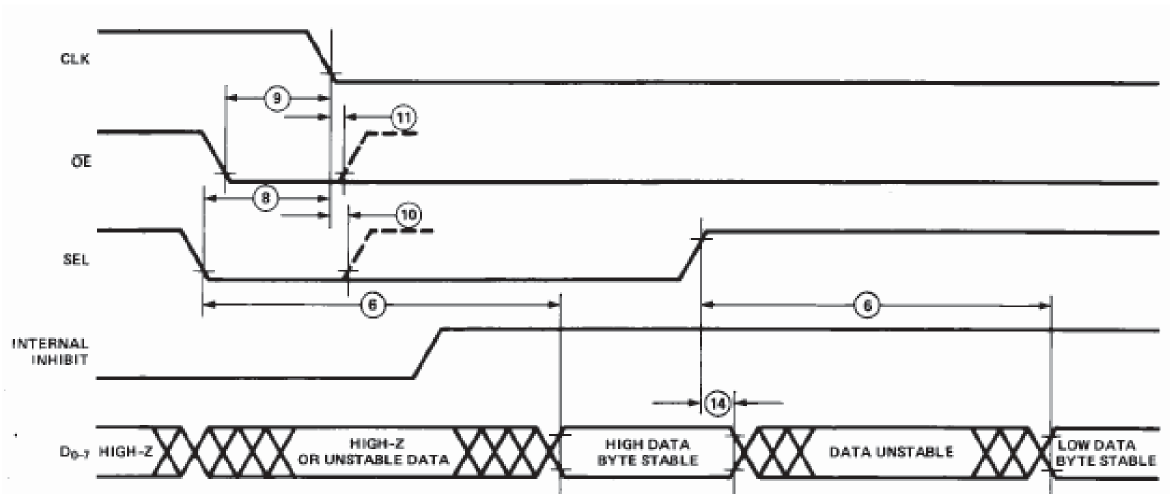


Figure 4: Bus Control Timing

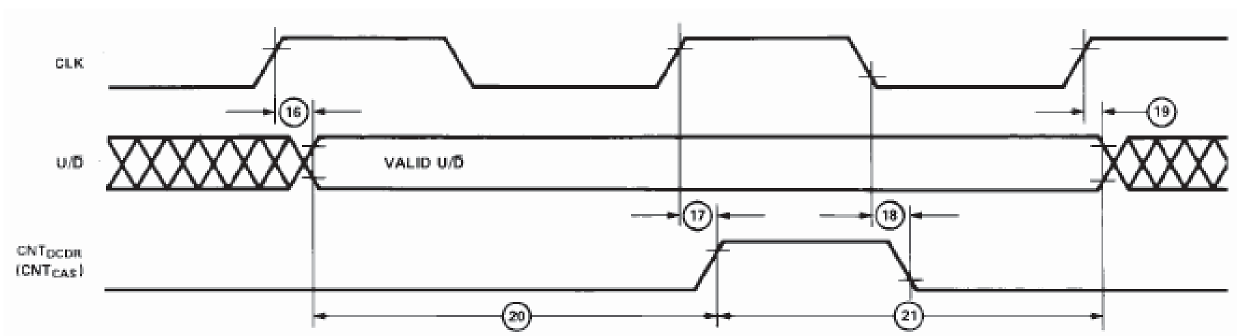


Figure 5: Decoder, Cascade Output Timing

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

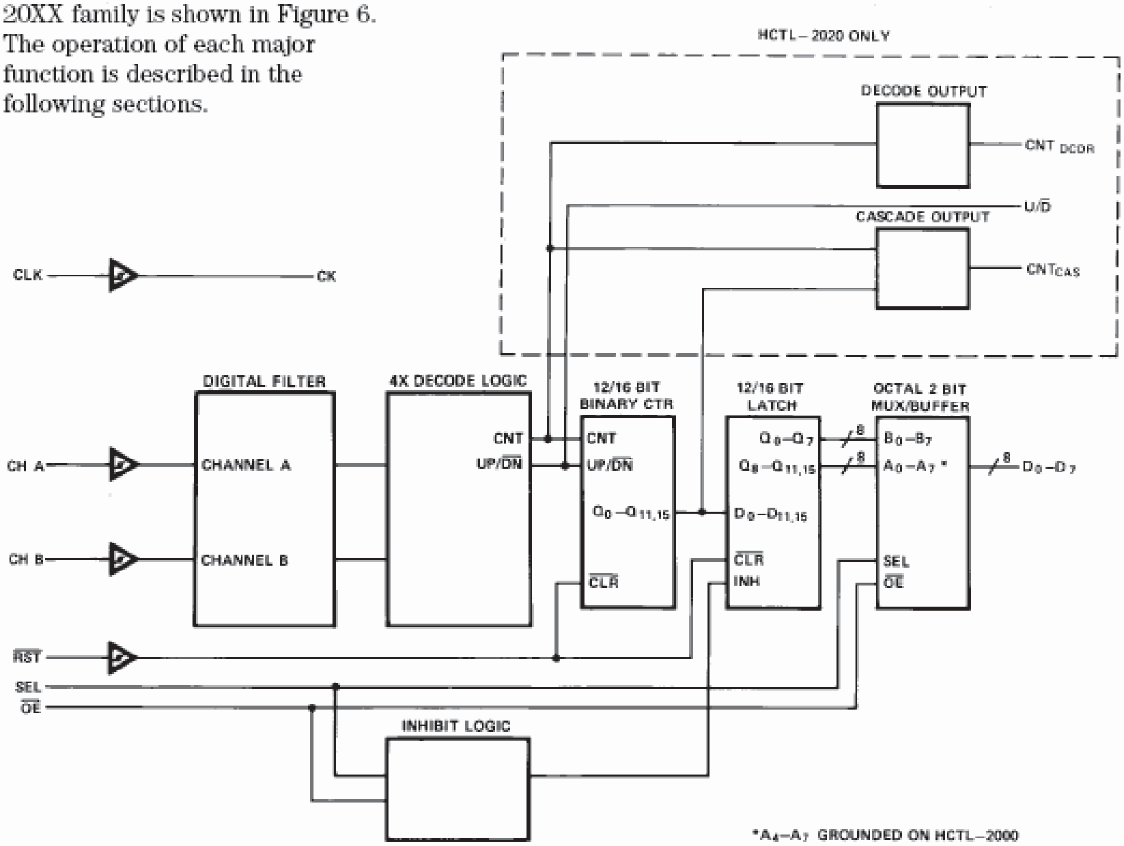


Figure 6. Simplified Logic Diagram

Digital Noise Filter

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 7 shows the simplified schematic of the input section. The signals are first passed through a Schmitt-trigger buffer to address the problem of input signals with slow rise times and low-level noise (approximately < 1V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges.

Refer to Figure 8, which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

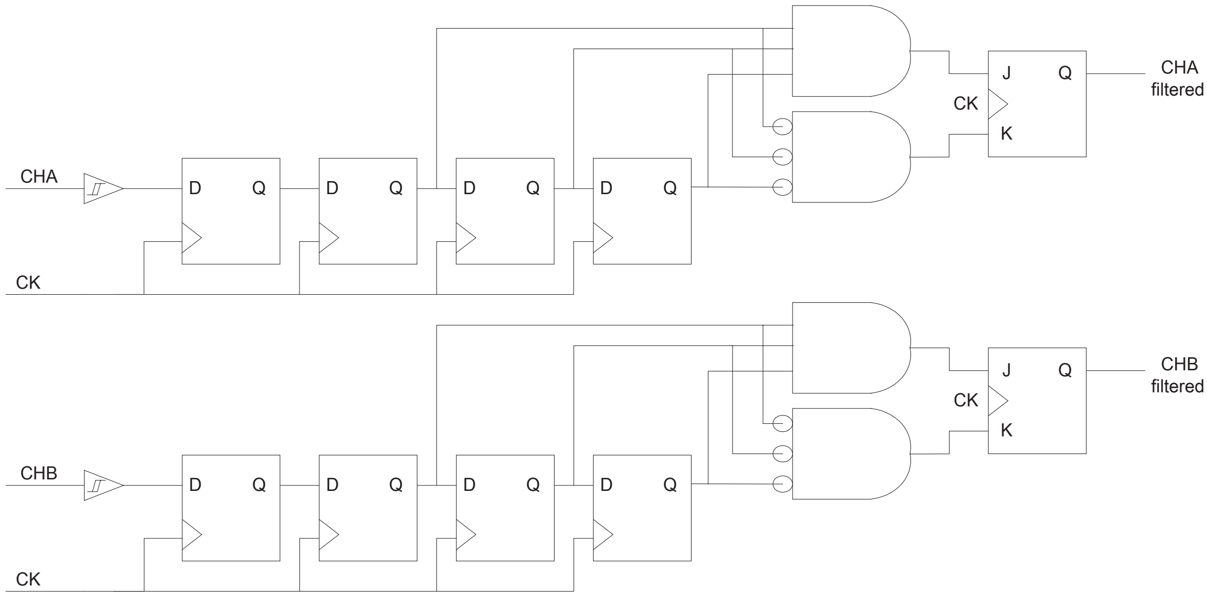


Figure 7. Simplified Digital Noise Filter Logic

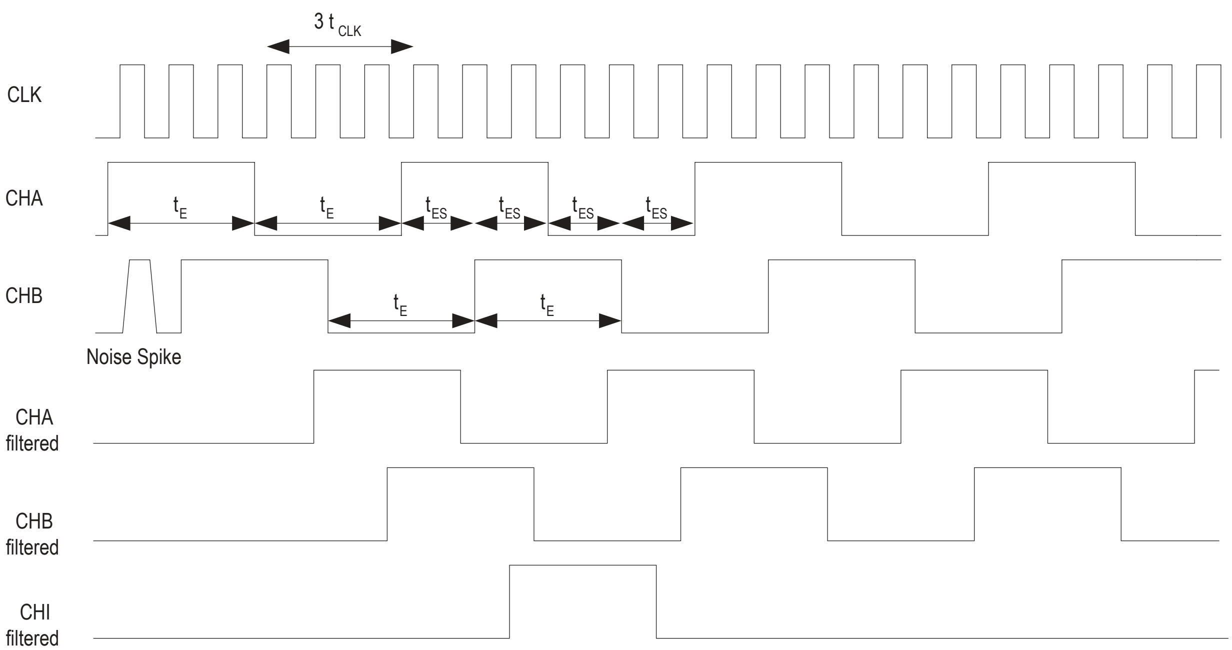


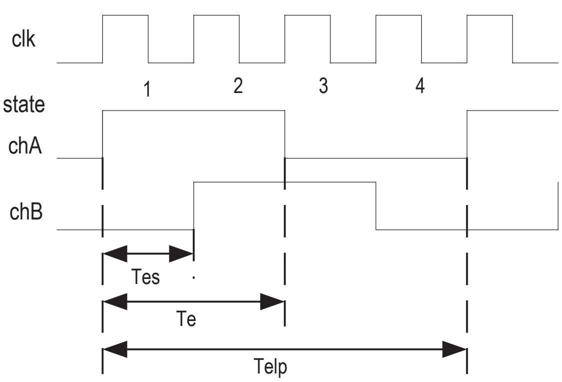
Figure 8. Signal Propagation through Digital Noise Filter

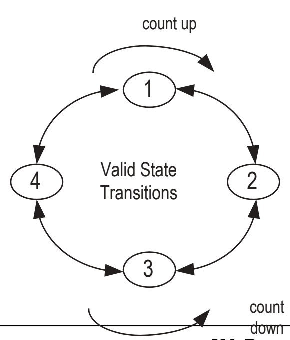
Quadrature Decoder

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding).

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the integral position counter.

Figure 9 shows the quadrature states of Channel A and Channel B signals. The 4x decoder will output a count signal for every state transition (count up and count down). Figure 9 shows the valid state transitions for 4x decoder. The 4x decoder will output a count signal at respective state transition, depending on the counting direction. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.





CHA	CHB	STATE	4X Decoder (Count Up & Count Down)
1	0	1	Pulse
1	1	2	Pulse
0	1	3	Pulse
0	0	4	Pulse

Figure 9. 4x Decoder Mode

Design Considerations

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 8 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high) has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take into account finite rise time of the waveforms, asymmetry of the waveforms, and noise. In the presence of large amounts of noise, t_E should be much greater than $3t_{CLK}$— to allow for the interruption of the consecutive level sampling by the three-bit delay filter. It should be noted that a change on the inputs that is qualified by the filter will internally propagate in a maximum of seven clock periods.

The quadrature decoder circuitry imposes a second timing constraint between the external clock and the input signals. There must be at least one clock period between consecutive quadrature states. As shown in Figure 8, a quadrature state is defined by consecutive edges on both channels. Therefore, t_{ES} (encoder state period) > t_{CLK}-. The designer must account for deviations from the nominal 90 degree phasing of input signals to guarantee that $t_{ES} > t_{CLK}$.

Position Counter

This section consists of a 16-bit binary up/down counter which counts on rising clock edges as explained in the Quadrature Decoder Section. All 16-bit of data are passed to the position data latch. The system can use this count data in several ways:

A. System total range is £ 16 bits, so the count represents "absolute" position.

B. The system is cyclic with £ 16 bits of count per cycle. RSTN (or CHI) is used to reset the counter every cycle and the system uses the data to interpolate within the cycle.

C. System count is > 8 or 16 bits, so the count data is used as a relative or incremental position input for a system software computation of absolute position. In this case counter rollover occurs. In order to prevent loss of position information, the processor must read the outputs of the IC before the count increments one-half of the maximum count capability. Two's-complement arithmetic is normally used to compute position from these periodic position updates.

D. The system count is >16 bits so the HCTL-2021-A00/PLC can be cascaded with other standard counter ICs to give absolute position.

Position Data Latch

The position data latch is a 16-bit latch which captures the position counter output data on each rising clock edge, except when its inputs are disabled by the inhibit logic section during two-byte read operations. The output data is passed to the bus interface section. When active, a signal from the inhibit logic section prevents new data from being captured by the latch, keeping the data stable while successive reads are made through the bus section. The latch is automatically re-enabled at the end of these reads. The latch is cleared to 0 asynchronously by the RST signal.

Inhibit Logic

The Inhibit Logic Section samples the OE and SEL signals on the falling edge of the clock and, in response to certain conditions (see Figure 10), inhibits the position data latch. The RST signal asynchronously clears the inhibit logic, enabling the latch.

Bus Interface

The bus interface section consists of a 16 to 8 line multiplexer and an 8-bit, three-state output buffer. The multiplexer allows independent access to the low and high bytes of the position data latch. The SEL and OE signals determine which byte is output and whether or not the output bus is in the high-Z state.

Quadrature Decoder Output

The quadrature decoder output section consists of count and up/down outputs derived from the 4x decoder mode of the HCTL-2021-A00/PLC. When the decoder has detected a count, a pulse, one-half clock cycle long, will be output on the CNT_{DCDR} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{DCDR} pulse, and held one clock cycle after the rising edge of the CNT_{DCDR} pulse. These outputs are not affected by the inhibit logic.

Cascade Output (HCTL-2021-A00/PLC only!)

The cascade output also consists of count and up/down outputs. When the HCTL-2021-A00/PLC internal counter overflows or underflows, a pulse, one-half clock cycle long, will be output on the CNT_{CAS} pin. This output will occur during the clock cycle in which the internal counter is updated. The U/D pin will be set to the proper voltage level one clock cycle before the rising edge of the CNT_{CAS} pulse, and held one clock cycle after the rising edge of the CNT_{CAS} pulse. These outputs are not affected by the inhibit logic.

Step	SEL	OE	CLK	Inhibit Signal	Action
1	L	L	Falling	1	Set inhibit; read high byte
2	H	L	Falling	1	Read low byte; starts reset
3	X	H	Falling	0	Complete inhibit logic reset

Figure 10. Two Bytes Read Sequence

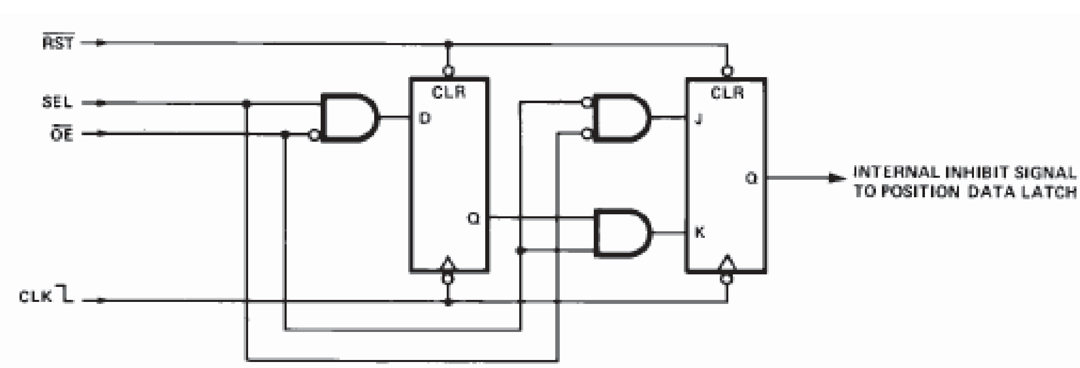


Figure 11. Simplified Inhibit Logic

Cascade Considerations (HCTL-2021-A00/PLC only!)

The HCTL-2021-A00/PLC cascading system allows for position reads of more than two bytes. These reads can be accomplished by latching all the bytes and then reading the bytes sequentially over the 8-bit bus. It is assumed here that, externally, a counter followed by a latch is used to count any count that exceeds 16 bits. This configuration is compatible with the HCTL-2021-A00/PLC internal counter/latch combination.

Consider the sequence of events for a read cycle that starts as the HCTL-2021-A00/PLC internal counter rolls over. On the rising clock edge, count data is updated in the internal counter, rolling it over. A count-cascade pulse (CNT_{CAS}) will be generated with some delay after the rising clock edge (t_{CHD}). There will be additional propagation delays through the external counters and registers. Meanwhile, with SEL and OE low to start the read, the internal latches are inhibited at the falling edge and do not update again till the inhibit is reset.

If the CNT_{CAS} pulse now toggles the external counter and this count gets latched a major count error will occur. The count error is because the external latches get updated when the internal latch is inhibited.

Valid data can be ensured by latching the external counter data when the high byte read is started (SEL and OE low). This latched external byte corresponds to the count in the inhibited internal latch. The cascade pulse that occurs during the clock cycle when the read begins gets counted by the external counter and is not lost.

For example, suppose the HCTL-2021-A00/PLC count is at FFFFh and an external counter is at F0h, with the count going up. A count occurring in the HCTL-2021-A00/PLC will cause the counter to roll over and a cascade pulse will be generated. A read starting on this clock cycle will show FFFFh from the HCTL-2021-A00/PLC. The external latch should read F0h, but if the host latches the count after the cascade signal propagates through, the external latch will read F1h.

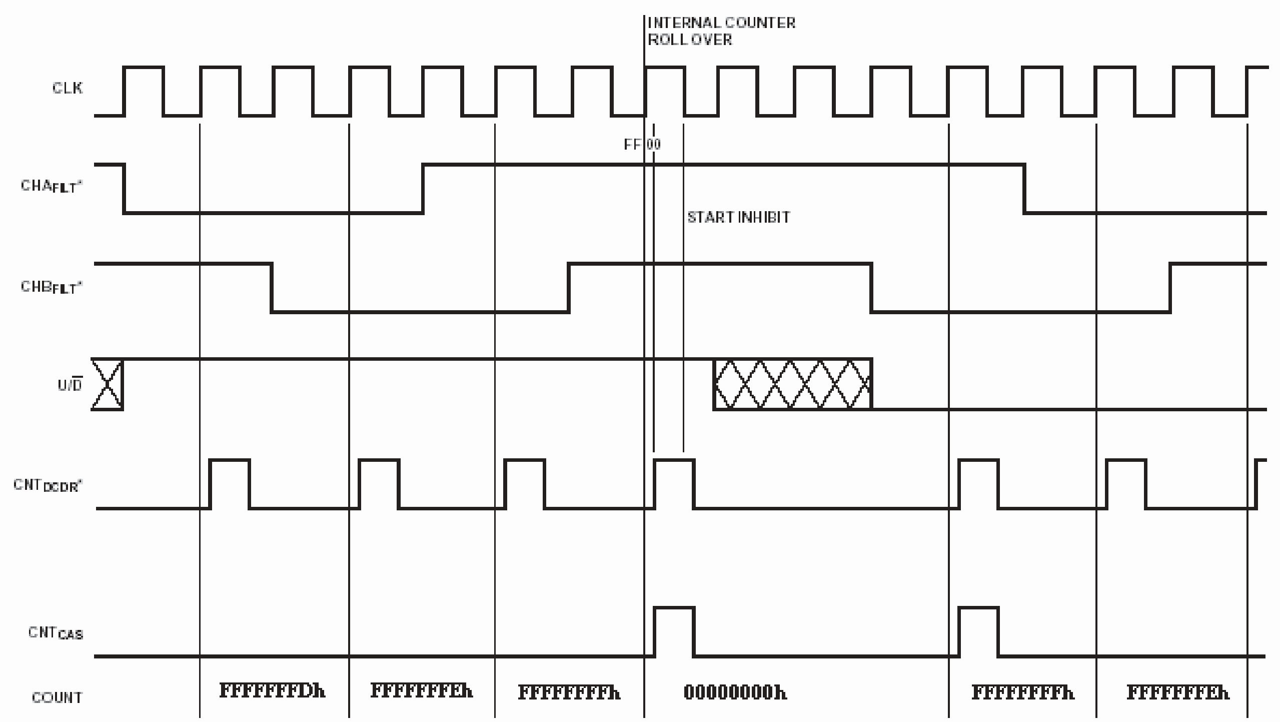


Figure 12. Decode and Cascade Output Diagram (4x)

General Interfacing

The 16-bit latch and inhibit logic allows access to 16 bits of count with an 8-bit bus. When only 8-bits of count are required, a simple 8-bit (1-byte) mode is available by holding SEL high continuously. This disables the inhibit logic. OE provides control of the tri-state bus, and read timing is shown in Figure 2 and 3.

For proper operation of the inhibit logic during a two-byte read, OE and SEL must be synchronous with CLK due to the falling edge sampling of OE and SEL.

The internal inhibit logic on the HCTL-2021-A00/PLC inhibits the transfer of data from the counter to the position data latch during the time that the latch outputs are being read. The inhibit logic allows the microprocessor / microcontroller to first read the high order 4 or 8 bits from the latch and then read the low order 8 bits from the latch. Meanwhile, the counter can continue to keep track of the quadrature states from the CHA and CHB input signals.

Figure 11 shows the simplified inhibit logic circuit. The operation of the circuitry is illustrated in the read timing shown in Figure 13.

Actions

1. On the rising edge of the clock, counter data is transferred to the position data latch, provided the inhibit signal is low.
2. When OE goes low, the outputs of the multiplexer are enabled onto the data lines. If SEL is low, then the high order data bytes are enabled onto the data lines. If SEL is high, then the low order data bytes are enabled onto the data lines.
3. When the IC detects a low on OE and SEL during a falling clock edge, the internal inhibit signal is activated. This blocks new data from being transferred from the counter to the position data latch.
4. When SEL goes high, the data outputs change from the high byte to the low byte.
5. The first of two reset conditions for the inhibit logic is met when the IC detects a logic high on SEL and a logic low on OE during a falling clock edge.
6. When OE goes high, the data lines change to a high impedance state.
7. The IC detects a logic high on OE during a falling clock edge. This satisfies the second reset condition for the inhibit logic.

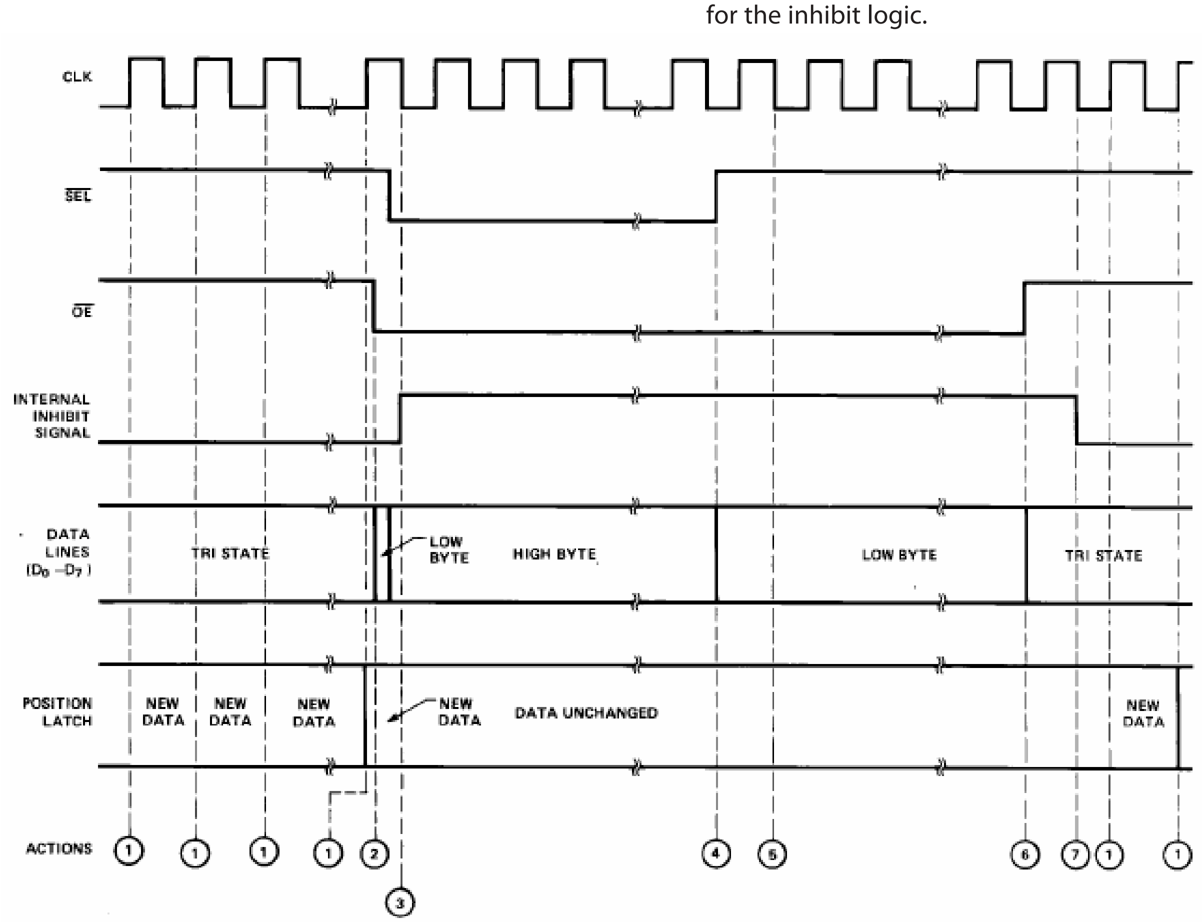
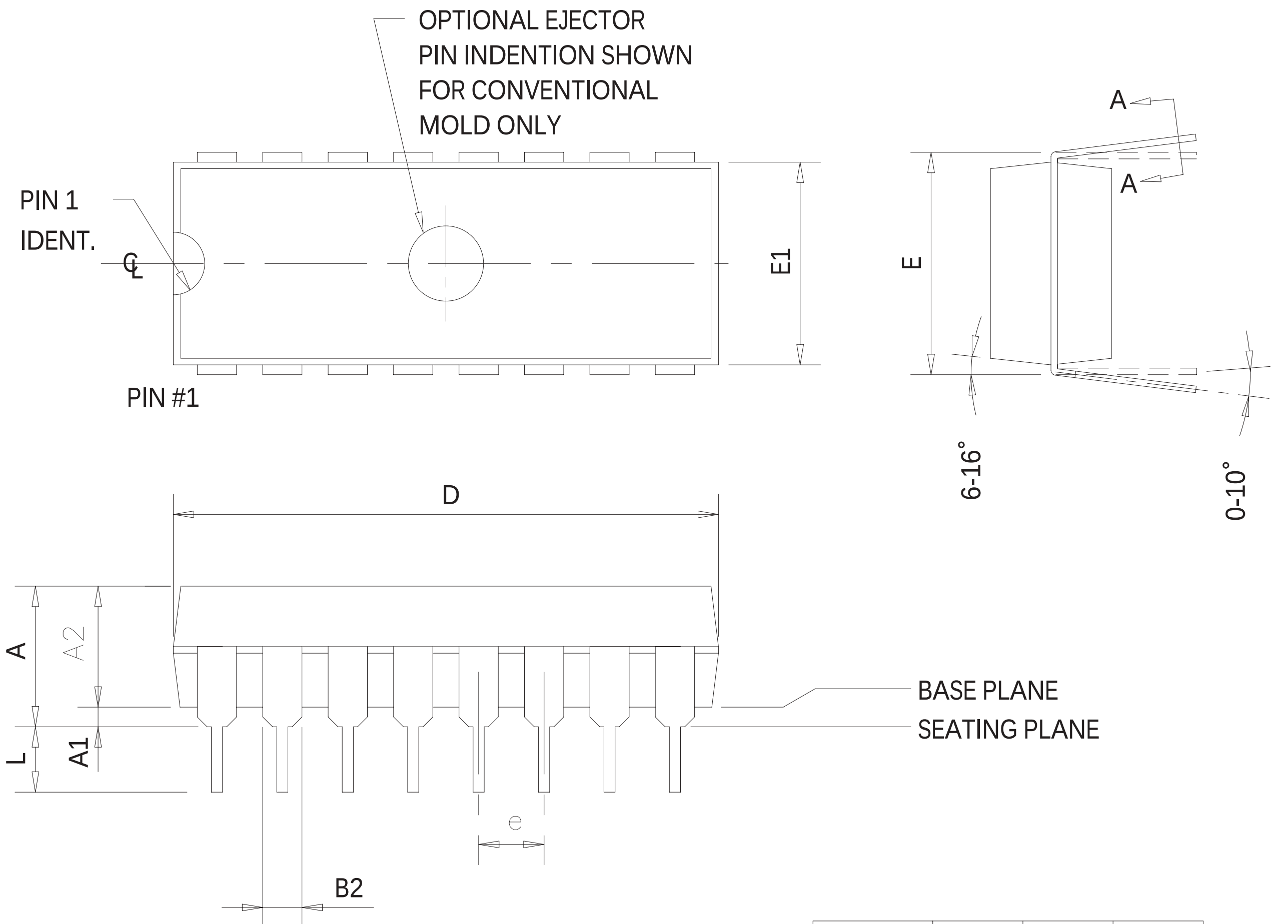
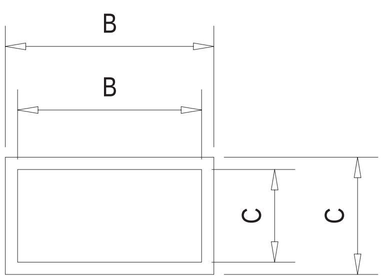


Figure 13. Typical Interface Timing

APPENDIX A

PACKAGE A



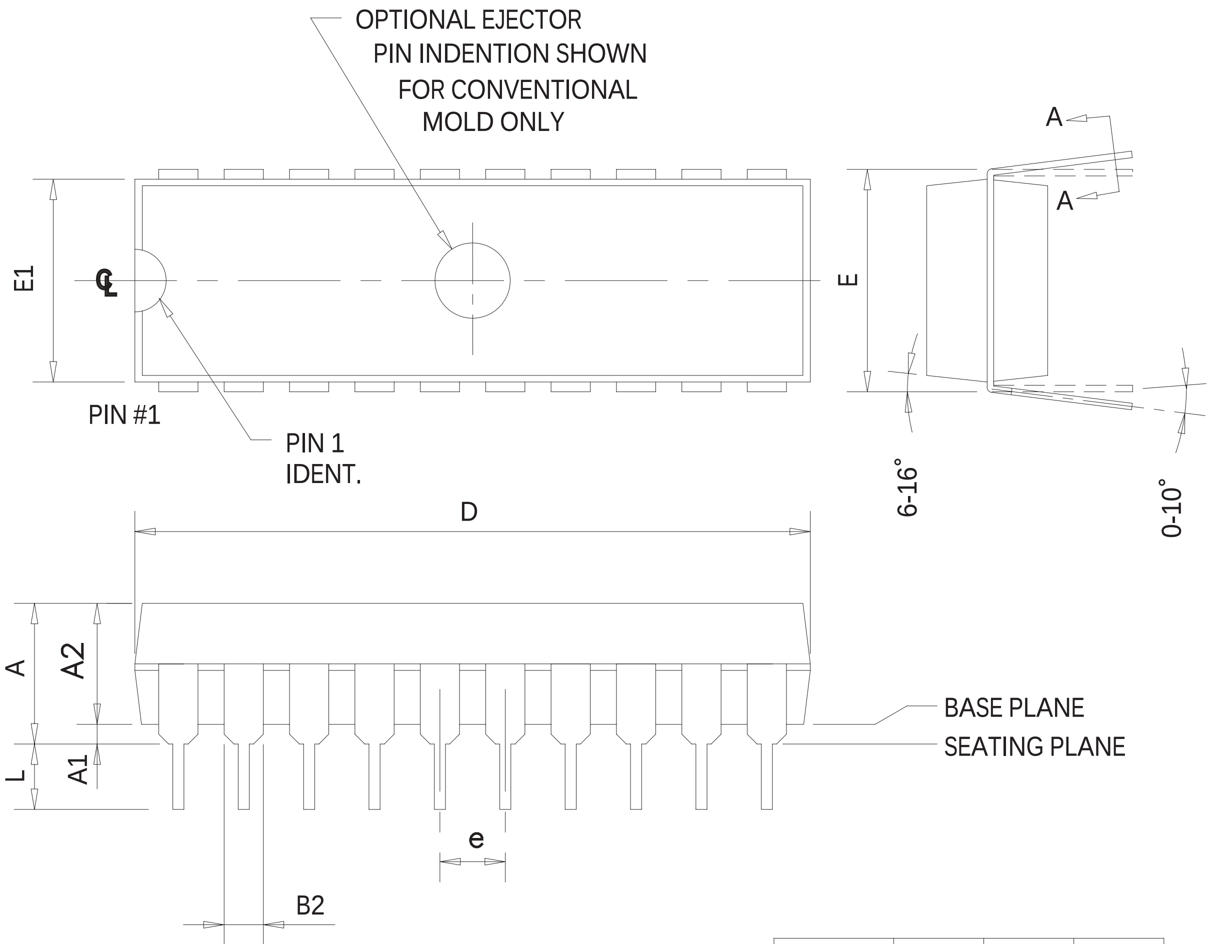


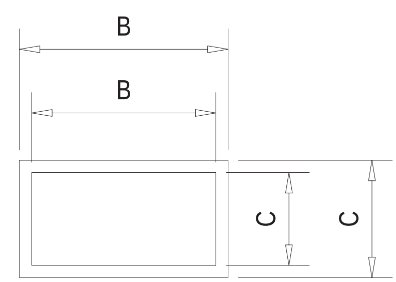
SECTION A-A

SYMBOL	MIN.	NOM.	MAX.
A	-	-	.175
A1	0.015	-	-
A2	0.115	0.130	0.195
B	0.014	-	0.022
B1	0.014	0.018	0.020
B2	0.550	0.600	0.650
C	0.008	-	0.014
C1	0.008	0.010	0.012
D	0.740	0.750	0.760
E	0.295	0.310	0.325
E1	0.240	0.250	0.260
e	0.100 BSC.		
L	0.125	-	0.150

ALL DIMENSIONS ARE IN INCHES

PACKAGE B



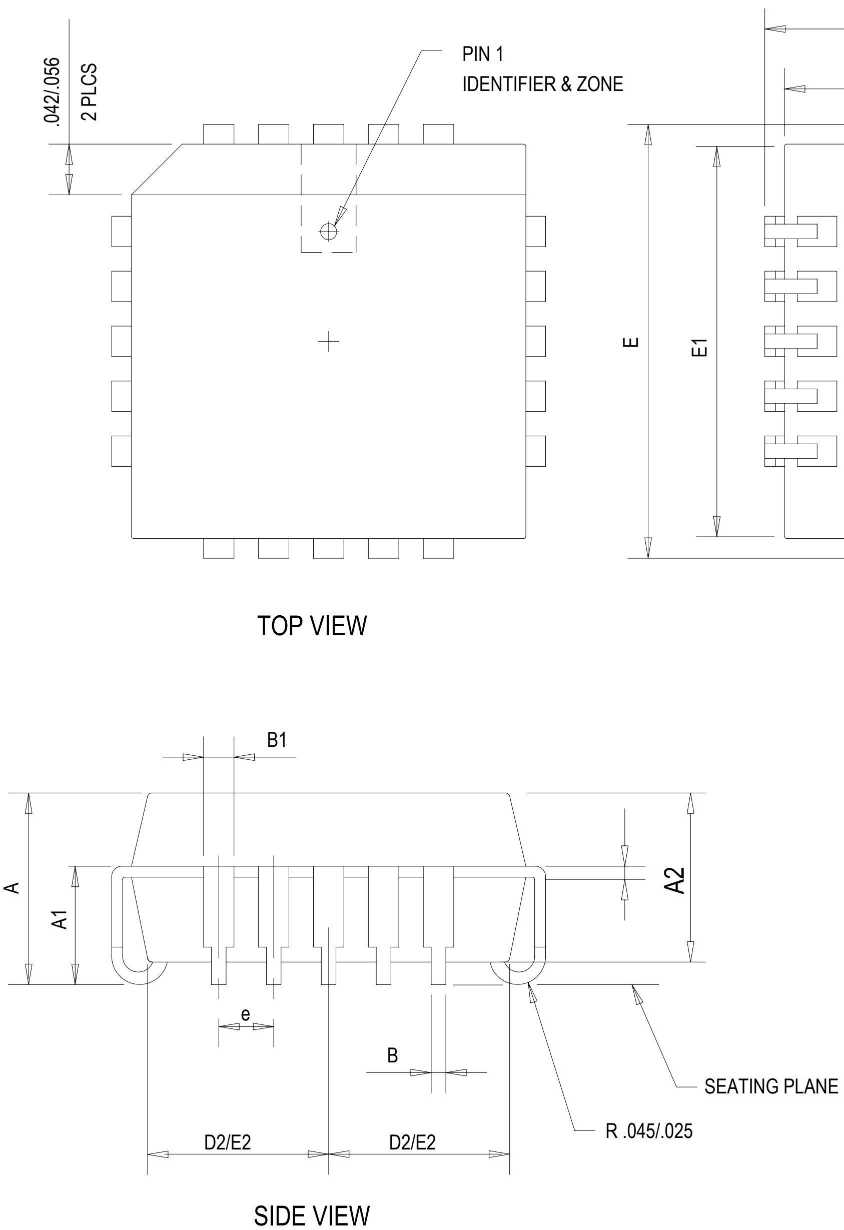


SECTION A-A

SYMBOL	MIN.	NOM.	MAX.
A	-	-	.175
A1	0.015	-	-
A2	0.115	0.130	0.195
B	0.014	-	0.022
B1	0.014	0.018	0.020
B2	0.550	0.600	0.650
C	0.008	-	0.014
C1	0.008	0.010	0.012
D	1.010	1.030	1.035
E	0.295	0.310	0.325
E1	0.240	0.250	0.260
e	0.100 BSC.		
L	0.125	-	0.150

ALL DIMENSIONS ARE IN INCHES

PACKAGE C



SYMBOL	MIN	NOM	MAX
A	0.165	0.172	0.180
A1	0.090	0.105	0.120
A2	0.146	0.152	0.156
B	0.013	0.017	0.021
B1	0.026	0.029	0.032
C	0.008	0.010	0.012
D	0.385	0.390	0.395
D1	0.350	0.352	0.355
D2	0.145	0.160	0.165
E	0.385	0.390	0.395
E1	0.350	0.352	0.355
E2	0.145	0.160	0.165
e	0.050 REF.		

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For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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