Application Diagram

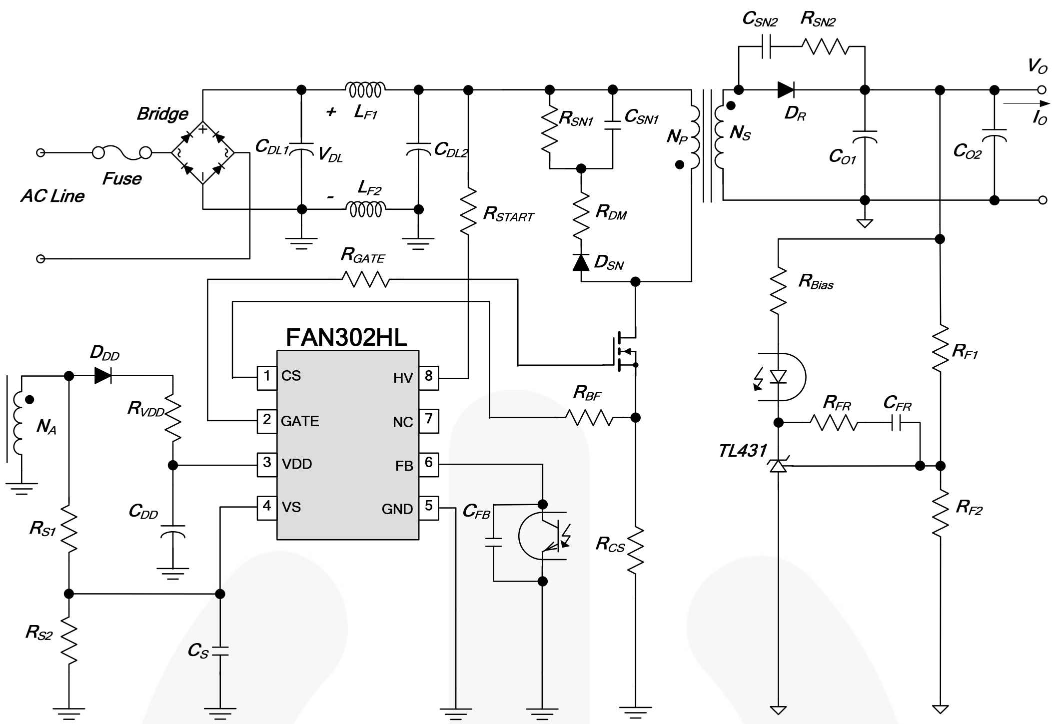


Figure 2. Typical Application

Internal Block Diagram

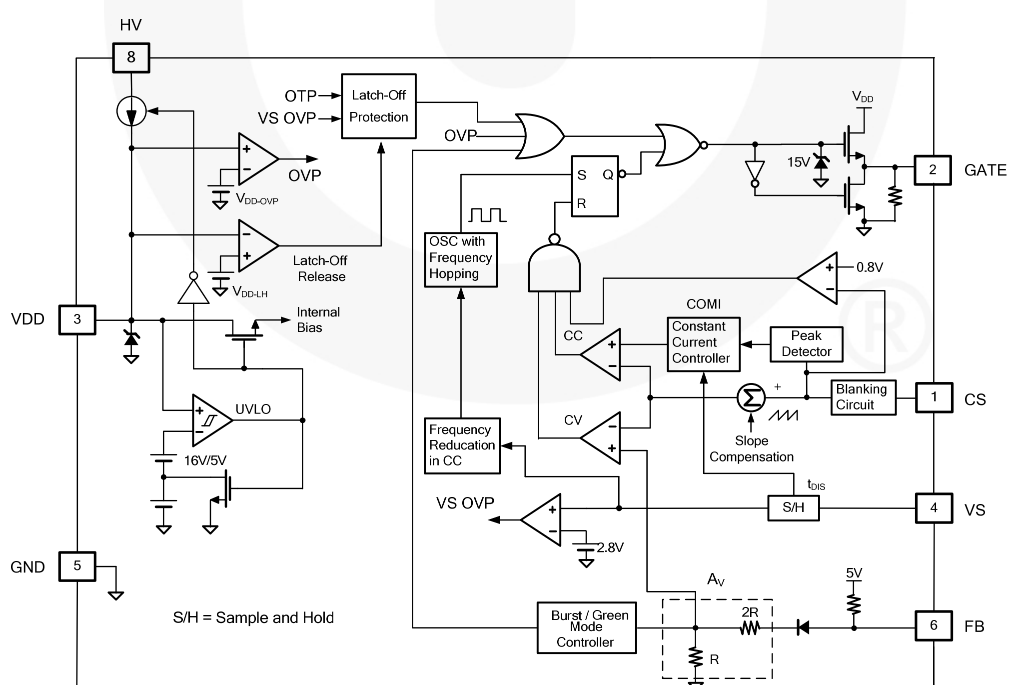
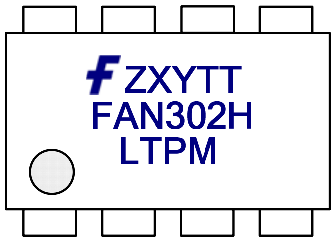


Figure 3. Functional Block Diagram

Marking Information



F- Fairchild Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: M=SOP
P: Y= Green Package
M: Manufacture Flow Code

Figure 4.Top Mark

Pin Configuration

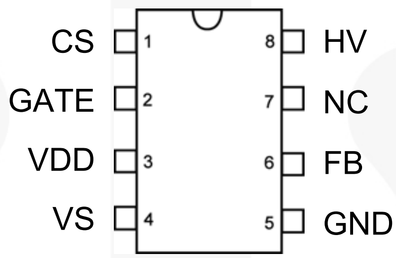


Figure 5. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current-sense resistor to detect the MOSFET current for Peak-Current-Mode control in CV regulation and provides the output-current regulation in CC regulation.
2	GATE	**PWM Signal Output**. This pin uses the internal totem-pole output driver to drive the power MOSFET. It is internally clamped below 15V.
3	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external V_{DD} capacitor. The threshold voltages for startup and turn-off are 16V and 5V, respectively.
4	VS	**Voltage Sense**. This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.
5	GND	**Ground**
6	FB	**Feedback**. The FB pin provides feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.
7	NC	**No Connect**
8	HV	**High Voltage**. This pin connects to bulk capacitor for high-voltage startup.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage[1,2]			30	V
V_{VS}	VS Pin Input Voltage		-0.3	7.0	V
V_{CS}	CS Pin Input Voltage		-0.3	7.0	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
P_D	Power Dissipation (T_A=25°C)			660	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			150	°C/W
Θ_{JC}	Thermal Resistance (Junction-to-Case)			39	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature, (Wave soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114 (Except HV Pin)[3]		5.0	kV
		Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)[3]		1.5	

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD ratings including HV pin: HBM=400V, CDM=750V.

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
HV Section							
V_{HV-MIN}	Minimum Startup Voltage on HV Pin					50	V
I_{HV}	Supply Current Drawn from HV Pin		V_{AC}=90V, V_{DD}=0V, Controller Off	0.8	1.5	5.0	mA
I_{HV-LC}	Leakage Current Drawn from HV Pin		With Auxiliary Supply, V_{HV}=500V, V_{DD}=15V, Controller On		0.8	3.0	μA
V_{DD} Section							
V_{OP}	Continuously Operation Voltage					25	V
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage			4.7	5.0	5.3	V
V_{DD-LH}	Threshold Voltage for Latch-Off Release				2.50		V
I_{DD-ST}	Startup Current		V_{DD}=V_{DD-ON} – 0.16V		400	450	μA
I_{DD-OP}	Operating Supply Current		V_{DD}=18V, f=f_{OSC}, C_L=1nF		3.5	4.0	mA
$I_{DD-BURST}$	Burst-Mode Operating Supply Current		V_{DD}=8V, C_L=1nF		200	350	μA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level		Auto-Restart	25.5	26.5	27.5	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		f=85kHz		100	180	μs
Oscillator Section							
f_{OSC}	Frequency	Center Frequency	V_{CS}=5V, V_S=2.5, V_{FB}=5V	82	85	88	kHz
		Hopping Range			±3		
t_{FHR}	Frequency Hopping Period				2.84		ms
$f_{OSC-CM-MIN}$	Minimum Frequency if CCM (Continuous Current Mode)			13	18	23	kHz
$f_{OSC-CCM}$	Minimum Frequency in CC Regulation (Constant Current Regulation)		V_{CS}=5V, V_S=0V	23	26	29	kHz
Feedback Input Section							
A_V	FB Input to Current Comparator Attenuation			1/3.5	1/3.0	1/2.5	V/V
Z_{FB}	Input Impedance			38	42	44	kΩ
$V_{FB-OPEN}$	Output High Voltage		FB Pin Open		5.3		V
V_{FB-G}	Green Mode Ending Voltage			1.7	1.8	1.9	V
V_{FB-L}	Enter Zero Duty Cycle of FB Voltage		V_{CS}=5V, V_S=0V	1.2	1.4	1.6	V
V_{FB-H}	Leave Zero Duty Cycle of FB Voltage		V_{CS}=5V, V_S=0V	1.3	1.5	1.7	V
Over-Temperature Protection Section							
T_{OTP}	Threshold Temperature for Over-Temperature Protection			+130	+140	+150	°C

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15V and T_A=25°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voltage-Sense Section						
I_{TC}	Bias Current	V_{CS}=5V	8.75	10.00	11.25	µA
$V_{VS\text{-}CM\text{-}MIN}$	V_S Threshold Voltage of ZCD Undetectable Protection			0.55		V
$V_{VS\text{-}CM\text{-}MAX}$	V_S Threshold Voltage of ZCD Undetectable Protection			0.75		V
$V_{SN\text{-}CC}$	Starting Voltage of Frequency Decreasing of CC	V_{CS}=5V, f_{S1}=f_{OSC}-2KHz		2.15		V
$V_{SG\text{-}CC}$	Ending Voltage of Frequency Decreasing of CC	V_{CS}=5V, f_{S2}=f_{OSC}+2KHz		0.70		V
$S_{G\text{-}CC}$	Frequency Decreasing Slop of CC Regulation	$S_{G\text{-}CC}$= $(f_{S1}-f_{S2})/(V_{SN\text{-}CC}-V_{SG\text{-}CC})$	30	38	46	Hz/mV
$V_{VS\text{-}OFFSET}$	ZCD Turn-Off Threshold			200		mV
$V_{VS\text{-}OVP}$	Output Over-Voltage Protection		2.7	2.80	2.85	V
$t_{VS\text{-}OVP}$	Output Over-Voltage Protection Debounce Time	f=85kHz		100	180	µs
Current-Sense Section						
V_{VR}	Reference Voltage		2.475	2.500	2.525	V
V_{CCR}	Variation Test Voltage on CS Pin for Constant Current Output	V_{CS}=0.47V	2.405	2.430	2.455	V
V_{STH}	Threshold Voltage for Current Limit			0.8		V
$V_{STH\text{-}VA}$	Threshold Voltage for Current Limit at Power Mode ($V_{VS\text{-}CM\text{-}MAX}$ <0.75V)	V_{VS}=0.3V	0.25	0.30	0.35	V
t_{PD}	Propagation Delay to GATE Output			100	200	ns
t_{MIN}	Minimum On Time	V_{VS}=0V, V_{CS}=5V	430	530	630	ns
t_{LEB}	Leading-Edge Blanking Time		300	400	500	ns
V_{SLOPE}	Slope Compensation	Maximum Duty Cycle		0.3		V
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		64	67	70	%
$V_{GATE\text{-}L}$	Output Voltage Low	V_{DD}=25V, I_O=10mA			1.5	V
$V_{GATE\text{-}H}$	Output Voltage High	V_{DD}=8V, I_O=1mA	5		8	V
$V_{GATE\text{-}H}$	Output Voltage High	V_{DD}=5.5V, I_O=1mA	4.0		5.5	V
t_r	Rising Time	V_{DD}=15V, C_L=1nF	100	140	180	ns
t_f	Falling Time	V_{DD}=15V, C_L=1nF	30	50	70	ns
$V_{GATE\text{-}CLAMP}$	Output Clamp Voltage	V_{DD}=25V	13	15	17	V

Typical Performance Characteristics

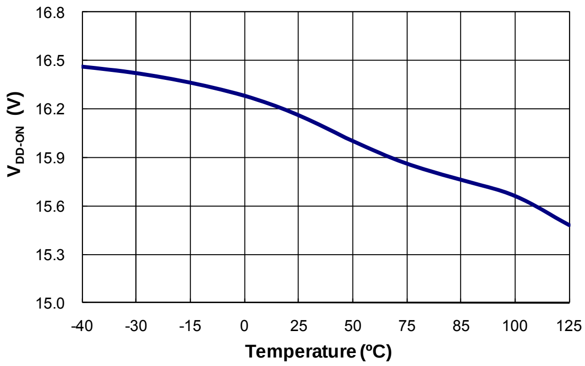


Figure 6. V_{DD} Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

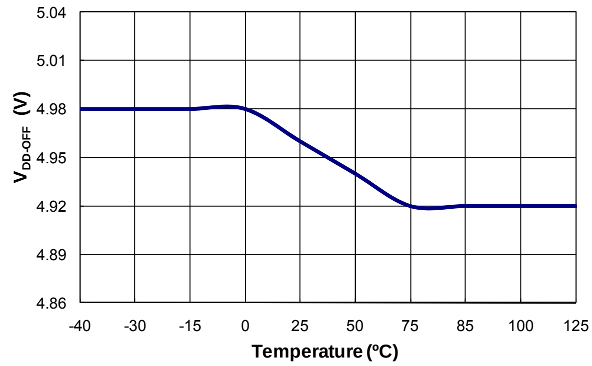


Figure 7. V_{DD} Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

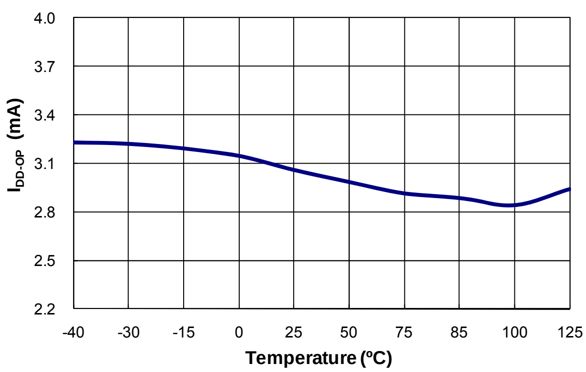


Figure 8. Operating Current (I_{DD-OP}) vs. Temperature

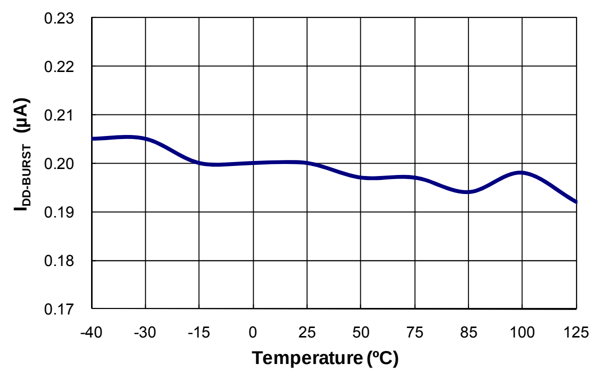


Figure 9. Burst Mode Operating Current ($I_{DD-BURST}$) vs. Temperature

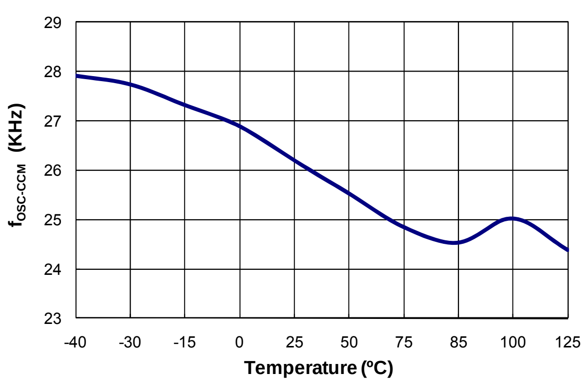


Figure 10. CC Regulation Minimum Frequency ($f_{OSC-CCM}$) vs. Temperature

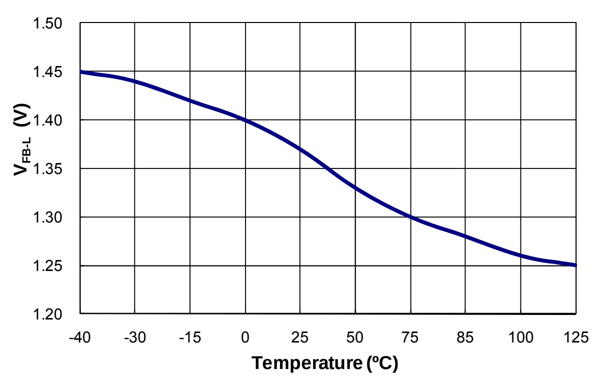


Figure 11. Enter Zero Duty Cycle of FB Voltage (V_{FB-L}) vs. Temperature

Typical Performance Characteristics

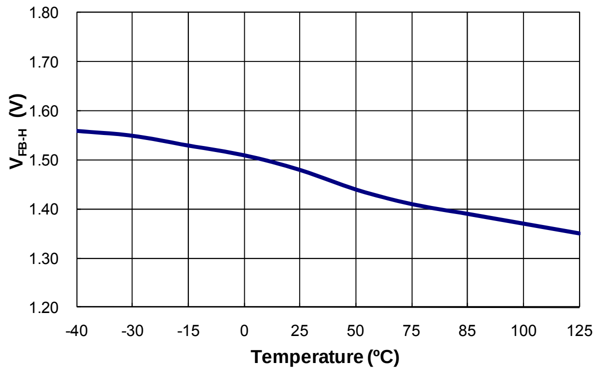


Figure 12. Leave Zero Duty Cycle of FB Voltage (V_{FB-H}) vs. Temperature

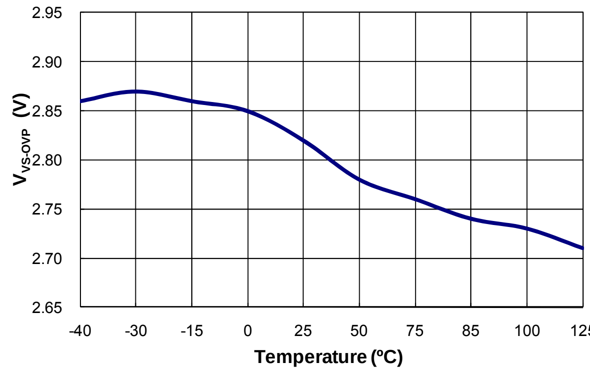


Figure 13. V_S Over-Voltage Protection (V_{VS-OVP}) vs. Temperature

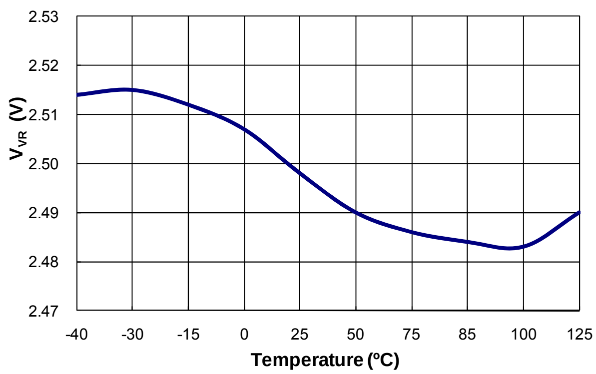


Figure 14. Reference Voltage of CS (V_{VR}) vs. Temperature

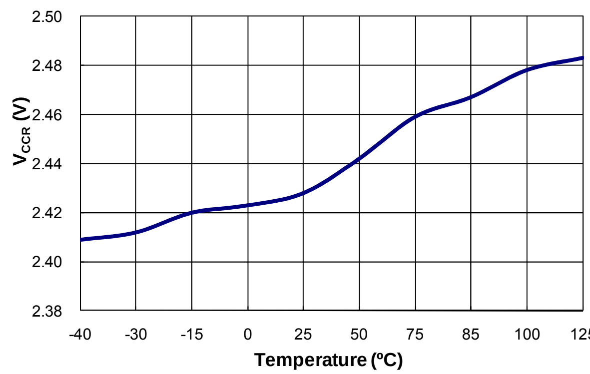


Figure 15.Variation Voltage on CS Pin for Constant-Current Regulation (V_{CCR}) vs. Temperature

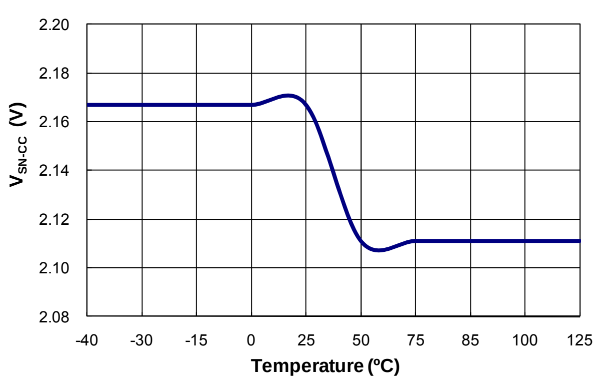


Figure 16. Starting Voltage of Frequency Decreasing of CC Regulation (V_{SN-CC}) vs. Temperature

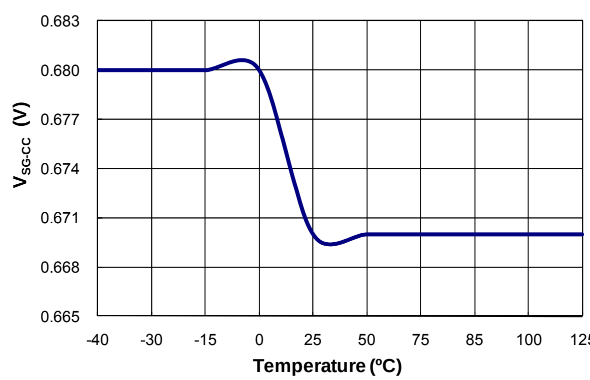


Figure 17. Ending Voltage of Frequency Decreasing of CC Regulation (V_{SG-CC}) vs. Temperature

Typical Performance Characteristics

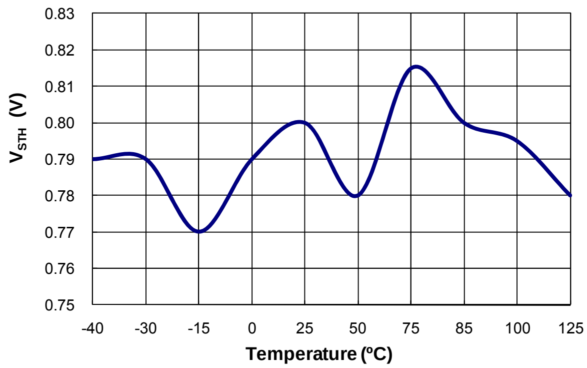


Figure 18. Threshold Voltage for Current Limit (V_{STH}) vs. Temperature

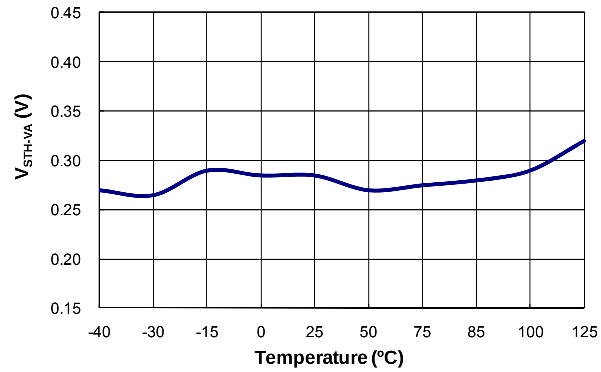


Figure 19. Threshold Voltage for Current Limit at Power Mode (V_{STH-VA}) vs. Temperature

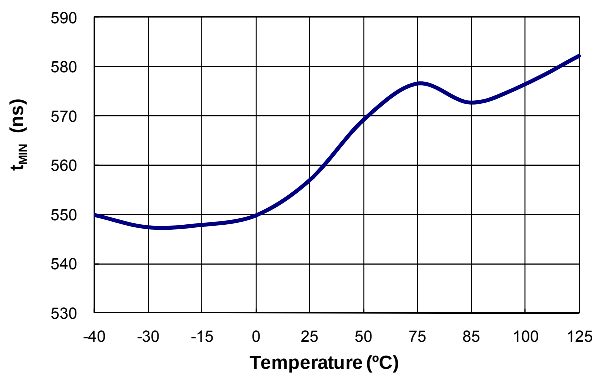


Figure 20. Minimum On Time (t_{MIN}) vs. Temperature

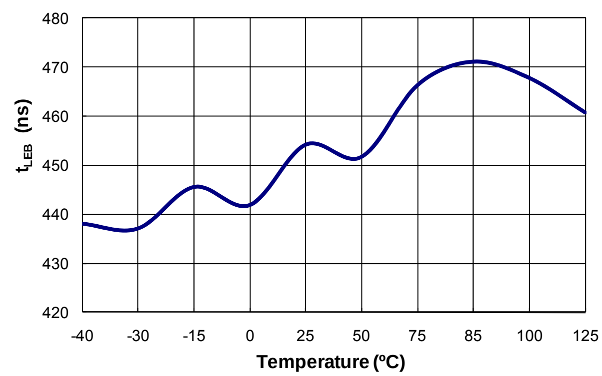


Figure 21.Leading-Edge Blanking Time (t_{LEB}) vs. Temperature

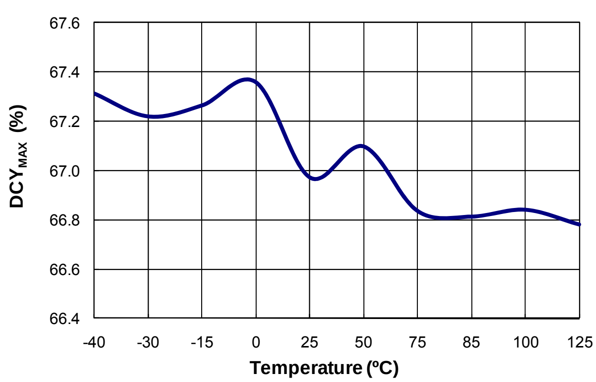


Figure 22. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

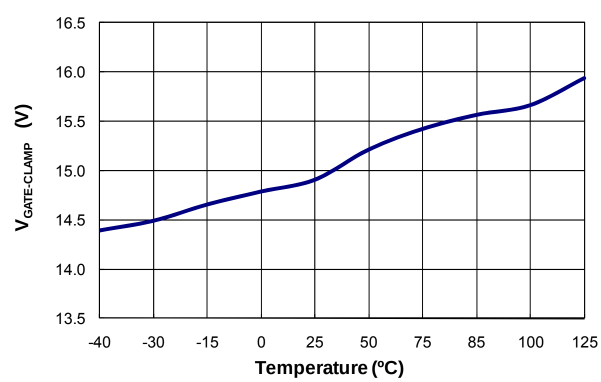


Figure 23. Gate Output Clamp Voltage ($V_{GATE-CLAMP}$) vs. Temperature

Operation Description

Constant-Voltage Regulation Operation

FAN302HL is the high-frequency and ultra-low standby power IC with Constant Voltage (CV) / Constant Current (CC) regulation.

When FAN302HL operates in CV regulation, the feedback voltage (V_{FB}) works as output load and modulates the PWM duty, as shown in Figure 24, causing fixed switching frequency (85kHz). Once the V_{FB} decreases below $V_{FB\text{-}G}$, frequency hopping is disabled and operation current decreases.

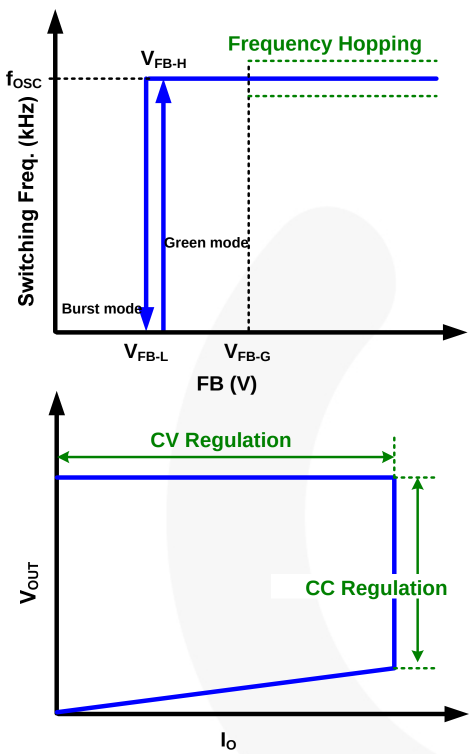


Figure 24. f_{OSC} vs. V_{FB} in CV Regulation

Constant-Current Regulation Operation

During CC operation, the proprietary Primary-Side Regulation (PSR) topology simplifies circuit design without secondary feedback circuitry for battery-charger applications. The CC regulation achieved through PSR technique uses a mixed-signal algorithm to detect the primary-side current and to sample the voltage through primary-side auxiliary winding and calculate the average current on secondary side.

Figure 25 shows the basic circuit diagram of a flyback converter, with typical waveforms shown in Figure 26. Generally, Discontinuous Conduction Mode (DCM) operation is preferred for constant-current control since it allows better output regulation. The operation principles of DCM flyback converter are:

During the MOSFET on time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then, MOSFET current (I_{ds}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.

When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. While the diode is conducting, the output voltage (V_O), together with diode forward voltage drop (V_F), are applied across the secondary-side inductor ($L_m \times N_s^2/N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($I_p k \times N_p/N_s$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

When the diode current reaches zero, V_S voltage drops quickly: if it is greater than the $V_{VS\text{-}OFFSET}$ drop voltage, the IC gets the t_{DIS} for CC regulation.

During the inductor current discharge time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as $(V_O+V_F) \times N_a/N_S$. This voltage signal is proportional to the secondary winding. In constant-current output operation, this voltage signal is detected and examined by the precise constant-current regulation controller. The on time of the MOSFET is determined to control input power and provide constant-current output property. With feedback voltage V_{CS} across the current-sense resistor, the controller can obtain the input power of power supply. Therefore, the region of constant-current output operation can be adjusted by the current-sense resistor, as shown in Equation (1).

$$I_O = \frac{1}{2} \cdot i_{PK} \cdot \frac{N_P}{N_S} \cdot \frac{t_{DIS}}{t_s} = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot \frac{V_{CS}}{R_{CS}} \cdot \frac{t_{DIS}}{t_s} \qquad (1)$$

During CC regulation, the V_S voltage decreases as output voltage decreases. The switching frequency reduces linearly from f_{OSC} to $f_{OSC\text{-}CCM}$ as V_S voltage changes from $V_{SN\text{-}CC}$ to $V_{SG\text{-}CC}$. Figure 27 shows the relationship between frequency and V_S voltage. Figure 28 shows the output V-I curve and V_S voltage.

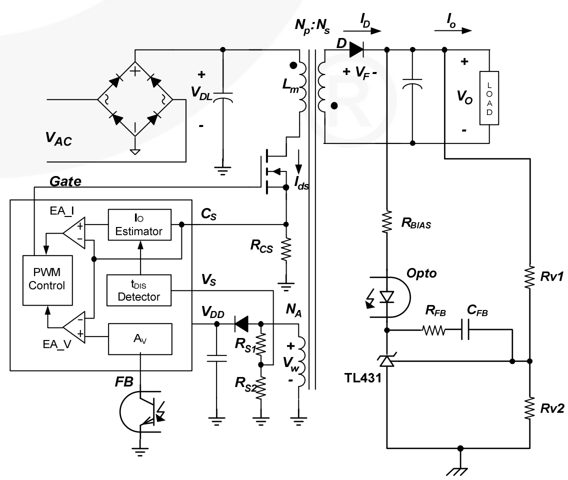


Figure 25. Simplified Flyback Converter Circuit

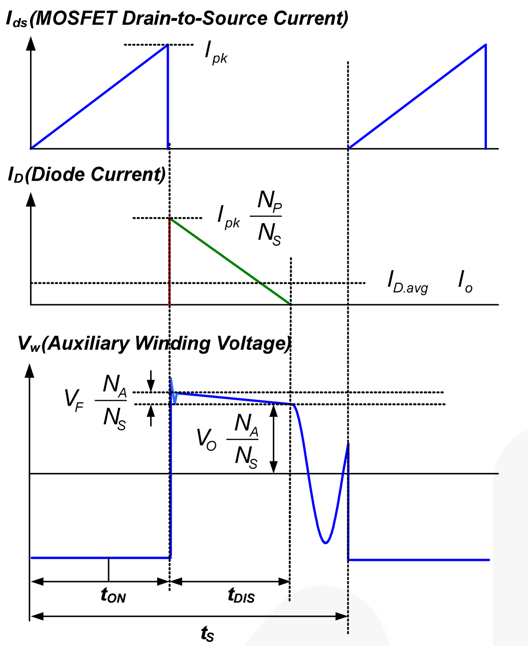


Figure 26. Waveforms of DCM Flyback Converter

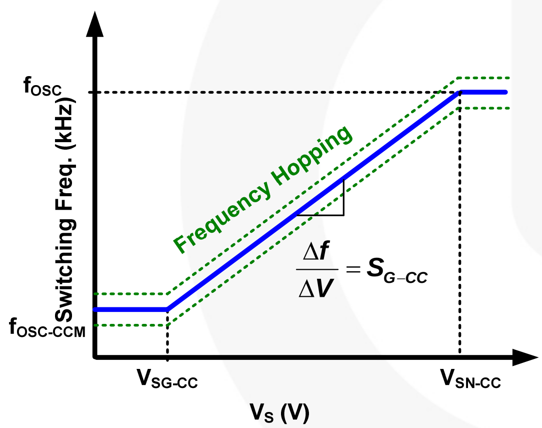


Figure 27. Frequency Reduction Curve in CC Regulation

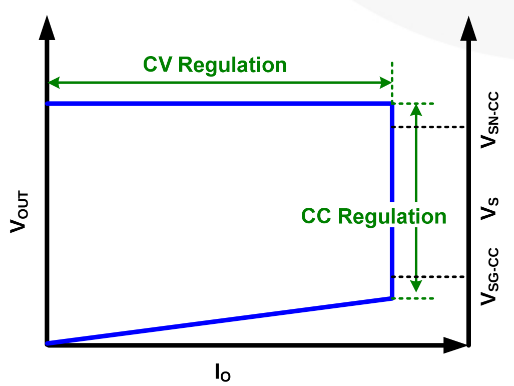


Figure 28. Output V-I Curve and V_S Voltage

High-Voltage Startup

Figure 29 shows the high-voltage (HV) startup circuit for FAN302HL applications. The HV pin is connected to the line input or bulk capacitor through a resistor. During startup, the internal startup circuit is enabled and the line input supplies the current, I_{HV}, to charge the hold-up capacitor, C_{VDD}, through R_{START}. When the V_{DD} voltage reaches $V_{DD\text{-}ON}$, the internal HV startup circuit is disabled, blocking I_{HV} from flowing into the HV pin. Once the IC turns on, C_{VDD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Therefore, C_{VDD} must be large enough to prevent V_{DD} from dropping to $V_{DD\text{-}OFF}$ before the power can be delivered from the auxiliary winding.

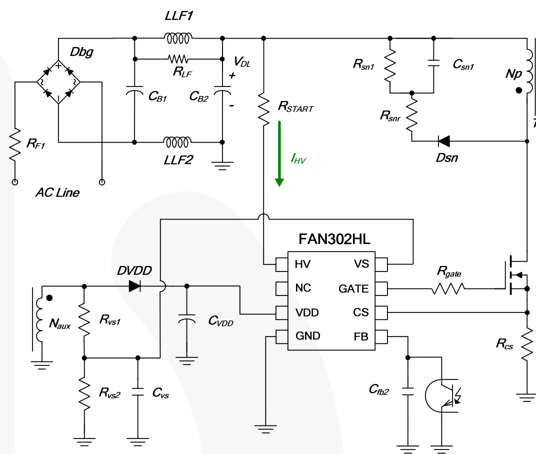


Figure 29. HV Startup Circuit

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. The FAN302HL internal frequency-hopping circuit changes the switching frequency between 82kHz and 88kHz with a period, as shown in Figure 30.

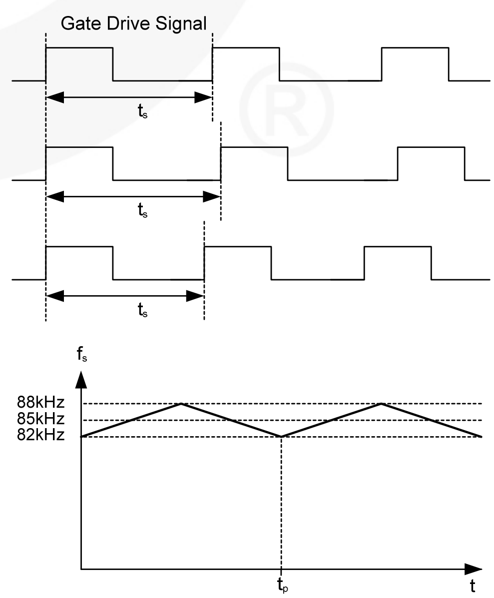


Figure 30. Frequency Hopping

Burst-Mode Operation

The power supply enters “Burst-Mode” at no-load conditions. As shown in Figure 31, when V_{FB} drops below V_{FBL}, the PWM output shuts off and the output voltage drops at a rate dependent on load current. This causes the feedback voltage to rise. Once V_{FB} exceeds V_{FBH}, the internal circuit starts to provide switching pulse. The feedback voltage then falls and the process repeats. Burst Mode operation alternately enables and disables switching of the MOSFET, reducing the switching losses in Standby Mode.

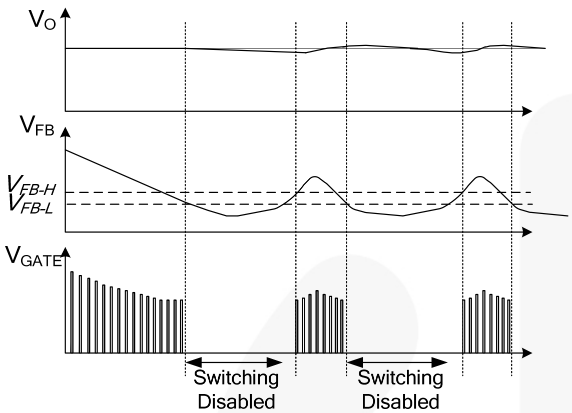


Figure 31. Burst-Mode Operation

Operating Current

The typical operating current is 3.5mA. This low operating current results in higher efficiency and reduces the V_{DD} hold-up capacitance requirement. Once FAN302HL enters Burst Mode, the operating current is reduced to 200µA, allowing the power supply to meet power conservation requirements.

Gate Output

The FAN302HL BiCMOS output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal Zener diode to protect the power MOSFET transistors against over-voltage gate signals.

Slope Compensation

The sensed voltage across the current-sense resistor is used for Current-Mode control and pulse-by-pulse current limiting. Built-in slope compensation, a synchronized positively-sloped ramp built-in at each switching cycle, improves stability and prevents sub-harmonic oscillations due to Peak-Current Mode control.

Constant Power Mode Control

When V_S is lower than $V_{S\text{-}CM\text{-}MIN}$, FAN302HL enters Constant-Power-Mode control, the primary-side current limit voltage (V_{CS}) changes from V_{STH} to $V_{STH\text{-}VA}$ to avoid mis-sampling V_S through the Zero Current Detection (ZCD). Once V_S is higher than $V_{S\text{-}CM\text{-}MAX}$, the V_{CS} returns to V_{STH}.

Protections

The FAN302HL self-protection functions include V_{DD} Over-Voltage Protection (V_{DD} OVP), internal Over-Temperature Protection (OTP), V_S Over-Voltage Protection (V_S OVP), brownout protection, and pulse-by-pulse current limit.

The V_{DD} OVP protection is implemented as Auto-Restart Mode. Once an abnormal condition occurs, switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5V, the internal startup circuit is enabled, and the supply current drawn from HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 16V, FAN302HL resumes normal operation. In this manner, the auto-restart alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated (*see Figure 32*).

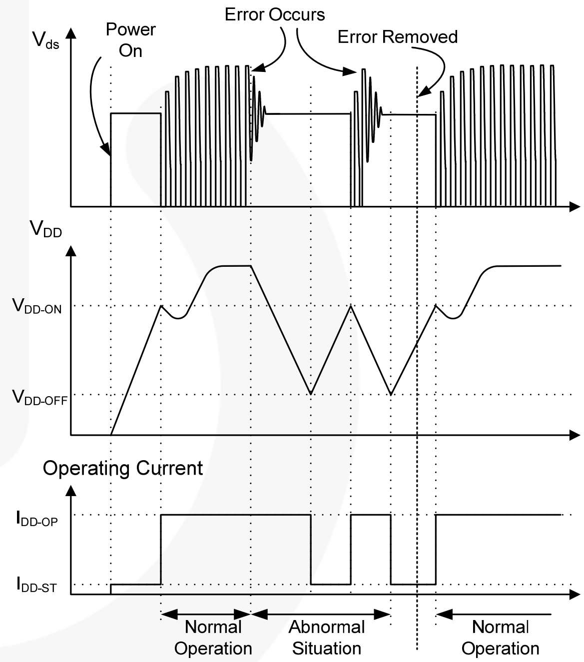


Figure 32. Auto-Restart Mode Operation

The V_S OVP and internal OTP protections are implemented as Latch Mode. If abnormal conditions occur, PWM switching is terminated and the MOSFET remains off. In this scenario, V_{DD} drops, but keeps working as auto-restart (V_{DD} auto-restart behavior doesn’t trigger PWM pulses). FAN302HL enters Latch Mode, disables PWM switching of the MOSFET until V_{DD} is lower than $V_{DD\text{-}LH}$ (AC power is removed), powers on again, then resumes normal operation (*see Figure 33*).

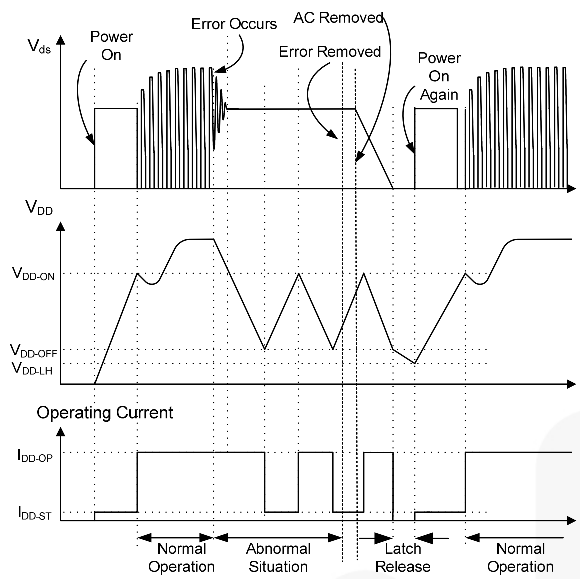


Figure 33. Latch-Mode Operation

V_S Over-Voltage Protection (OVP)

V_S over-voltage protection prevents damage due to output over-voltage conditions. Figure 34 shows the V_S OVP protection method. When abnormal system conditions occur that cause V_S to exceed 2.8V, after a period of debounce time; PWM pulses are disabled and FAN302HL enters Latch Mode until V_{DD} drops to under V_{DD-LH}. By that time, PWM pulses revive. V_S over-voltage conditions are usually caused by open feedback loops or abnormal behavior by the VS pin divider resistor.

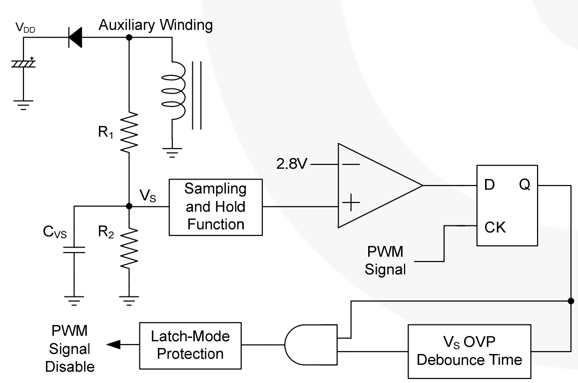


Figure 34. V_S OVP Protection

V_{DD} Over-Voltage Clamping

V_{DD} over-voltage protection prevents damage due to over-voltage conditions. When the V_{DD} voltage exceeds 26.5V due to abnormal conditions, PWM pulses are disabled until the V_{DD} voltage drops below the UVLO, then starts again. Over-voltage conditions are usually caused by open feedback loops.

Over-Temperature Protection (OTP)

The FAN302HL temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C (T_{OTP}). The PWM pulses are disabled until V_{DD} voltage drops below the V_{DD-LH}.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a 350ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16V and 5V, respectively. During startup, the hold-up capacitor must be charged to 16V through the startup resistor to enable the FAN302HL. The hold-up capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} must not drop below 5V during this startup process. This UVLO hysteresis window ensures that the hold-up capacitor is adequate to supply V_{DD} during startup.

Noise Immunity

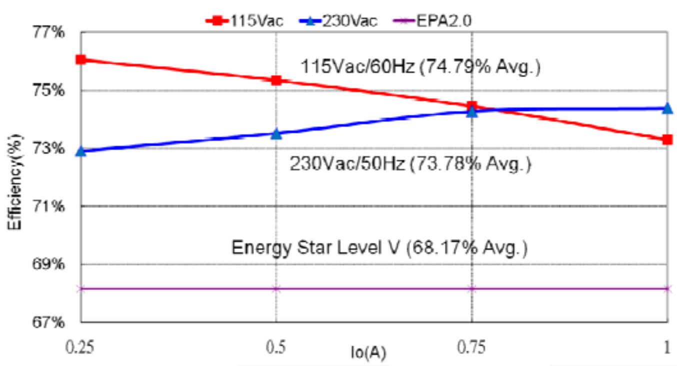
Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in Continuous-Conduction Mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FAN302HL, and increasing the power MOS gate resistance are advised.

Typical Application Circuit (Flyback Charger)

Application	Fairchild Devices	Input Voltage Range	Output
Cell Phone Charger	FAN302HL	90~265V_{AC}	5V/1.2A (6W)

Features

- High Efficiency (Avg. >71%), Meeting Energy Star V2.0 Standard (Avg. 68.17%)
- Ultra-Low Standby Power: Under 10mW at 230V_{AC} (Pin=6.3mW for 115V_{AC} and Pin=7.3mW for 230V_{AC})
- Output Regulation (CV: ±5%, CC: ±15%)



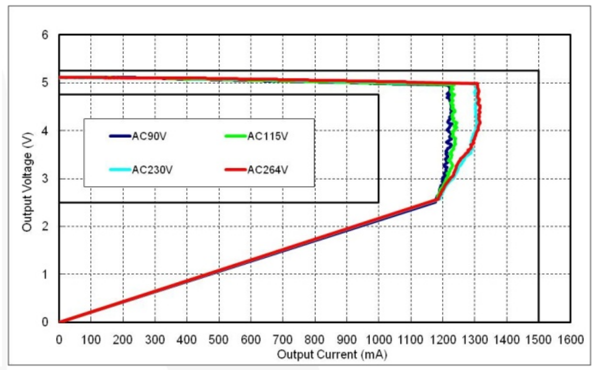


Figure 35. Measured Efficiency and Output Regulation

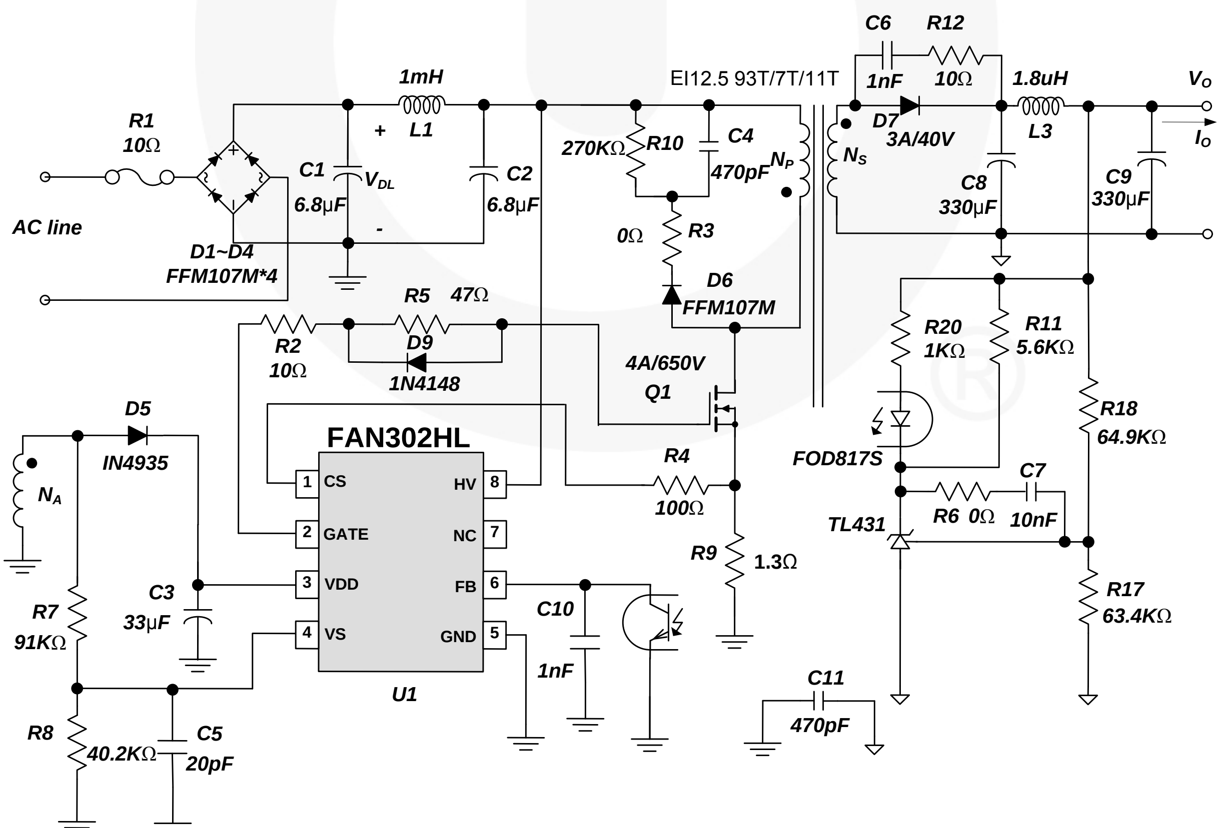


Figure 36. Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EI12.5
- Bobbin: EI12.5

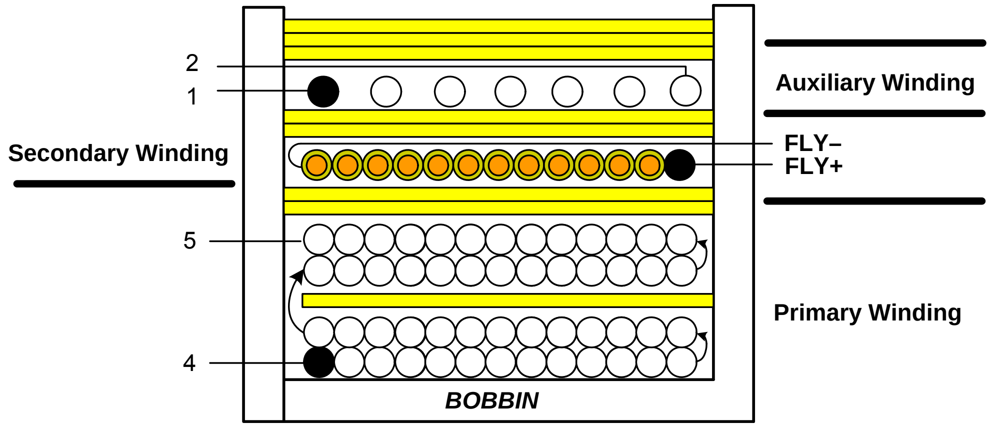


Figure 37.Transformer

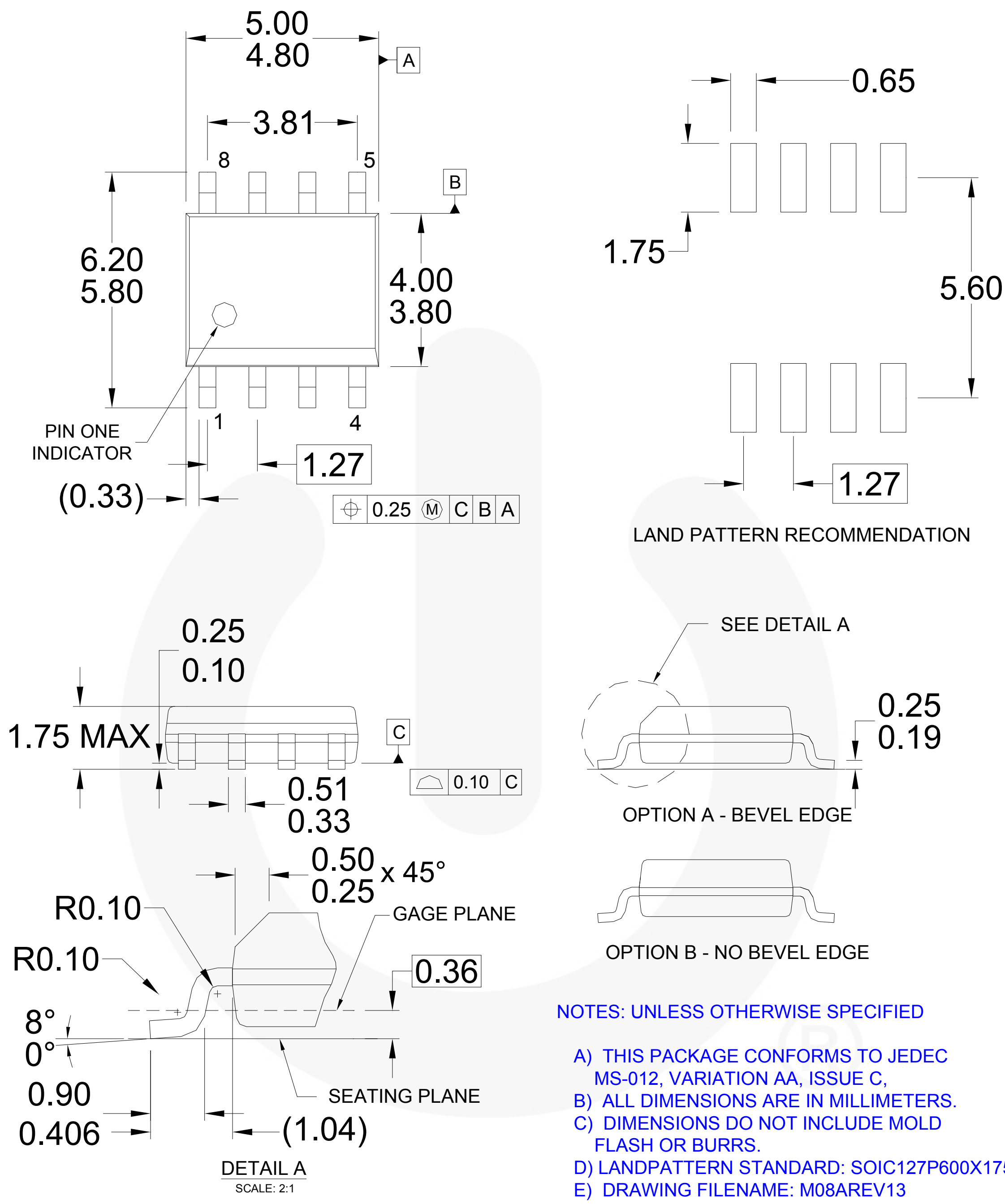
- W1 is four winds; for each wind of turns, refer to Table 1. Add one insulating tape layer between the first and second layers.
- W2 is wound two layers and uses triple-insulated wire: end of positive fly line is 3.5cm, layer end of negative fly line is 2.5cm.
- W3 is spares winding in one layer.
- W4 is wound in the core of the outermost layer and sparse winding.

Table 1. Transformer Turns Specifications

NO	Terminal		Wire	Turns	Insulation
	Start Pin	End Pin			Turns
W1	4	5	2UEW 0.1*1	26	0
				25	1
				24	0
				18	2
W2	Fly+	Fly-	TEX-E 0.45*1	7	2
W3	1	2	2UEW 0.18*1	11	2
			CORE ROUNDING TAPE		3
			CORE		0
W4	2		2UEW 0.18*1	5	2

	Pin	Specifications	Remark
Primary-Side Inductance	4 – 5	700μH ±7%	100kHz, 1V
Primary-Side Effective Leakage	4 – 5	200μH ±5%	Short one of the secondary windings.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 38. 8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch, Narrow Body

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TINYOPTO™
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Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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