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1

Test and application circuit, block diagram

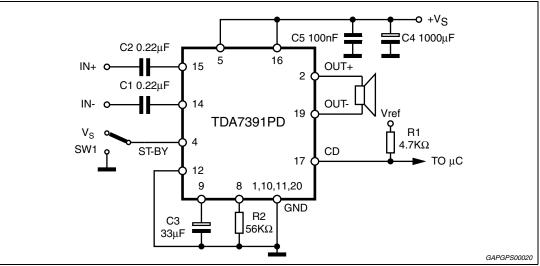
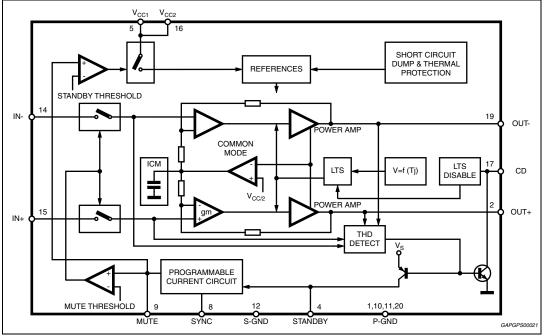


Figure 1. Test and application circuit







2 Pins description

Figure 3. Pins connection (top view)

Table 2. Pins function

Pin	Function	Description
14, 15	INPUTS	The input stage is a high impedance type also capable of operation in single ended mode with one input capacitively coupled to the signal GND. The impedance seen by the inverting and non inverting input pins must be matched.
5, 16	+V _S	Supply voltage.
17	CD	The TDA7391PD is equipped with a diagnostic circuitry able to detect the clipping in the Output Signal (distortion = 10%). The CD pin (open collector) gives out low level signal during clipping.
2, 19	OUTPUTS	The output stage is a bridge type able to drive loads as low as 3.2Ω. It consists of two class AB fully complementary PNP/NPN stages fully protected. A rail to rail output voltage swing is achieved without need of bootstrap capacitors. No external compensation is necessary.
1, 10, 11, 20	GND	Power Ground.
12	S-GND	Signal ground.
4	STAND-BY	The device features a ST-BY function which shuts down all the internal bias supplies when the ST-BY pin is low. In ST-BY mode the amplifier sinks a small current (in the range of few μ A). When the ST-BY pin is high the IC becomes fully operational.
8	SYNC	A resistor (R_2) has to be connect between pin 8 and GND in order to program the current that flows in the C_3 capacitor (pin 9). The values of C_3 and R_2 determine the time required to bias the amplifier.
9	MUTE	The pin will have a capacitor (C_3) tied to GND to set the MUTE/STAND-BY time. An automatic Mute during turn on/off is provided to prevent noisy transients.



3 Electrical specifications

3.1 Absolute maximum ratings

Table 3.Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _S	DC supply voltage	28	V	
V _{OP}	Operating supply voltage	18	V	
V _{PEAK}	Peak supply voltage (t = 50 ms)	50	V	
	Output peak current repetitive (f > 10 Hz)	4.5	А	
Ι _Ο	Output peak current non repetitive	6	А	
P _{tot}	Power dissipation (T _{case} = 85 °C)	32	W	
T _{stg} , T _j	Storage and junction temperature	-40 to 150	°C	

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R _{th j-case}	Thermal resistance junction-to-case Max.	2	°C/W

3.3 Electrical characteristics

 V_S = 14.4 V; R_L = 4 $\Omega,$ f = 1 kHz, T_{amb} = 25 °C, unless otherwise specified.

Table 5.Electrical characteristics

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _S	Supply voltage range	-	8	-	18	V
Ι _q	Total quiescent current	-	-	60	150	mA
V _{OS}	Output offset voltage	-	-	-	120	mV
I _{SB}	Standby current	V _{ST-BY} = 1.5 V	-	-	100	μA
I _{SBin}	Standby input Bias current	V _{ST-BY} = 5 V	-	-	10	μA
V _{SBon}	Standby on threshold voltage	-	-	-	1.5	V
V _{SBoff}	Standby off threshold voltage	-	3.5	-	-	V
ATT _{Standby}	Standby attenuation	-	-	90	-	dB
I _{M in}	Mute input bias current	(V _{MUTE} = 5 V)	-	-	10	μA
A _M	Mute attenuation	-	-	90	-	dB



Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
		d = 10 %	20	26	-	W
Po	Output power	d = 1 %	-	21	-	W
		d = 10 %; $R_L = 3.2 \Omega$	-	32	-	W
P _{O EIAJ}	EIAJ output power (*)	V _S = 13.7 V	-	40	-	W
d	Distortion	-	-	0.06	-	%
u	Distortion	P _O = 0.1 to 15 W	-	0.03	-	%
G _V	Voltage gain	-	29.5	30	30.5	dB
f _H	High frequency rolloff	P _O = 1 W; -3 dB	75	-	-	kHz
D	Input Impedance	Differential	36	60	-	kΩ
R _{IN}		Single Ended	30	55	-	kΩ
E _{IN}	Input noise voltage	$R_g = 0 \Omega$; f = 22 Hz to 22 kHz	-	4	-	mV
CMRR	Input common mode rejection	f = 1 kHz; V _{IN} = 1 V _{rms}	-	65	-	dB
SVR	Supply voltage rejection	$R_g = 0 \Omega; V_r = 1 Vrms$	-	60	-	dB
CDL	Clipping detection level	-	-	10	-	%
T _{sd}	Absolute thermal shutdown junction temperature	-	-	160	-	°C

Table 5. Electrical characteristics (continued)

3.4 Electrical characteristics curves

Figure 4. Quiescent current vs. supply voltage

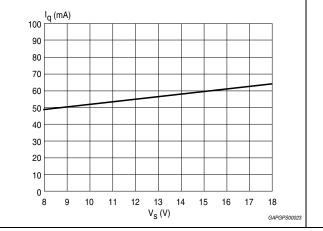


Figure 5. EIAJ power vs. supply voltage

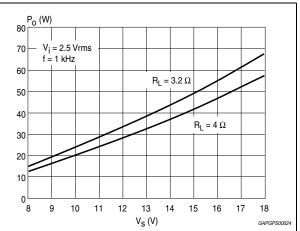
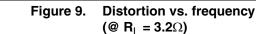




Figure 7. Distortion vs. frequency (@ $R_L = 4\Omega$)

45 Po (W) THD (%) 10 V_S = 14.4V 40 $R_L = 4 \ \Omega$ $R_L = 4\Omega$ f = 1 kHzP₀ = 12W 35 THD = 10% ĬIIIII 30 25 20 THD = 1% 0.1 15 10 TT 0 0.01 8 9 10 11 12 13 14 15 16 17 18 10000 100 10 1000 f = (Hz)Vs (V) GAPGPS00025 GAPGPS00026 Figure 8. Output power vs. supply voltage

Figure 6. Output power vs. supply voltage $(@R_L = 4\Omega)$



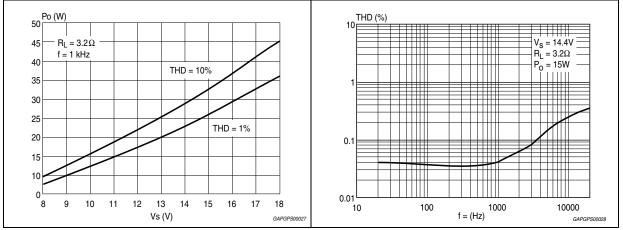
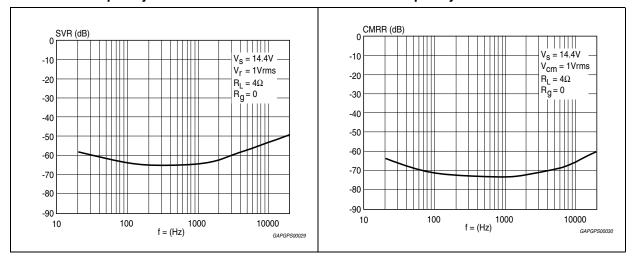


Figure 10. Supply voltage rejection vs. frequency

 $(@R_1 = 3.2\Omega)$

Figure 11. Common mode rejection vs. frequency





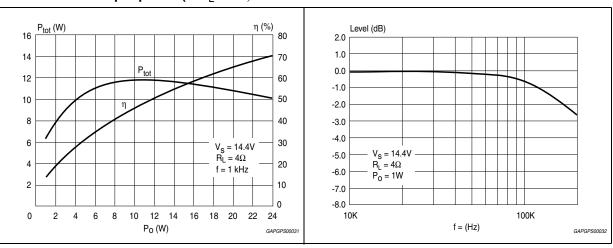


Figure 12. Total power dissipation and effic. vs. output power (@R_L = 4Ω)

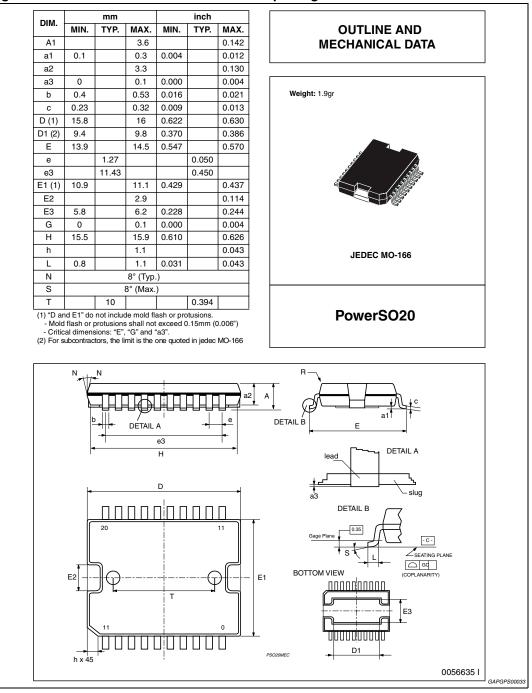
Figure 13. Power bandwidth



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: <u>www.st.com</u>.

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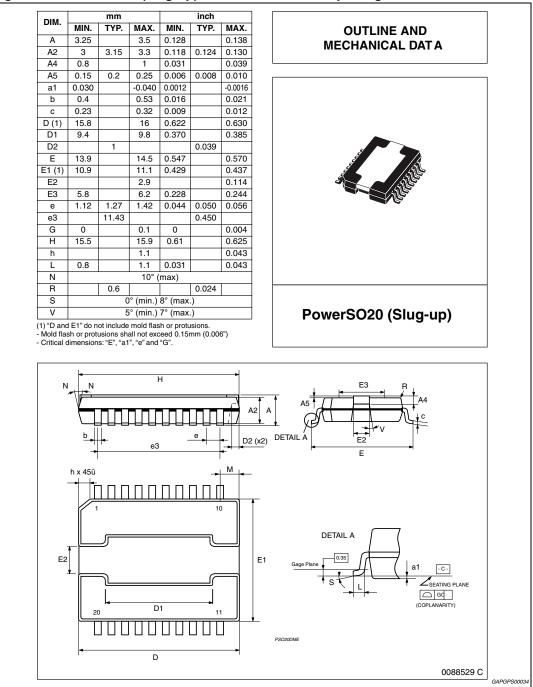


Figure 15. PowerSO20 (slug-up) mechanical data and package dimensions



5 Revision history

Table 6.	Document revision history
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Date	Revision	Changes
10-Oct-1998	1	Initial release.
02-Jul-2008	2	Document reformatted. Document status promoted from product preview to datasheet. Added <i>Table 1: Device summary</i> . Added ECOPACK description in <i>Section 5: Package information</i> .
19-Apr-2010	3	Updated Table 1: Device summary.
26-Jan-2011	4	Updated <i>Table 1: Device summary</i> . Added PowerSO20 (slug-up) drawing in <i>Figure 3</i> . Added PowerSO20 (slug-up) in <i>Section 4: Package information</i> .
16-Sep-2013	5	Updated Disclaimer.



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