

1 Characteristics

Figure 2. Pin configuration (top view)

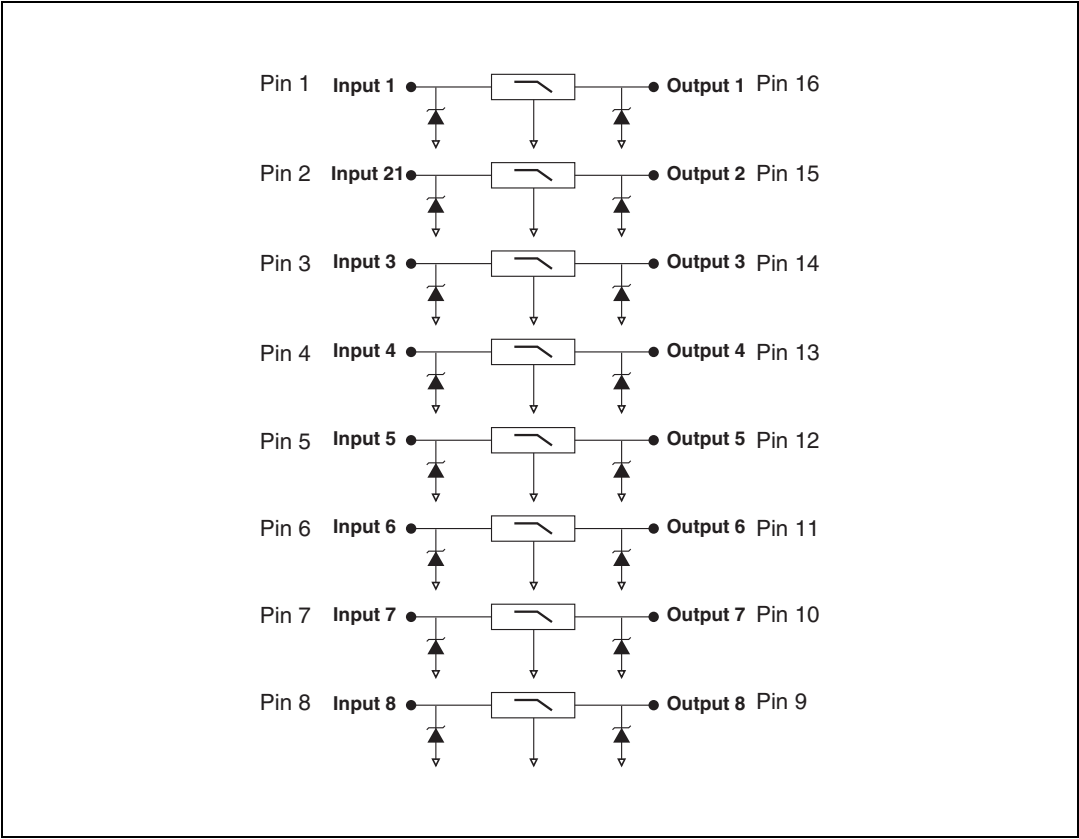
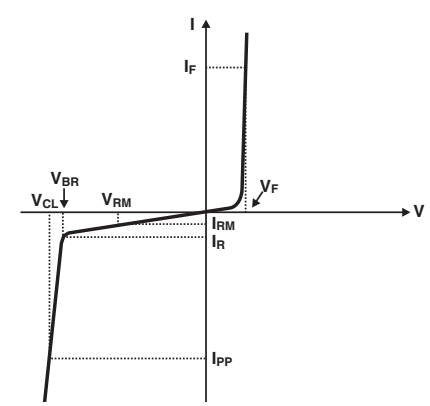


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V_{PP}	ESD IEC 61000-4-2, air discharge	15	kV
	ESD IEC 61000-4-2 contact discharge	15	
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	
V _{BR}	Breakdown voltage	
I _{RM}	Leakage current @ V _{RM}	
V _{RM}	Stand-off voltage	
V _{CL}	Clamping voltage	
R _d	Dynamic resistance	
I _{PP}	Peak pulse current	
R _{I/O}	Series resistance between Input and Output	
C _{line}	Input capacitance per line	

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V _{BR}	I _R = 1 mA	6	8	10	V
V _F	I _F = 10 mA	0.5	1.0	1.5	V
I _{RM}	V _{RM} = 3 V per line			200	nA
R _{I/O}	Tolerance ± 10%	90	100	110	Ω
C _{line}	V _{LINE} = 0 V dc, V _{OSC} = 30 mV, F = 1 MHz	38	45	52	pF

Figure 3. S21 attenuation measurement

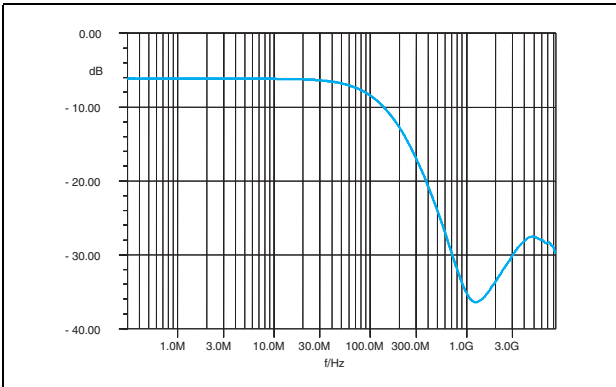


Figure 4. Analog cross talk measurements

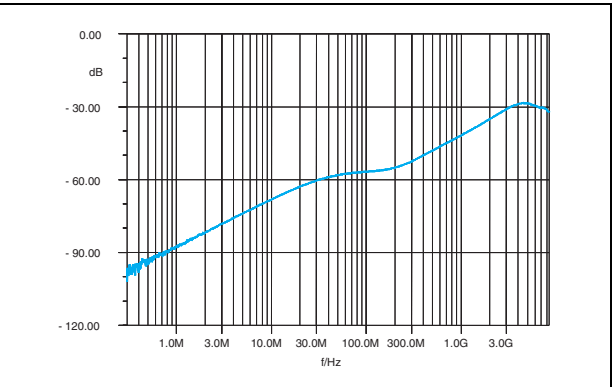


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

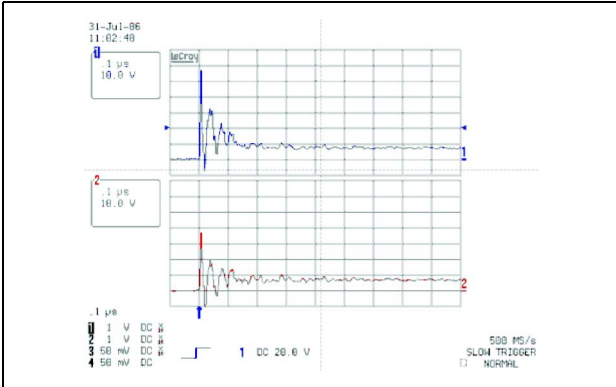


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

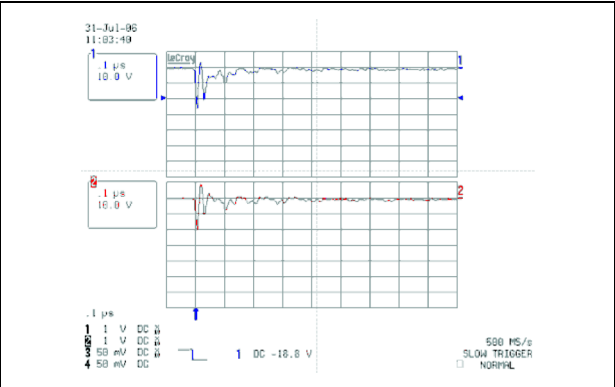
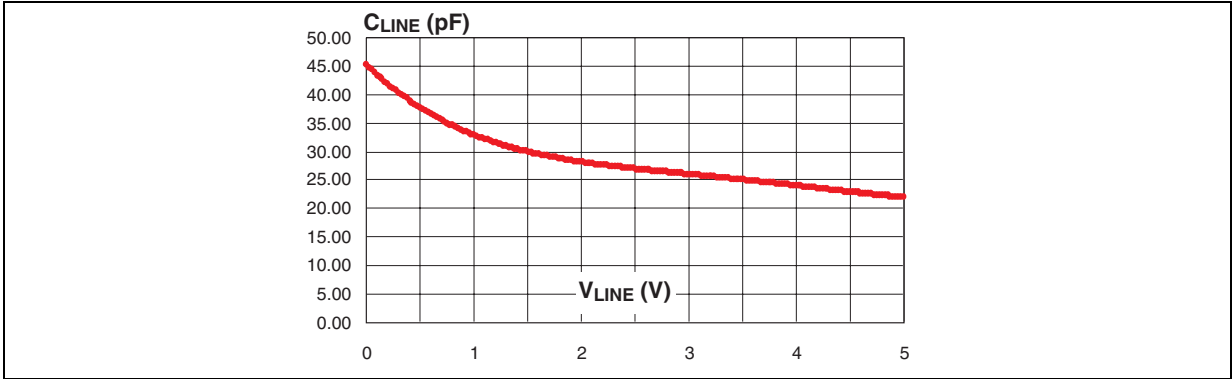
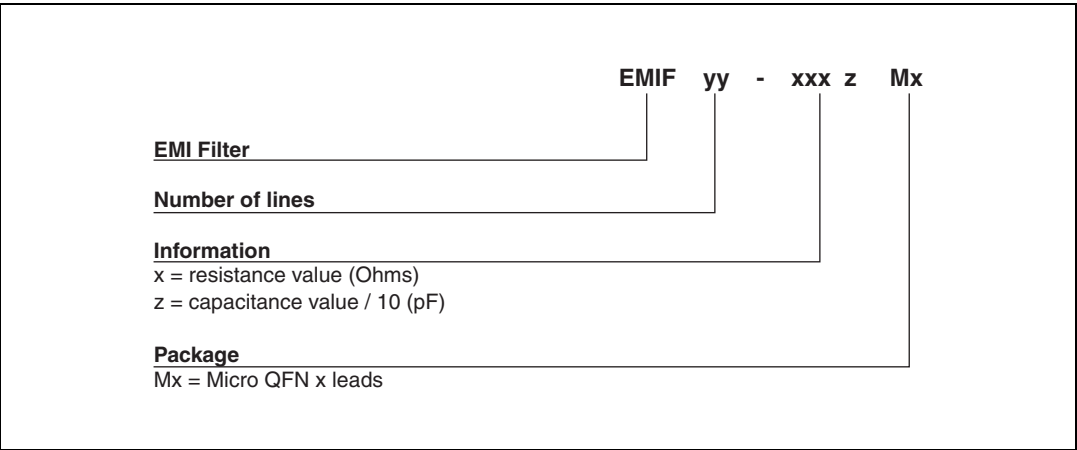


Figure 7. Line capacitance versus reverse voltage applied (typical value)



2 Ordering information scheme

Figure 8. Ordering information scheme



3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Table 3. Micro QFN 3.3x1.5 16L dimensions

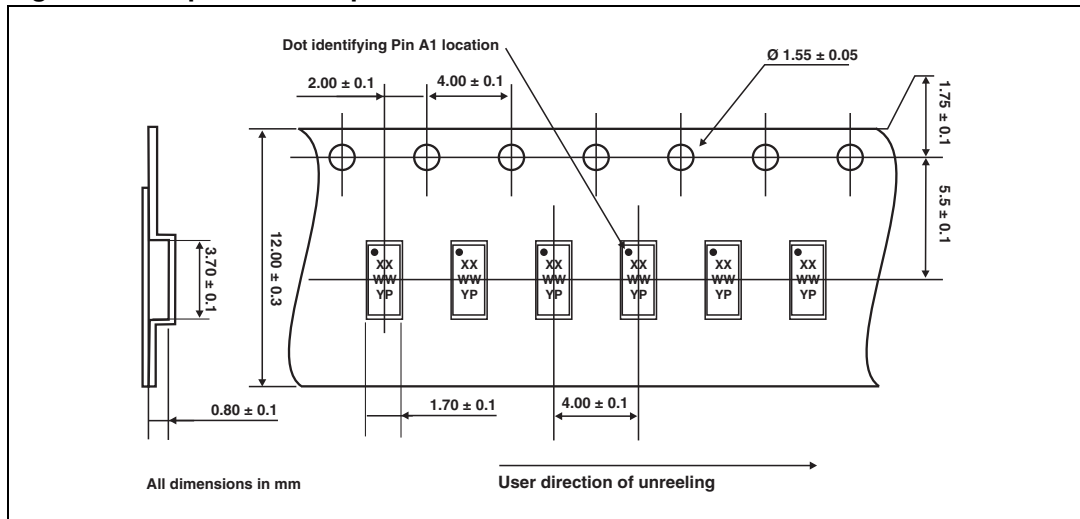
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.20	3.30	3.40	0.126	0.130	0.134
D2	2.45	2.60	2.70	0.096	0.102	0.106
E	1.40	1.50	1.60	0.055	0.059	0.063
E2	0.20	0.35	0.45	0.008	0.014	0.018
e		0.40			0.016	
K	0.20			0.008		
L	0.20	0.30	0.40	0.008	0.012	0.016

Figure 9. Micro QFN 3.3x1.5 16L footprint (dimensions in mm)

Figure 10. Marking

	<p>Dot : Pin 1 Identification X X= Marking WW= DataCode (week) Y=Data code (Year) P=Assembly plant</p>
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Figure 11. Tape and reel specification



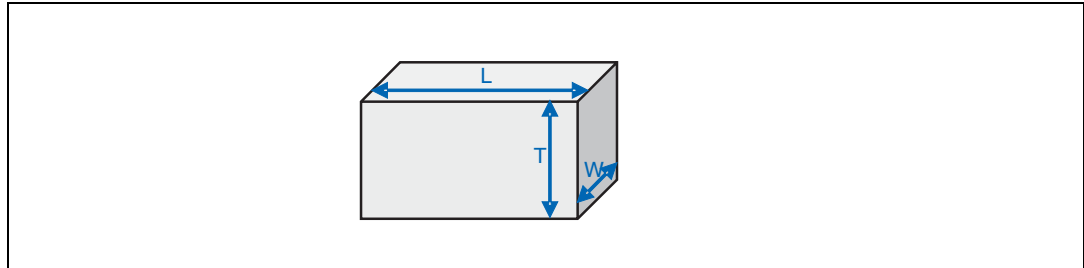
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 12. Stencil opening dimensions



- b) General design rule

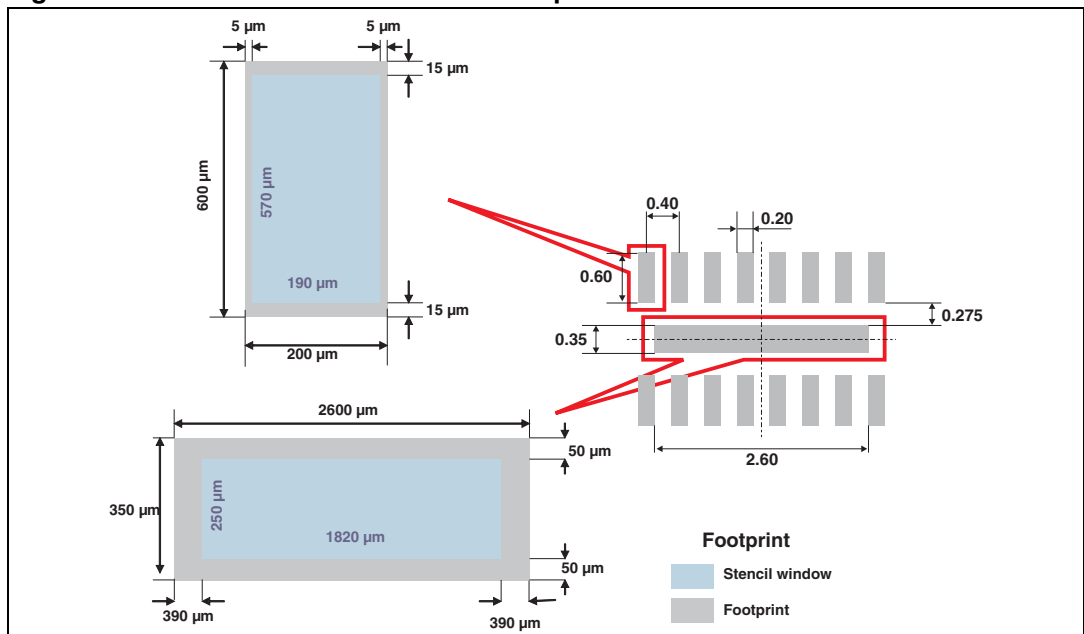
Stencil thickness (T) = 75 ~ 125 μm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
 - a) Stencil opening thickness: 100 μm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 13. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 μm .

4.3 Placement

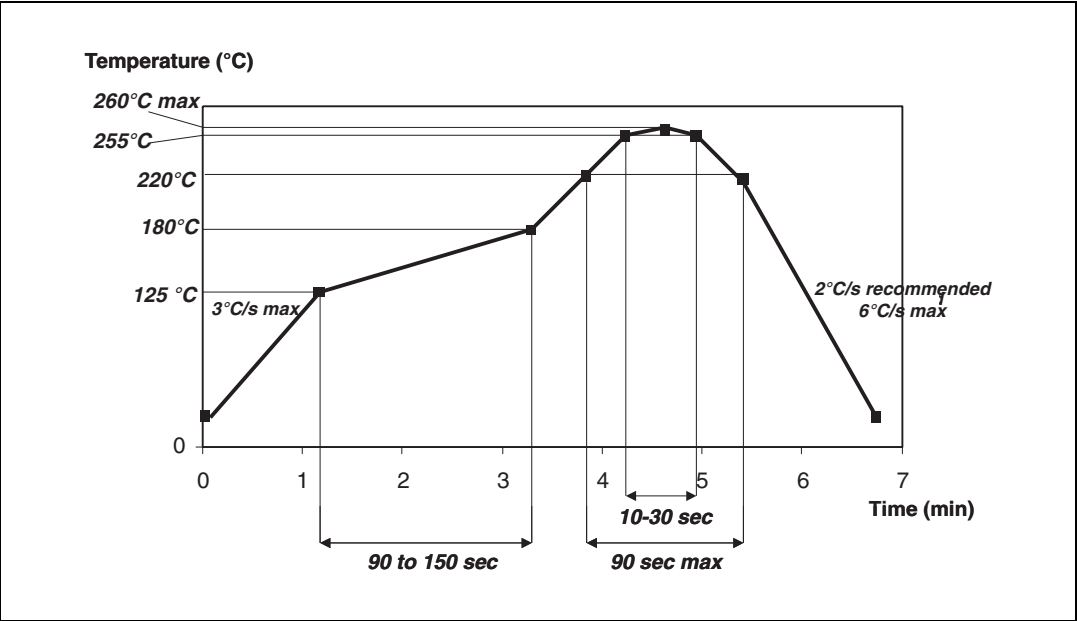
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-1005M16	H8 ⁽¹⁾	Micro QFN	7.2 mg	3000	Tape and reel (7")

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
24-Oct-2006	1	Initial release.
04-Feb-2008	2	Reformatted to current standards. Updated ECOPACK statement. Added Section 4: Recommendation on PCB assembly .

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