## Absolute Maximum Ratings

Voltage Range on $V_{DD}$ Relative to GND.....-0.5V to +6.5V
Voltage Range on $V_{DDA}$ Relative to GND.....-0.5V to +6.5V
Voltage Range on CLKA, RSTA, I/OA.....-0.5V to ($V_{CCA}$ + 0.5V)
Voltage Range on CLKB, RSTB, I/OB.....-0.5V to ($V_{CCB}$ + 0.5V)
Voltage Range on All Other Pins
Relative to GND.....-0.5V to ($V_{DD}$ + 0.5V)
Maximum Junction Temperature.....+125°C
Maximum Power Dissipation Range ($T_A$ = -25°C to +85°C)..700mW
Storage Temperature Range.....-55°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Recommended DC Operating Conditions

($V_{DD}$ = +3.3V, $V_{DDA}$ = +5.0V, $T_A$ = +25°C, unless otherwise noted. All specifications apply to the device, unless otherwise noted in the CONDITIONS column.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Digital Supply Voltage | $V_{DD}$ | | 2.7 | | 6.0 | V |
| Card Voltage-Generator Supply Voltage | $V_{DDA}$ | Must be ≥ $V_{DD}$ | 4.75 | | 6.0 | V |
| Reset Voltage Thresholds | $V_{TH2}$ | Threshold voltage (falling) | 2.20 | 2.45 | 2.65 | V |
| | $V_{HYS2}$ | Hysteresis | 50 | 100 | 200 | mV |
| **CURRENT CONSUMPTION** | | | | | | |
| Active $V_{DD}$ Current 5V Cards (Including 80mA Draw from 5V Card) | $I_{DD\_50V}$ | $I_{CC}$ = 80mA, $f_{XTAL}$ = 20MHz, $f_{CLK}$ = 10MHz, $V_{DDA}$ = 5.0V | | 80.75 | 85 | mA |
| Active $V_{DD}$ Current 5V Cards (Current Consumed by Device Only) | $I_{DD\_IC}$ | $I_{CC}$ = 80mA, $f_{XTAL}$ = 20MHz, $f_{CLK}$ = 10MHz, $V_{DDA}$ = 5.0V (Note 2) | | 0.75 | 5 | mA |
| Active $V_{DD}$ Current 3V Cards (Including 65mA Draw from 3V Card) | $I_{DD\_30V}$ | $I_{CC}$ = 65mA, $f_{XTAL}$ = 20MHz, $f_{CLK}$ = 10MHz, $V_{DDA}$ = 5.0V | | 65.75 | 70 | mA |
| Active $V_{DD}$ Current 3V Cards (Current Consumed by Device Only) | $I_{DD\_IC}$ | $I_{CC}$ = 65mA, $f_{XTAL}$ = 20MHz, $f_{CLK}$ = 10MHz, $V_{DDA}$ = 5.0V (Note 2) | | 0.75 | 5 | mA |
| Active $V_{DD}$ Current 1.8V Cards (Including 30mA Draw from 1.8V Card) | $I_{DD\_18V}$ | $I_{CC}$ = 30mA, $f_{XTAL}$ = 20MHz, $f_{CLK}$ = 10MHz, $V_{DDA}$ = 5.0V | | 30.75 | 40 | mA |
| Active $V_{DD}$ Current 1.8V Cards (Current Consumed by Device Only) | $I_{DD\_IC}$ | $I_{CC}$ = 30mA, $f_{XTAL}$ = 20MHz, $f_{CLK}$ = 10MHz, $V_{DDA}$ = 5.0V (Note 2) | | 0.75 | 5 | mA |
| Inactive-Mode Current | $I_{DD}$ | Card inactive, active-high PRES_, device not in stop mode | | 50 | 400 | µA |
| Stop-Mode Current | $I_{DD\_STOP}$ | Device in ultra-low-power stop mode ($\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V set to logic 1) (Note 3) | | 0.01 | 2 | µA |

## Recommended DC Operating Conditions (continued)

($V_{DD}$ = +3.3V, $V_{DDA}$ = +5.0V, $T_A$ = +25°C, unless otherwise noted. All specifications apply to the device, unless otherwise noted in the CONDITIONS column.) (Note 1)

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **CLOCK SOURCE** | | | | | | | |
| Crystal Frequency | | $f_{XTAL}$ | External crystal (Note 1) | 0 | | 20 | MHz |
| XTAL1 Operating Conditions | | $f_{XTAL1}$ | (Note 1) | 0 | | 20 | MHz |
| | | $V_{IL\_XTAL1}$ | Low-level input on XTAL1 | -0.3 | | 0.3 x $V_{DD}$ | V |
| | | $V_{IH\_XTAL1}$ | High-level input on XTAL1 | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 | |
| External Capacitance for Crystal | | $C_{XTAL1}$, $C_{XTAL2}$ | | | | 15 | pF |
| Internal Oscillator | | $f_{INT}$ | | 2.2 | 2.7 | 3.4 | MHz |
| **SHUTDOWN TEMPERATURE** | | | | | | | |
| Shutdown Temperature | | $T_{SD}$ | | | +150 | | °C |
| **RSTA AND RSTB PINS** | | | | | | | |
| Card-Inactive Mode | Output Low Voltage | $V_{OL\_RST1}$ | $I_{OL\_RST}$ = 1mA | | | 0.3 | V |
| | Output Current | $I_{OL\_RST1}$ | $V_{OL\_RST}$ = 0V | | | -1 | mA |
| Card-Active Mode | Output Low Voltage | $V_{OL\_RST2}$ | $I_{OL\_RST}$ = 200µA | | | 0.3 | V |
| | Output High Voltage | $V_{OH\_RST2}$ | $I_{OH\_RST}$ = -200µA | $V_{CC}$ - 0.5 | | | V |
| | Rise Time | $t_{R\_RST}$ | $C_L$ = 30pF (Note 1) | | | 0.1 | µs |
| | Fall Time | $t_{F\_RST}$ | $C_L$ = 30pF (Note 1) | | | 0.1 | µs |
| | Current Limitation | $I_{RST(LIMIT)}$ | | -20 | | +20 | mA |
| | RSTIN to RST Delay | $t_{D(RSTIN-RST)}$ | | | | 2 | µs |
| **CLKA AND CLKB PINS** | | | | | | | |
| Card-Inactive Mode | Output Low Voltage | $V_{OL\_CLK1}$ | $I_{OLCLK}$ = 1mA | | | 0.3 | V |
| | Output Current | $I_{OL\_CLK1}$ | $V_{OLCLK}$ = 0V | | | -1 | mA |
| Card-Active Mode | Output Low Voltage | $V_{OL\_CLK2}$ | $I_{OLCLK}$ = 200µA | | | 0.3 | V |
| | Output High Voltage | $V_{OH\_CLK2}$ | $I_{OHCLK}$ = -200µA | $V_{CC}$ - 0.5 | | | V |
| | Rise Time | $t_{R\_CLK}$ | $C_L$ = 30pF (Notes 1, 4) | | | 8 | ns |
| | Fall Time | $t_{F\_CLK}$ | $C_L$ = 30pF (Notes 1, 4) | | | 8 | ns |
| | Current Limitation | $I_{CLK(LIMIT)}$ | | -75 | | +75 | mA |
| | Clock Frequency | $f_{CLK}$ | Operational | 0 | | 10 | MHz |
| | Duty Factor | δ | $C_L$ = 30pF | 45 | | 55 | % |
| | Slew Rate | SR | $C_L$ = 30pF (Note 1) | 0.2 | | | V/ns |
| **$V_{CCA}$ AND $V_{CCB}$ PINS** | | | | | | | |
| Card-Inactive Mode | Output Low Voltage | $V_{CC1}$ | $I_{CC}$ = 1mA | | | 0.3 | V |
| | Output Current | $I_{CC1}$ | $V_{CC}$ = 0V | 0 | | -1 | mA |

## Recommended DC Operating Conditions (continued)

($V_{DD}$ = +3.3V, $V_{DDA}$ = +5.0V, $T_A$ = +25°C, unless otherwise noted. All specifications apply to the device, unless otherwise noted in the CONDITIONS column.) (Note 1)

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Card-Active Mode | Output Low Voltage | $V_{CC2}$ | Device: $I_{CC(5V)}$ < 30mA, $V_{DDA}$ = 4.75V (Note 1) | 4.65 | 5 | 5.25 | V |
| | | | Device: $I_{CC(5V)}$ < 80mA | 4.75 | 5 | 5.25 | |
| | | | Device: $I_{CC(3V)}$ < 65mA | 2.78 | 3 | 3.24 | |
| | | | Device: $I_{CC(1.8V)}$ < 30mA | 1.64 | 1.8 | 1.98 | |
| | | | 5V card; current pulses of 40nC with I < 200mA, t < 400ns, f < 20MHz | 4.6 | | 5.4 | |
| | | | 3V card; current pulses of 24nC with I < 200mA, t < 400ns, f < 20MHz | 2.75 | | 3.25 | |
| | | | 1.8V card; current pulses of 12nC with I < 200mA, t < 400ns, f < 20MHz | 1.62 | | 1.98 | |
| | Output Current | $I_{CC2}$ | $V_{CC(5V)}$ = 0 to 5V | | | -80 | mA |
| | | | $V_{CC(3V)}$ = 0 to 3V | | | -65 | |
| | | | $V_{CC(1.8V)}$ = 0 to 1.8V | | | -30 | |
| | Shutdown Current Threshold | $I_{CC(SD)}$ | (Note 1) | | 120 | | mA |
| | Slew Rate | $V_{CCSR}$ | Up/down; C < 300nF (Note 5) | 0.05 | 0.16 | 0.22 | V/µs |
| **DATA LINES (I/O_ AND I/OIN)** | | | | | | | |
| I/O_ □ I/OIN Falling Edge Delay | | $t_{D(IO-IOIN)}$ | (Note 1) | | | 200 | ns |
| Pullup Pulse Active Time | | $t_{PU}$ | (Note 1) | | | 100 | ns |
| Maximum Frequency | | $f_{IOMAX}$ | | | | 1 | MHz |
| Input Capacitance | | $C_I$ | | | | 10 | pF |
| **I/OA AND I/OB PINS** | | | | | | | |
| Card-Inactive Mode | Output Low Voltage | $V_{OL\_IO1}$ | $I_{OL\_IO}$ = 1mA | | | 0.3 | V |
| | Output Current | $I_{OL\_IO1}$ | $V_{OL\_IO}$ = 0V | 0 | | -1 | mA |
| | Internal Pullup Resistor | $R_{PU\_IO}$ | To $V_{CC}$ | 6 | 11 | 19 | kΩ |
| Card-Active Mode | Output Low Voltage | $V_{OL\_IO2}$ | $I_{OL\_IO}$ = 1mA | | | 0.3 | V |
| | Output High Voltage | $V_{OH\_IO2}$ | $I_{OH\_IO}$ = < -20µA | 0.8 x $V_{CC}$ | | | V |
| | | | $I_{OH\_IO}$ = < -40µA (3V/5V) | 0.75 x $V_{CC}$ | | | |
| | Output Rise/Fall Time | $t_{OT}$ | $C_L$ = 30pF (Note 1) | | | 0.1 | µs |
| | Input Low Voltage | $V_{IL\_IO}$ | | -0.3 | | +0.8 | V |
| | Input High Voltage | $V_{IH\_IO}$ | | 1.5 | | $V_{CC}$ | |

## Recommended DC Operating Conditions (continued)

($V_{DD}$ = +3.3V, $V_{DDA}$ = +5.0V, $T_A$ = +25°C, unless otherwise noted. All specifications apply to the device, unless otherwise noted in the CONDITIONS column.) (Note 1)

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Card-Active Mode | Input Low Current | $I_{IL\_IO}$ | $V_{IL\_IO}$ = 0V | | | 700 | µA |
| | Input High Current | $I_{IH\_IO}$ | $V_{IH\_IO}$ = $V_{CC}$ | -20 | | +20 | µA |
| | Input Rise/Fall Time | $t_{IT}$ | | | | 1.2 | µs |
| | Current Limitation | $I_{IO(LIMIT)}$ | $C_L$ = 30pF | -15 | | +15 | mA |
| **I/OIN PIN** | | | | | | | |
| Output Low Voltage | | $V_{OL}$ | $I_{OL}$ = 1mA | | | 0.3 | V |
| Output High Voltage | | $V_{OH}$ | $I_{OH}$ < -40µA | 0.75 x $V_{DD}$ | | $V_{DD}$ + 0.1 | V |
| Output Rise/Fall Time | | $t_{OT}$ | $C_L$ = 30pF, 10% to 90% | | | 0.1 | µs |
| Input Low Voltage | | $V_{IL}$ | | -0.3 | | +0.3 x $V_{DD}$ | V |
| Input High Voltage | | $V_{IH}$ | | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input Low Current | | $I_{IL\_IO}$ | $V_{IL}$ = 0V | | | 700 | µA |
| Input High Current | | $I_{IH\_IO}$ | $V_{IH}$ = $V_{DD}$ | -10 | | +10 | µA |
| Input Rise/Fall Time | | $t_{IT}$ | $V_{IL}$ to $V_{IH}$ | | | 1.2 | µs |
| Integrated Pullup Resistor | | $R_{PU}$ | Pullup to $V_{DD}$ | 6 | 11 | 19 | kΩ |
| **CONTROL PINS (CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, 5V/$\overline{\text{3V}}$, 1_8V)** | | | | | | | |
| Input Low Voltage | | $V_{IL}$ | | -0.3 | | +0.3 x $V_{DD}$ | V |
| Input High Voltage | | $V_{IH}$ | | 0.7 x $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Input Low Current | | $I_{IL\_IO}$ | 0 < $V_{IL}$ < $V_{DD}$ | -5 | | +5 | µA |
| Input High Current | | $I_{IH\_IO}$ | 0 < $V_{IH}$ < $V_{DD}$ | -5 | | +5 | µA |
| **INTERRUPT OUTPUT PINS ($\overline{\text{OFF}}$ AND $\overline{\text{OFF2}}$)** | | | | | | | |
| Output Low Voltage | | $V_{OL}$ | $I_{OL}$ = 2mA | | | 0.3 | V |
| Output High Voltage | | $V_{OH}$ | $I_{OH}$ = -15µA | 0.75 x $V_{DD}$ | | | V |
| Integrated Pullup Resistor | | $R_{PU}$ | Pullup to $V_{DD}$ | 12 | 24 | 38 | kΩ |
| **PRESA AND PRESB PINS** | | | | | | | |
| Input Low Voltage | | $V_{IL\_PRES}$ | | | | 0.3 x $V_{DD}$ | V |
| Input High Voltage | | $V_{IH\_PRES}$ | | 0.7 x $V_{DD}$ | | | V |
| Input Low Current | | $I_{IL\_PRES}$ | $V_{IL\_PRES}$ = 0V | -5 | | +5 | µA |
| Input High Current | | $I_{IH\_PRES}$ | $V_{IH\_PRES}$ = $V_{DD}$ | | | 10 | µA |

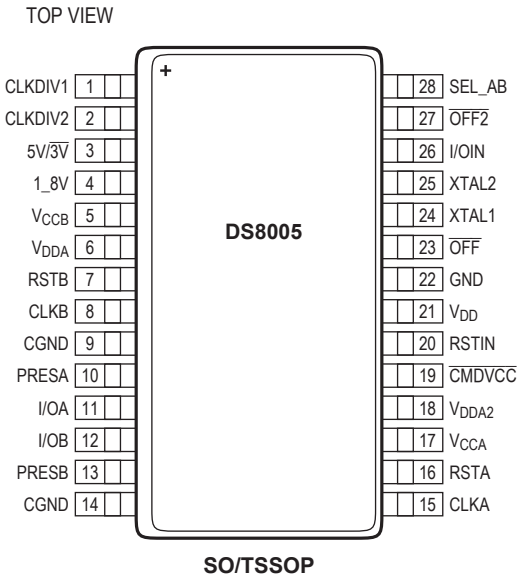
## Recommended DC Operating Conditions (continued)

($V_{DD}$ = +3.3V, $V_{DDA}$ = +5.0V, $T_A$ = +25°C, unless otherwise noted. All specifications apply to the device, unless otherwise noted in the CONDITIONS column.) (Note 1)

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **TIMING** | | | | | | | |
| Activation Time | | $t_{ACT}$ | | 50 | 160 | 220 | µs |
| Deactivation Time | | $t_{DEACT}$ | | 50 | 80 | 100 | µs |
| CLK_ to Card Start Time | Window Start | $t_3$ | | 50 | 95 | 130 | µs |
| | Window End | $t_5$ | | 140 | 160 | 220 | |
| PRES Debounce Time | | $t_{DEBOUNCE}$ | | 5 | 8 | 11 | ms |

**Note 1:** Operation guaranteed at -40°C and +85°C but not tested.
**Note 2:** $I_{DD\_IC}$ measures the amount of current used by the device to provide the smart card current minus the load.
**Note 3:** Stop mode is enabled by setting $\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V to a logic-high.
**Note 4:** Parameters are guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the maximum rise and fall time is 10ns.
**Note 5:** Parameter is guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the minimum slew rate is 0.05V/µs and the maximum slew rate is 0.5V/µs.

## Pin Configuration




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 2 | CLKDIV1, CLKDIV2 | Clock Divider. Determines the divided-down input clock frequency (presented at XTAL1 or from a crystal at XTAL1 and XTAL2) on the CLK_ output pin. Dividers of 1, 2, 4, and 8 are available. |
| 3 | 5V/$\overline{3V}$ | 5V/3V Selection Pin. Allows selection of 5V or 3V for communication with an IC card. Logic-high selects 5V operation; logic-low selects 3V operation. The 1_8V pin overrides the setting on this pin if active. See Table 3 for a complete description of choosing card voltages. |
| 4 | 1_8V | 1.8V Operation Selection. This active-high input puts the device into 1.8V smart card communication mode. The selected interface (when activated) powers a card with a 1.8V supply and all I/O lines operate at 1.8V. |
| 5 | $V_{CCB}$ | Smart Card Supply Voltage, Interface B. Decouple to CGND (card ground) with 2 x 100nF or 100 + 200nF capacitors (ESR < 100mΩ). |
| 6 | $V_{DDA}$ | Smart Card Interface Supply. Connect to a 5V power supply to support 1.8V, 3.0V, and 5.0V cards. If $V_{DD} \geq 4.9V$, this pin can be connected directly to $V_{DD}$. Decouple this pin to GND using 100nF and 10µF capacitors. |
| 7 | RSTB | Smart Card Reset, Interface B. Card reset output from contact C2. |
| 8 | CLKB | Smart Card Clock, Interface B. Card clock, contact C3. |
| 9, 14 | CGND | Smart Card Ground |
| 10 | PRESA | Interface A Card Presence Indicator. Active-high card presence input for the first card interface. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ), the $\overline{OFF}$ signal becomes active if the first card interface is selected (SEL_AB low), else the $\overline{OFF2}$ signal becomes active. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 11 | I/OA | Smart Card Data-Line Output, Interface A. Card data communication line, contact C7. This pin is only active if the first card interface is selected (SEL_AB low) and the interface has gone through an activation sequence. |
| 12 | I/OB | Smart Card Data-Line Output, Interface B. Card data communication line, contact C7. This pin is only active if the second card interface is selected (SEL_AB high) and the interface has gone through an activation sequence. |
| 13 | PRESB | Interface B Card Presence Indicator. Active-high card presence input for the second card interface. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ), the $\overline{OFF}$ signal becomes active if the second card interface is selected (SEL_AB high), else the $\overline{OFF2}$ signal becomes active. |
| 15 | CLKA | Smart Card Clock, Interface A. Card clock, contact C3. |
| 16 | RSTA | Smart Card Reset, Interface A. Card reset output from contact C2. |
| 17 | $V_{CCA}$ | Smart Card Supply Voltage, Interface A. Decouple to CGND (card ground) with 2 x 100nF or 100 + 220nF capacitors (ESR < 100mΩ). |
| 18 | $V_{DDA2}$ | Smart Card Interface Supply. Connect to a 5V power supply to support 1.8V, 3.0V, and 5.0V cards. If $V_{DD} \geq 4.9V$, this pin can be connected directly to $V_{DD}$. Decouple this pin to GND using 100nF and 10µF capacitors. |
| 19 | $\overline{CMDVCC}$ | Activation Sequence Initiate. Active-low input from host. |
| 20 | RSTIN | Card Reset Input. Reset input from the host. |
| 21 | $V_{DD}$ | Supply Voltage |
| 22 | GND | Digital Ground |
| 23 | $\overline{OFF}$ | Status Output for Selected Interface. Active-low interrupt output to the host. Includes a 20kΩ integrated pullup resistor to $V_{DD}$. This pin reflects fault events and PRES_ events on the currently selected interface only (behaving as if it were a DS8024 with only one interface). The $\overline{OFF2}$ pin should be used to monitor presence events on the nonselected interface. |
| 24, 25 | XTAL1, XTAL2 | Crystal/Clock Input. Connect an input from an external clock to XTAL1 or connect a crystal across XTAL1 and XTAL2. Leave XTAL2 disconnected if driving XTAL1 from an external clock source. |
| 26 | I/OIN | I/O Input. Host-to-interface chip data I/O line. |
| 27 | $\overline{OFF2}$ | Status Output for Nonselected Interface. This pin passes through the presence signal for the nonselected interface. If SEL_AB is low (the A interface is selected), this pin reflects the state of the PRESB input. If SEL_AB is high (the B interface is selected), this pin reflects the state of the PRESA input. |
| 28 | SEL_AB | Interface Selection. This pin selects the interface the input pins (I/OIN, RSTIN, etc.) communicate with and control. If SEL_AB is low, the A interface is selected. Activation sequences power up $V_{CCA}$ and communication occurs with CLKA, I/OA, and RSTA. If SEL_AB is high, the B interface is selected. Both interfaces can be powered and clocking at the same time. See the *Switching A/B Interfaces* section for more information. |

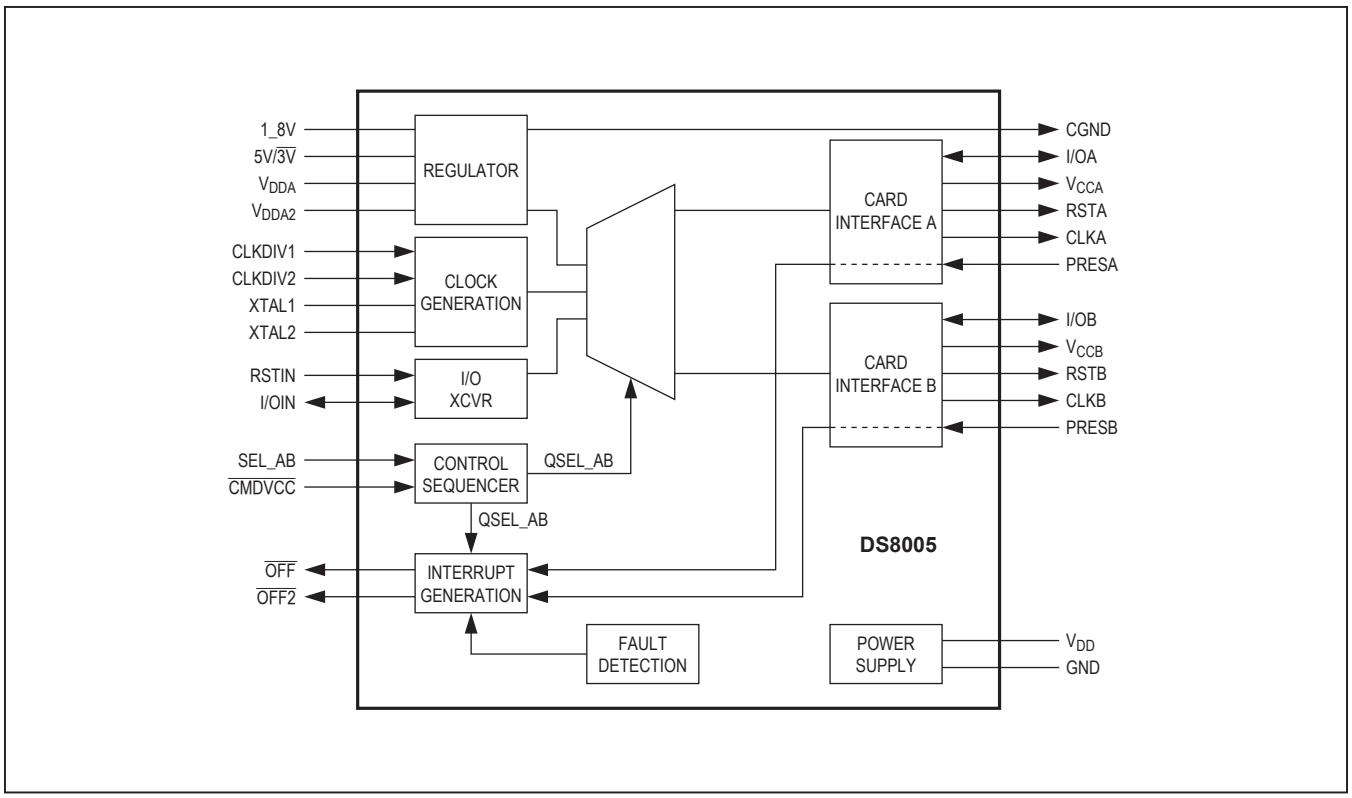



*Figure 1. Functional Diagram*

## Detailed Description

The DS8005 is an analog front-end for communicating with 1.8V, 3V, and 5V dual smart cards. It is a dual input-voltage device, requiring one supply to match that of a host microcontroller and a separate +5V supply for generating correct smart card supply voltages. The device translates all communication lines to the correct voltage level and provides power for smart card operation. It is a low-power device, consuming very little current in active-mode operation (during a smart card communication session), and is suitable for use in battery-powered devices such as laptops and PDAs, consuming only 10nA in stop mode. The device is designed for applications that do not require communication using the C4 and C8 card contacts (AUX1 and AUX2). It is suitable for SIM/SAM interfacing, as well as for applications where only the I/O line is used to communicate with a smart card.

## Power Supply

The device has dual supplies. The supply pins for the device are $V_{DD}$, GND, and $V_{DDA}$. $V_{DD}$ should be in the 2.7V to 6.0V range, and is the supply for signals that interface with the host controller. It should, therefore, be the same supply as used by the host controller. All smart card contacts remain inactive during power-on or power-off. The internal circuits are kept in the reset state until $V_{DD}$ reaches $V_{TH2}$ + $V_{HYS2}$ and for the duration of the internal power-on reset pulse, $t_W$. A deactivation sequence is executed when $V_{DD}$ falls below $V_{TH2}$.

An internal regulator generates the 1.8V, 3V, or 5V card supply voltage ($V_{CC\_}$). The regulator should be supplied separately by $V_{DDA}$. $V_{DDA}$ should be connected to a minimum 4.75V supply to provide the correct supply voltage for 5V smart cards.

## Voltage Supervisor

The voltage supervisor monitors the $V_{DD}$ supply. A 220µs reset pulse ($t_W$) is used internally to keep the device inactive during power-on or power-off of the $V_{DD}$ supply. See Figure 2.

The IC card interface remains inactive regardless of the levels on the command lines until duration $t_W$ after $V_{DD}$ has reached a level higher than $V_{TH2}$ + $V_{HYS2}$. When $V_{DD}$ falls below $V_{TH2}$, the device executes a card deactivation sequence if the card interface is active.

## Clock Circuitry

The card clock signal (CLKA/CLKB) is derived from a clock signal input to XTAL1 or from a crystal operating at up to 20MHz connected between XTAL1 and XTAL2. The output clock frequency of CLK_ is selectable through inputs CLKDIV1 and CLKDIV2. The CLK signal frequency can be $f_{XTAL}$, $f_{XTAL}/2$, $f_{XTAL}/4$, or $f_{XTAL}/8$. See Table 1 for the frequency generated on the CLK_ signal given the inputs to CLKDIV1 and CLKDIV2.

Note that CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10ns minimum between changes is needed. The minimum duration of any state of CLK_ is eight periods of XTAL1.

## Table 1. Clock Frequency Selection

| CLKDIV1 | CLKDIV2 | $f_{CLK}$ |
|---|---|---|
| 0 | 0 | $f_{XTAL}/8$ |
| 0 | 1 | $f_{XTAL}/4$ |
| 1 | 1 | $f_{XTAL}/2$ |
| 1 | 0 | $f_{XTAL}$ |

The frequency change is synchronous: during a transition of the clock divider, no pulse is shorter than 45% of the smallest period, and the first and last clock pulses about the instant of change have the correct width. When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command.

The $f_{XTAL}$ duty factor depends on the input signal on XTAL1. To reach a 45% to 55% duty factor on CLK_, XTAL1 should have a 48% to 52% duty factor with transition times less than 5% of the period.

With a crystal, the duty factor on CLK_ can be 45% to 55% depending on the circuit layout and on the crystal characteristics and frequency. In other cases, the duty factor on CLK_ is guaranteed between 45% and 55% of the clock period.

## I/O Transceivers

I/O_ and I/OIN are pulled high with an 11kΩ resistor (I/O_ to $V_{CC}$_ and I/OIN to $V_{DD}$) in the inactive state. The first side of the transceiver to receive a falling edge becomes the master. When a falling edge is detected (and the master is decided), the detection of falling edges on the line of the other side is disabled; that side then becomes a slave. After a time delay $t_{D(EDGE)}$, an n transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side asserts a logic 1, a p transistor on the slave side is activated during the time delay $t_{PU}$ and then both sides return to their inactive (pulled up) states. This active pullup provides fast low-to-high transitions. After the duration of $t_{PU}$, the output voltage depends only on the internal pullup resistor and the load current. Current to and from the card I/O lines is limited internally to 15mA. The maximum frequency on these lines is 1MHz.

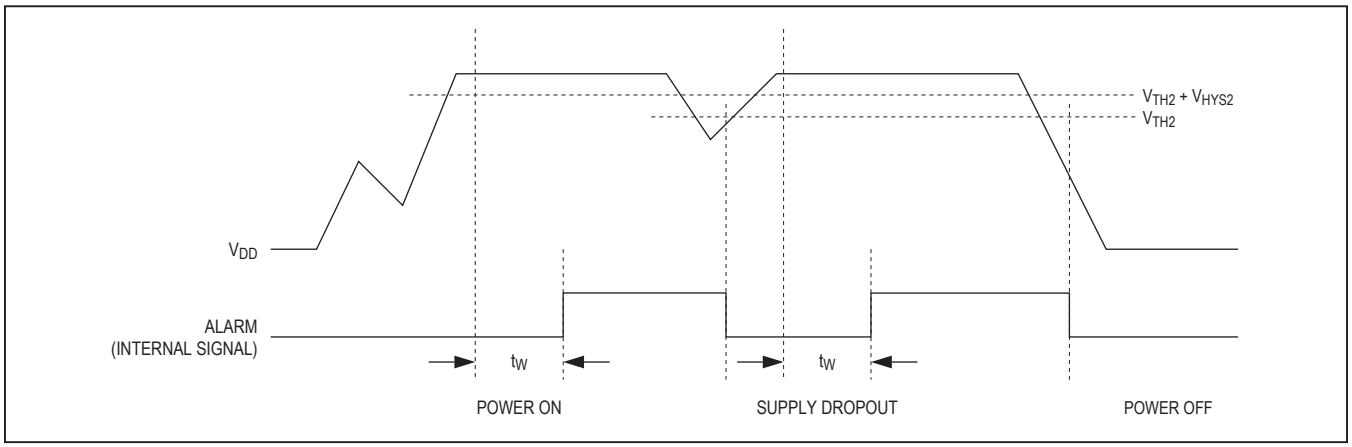



*Figure 2. Voltage Supervisor Behavior*

## Inactive Mode

The device powers up with the card interface in the inactive mode. Minimal circuitry is active while waiting for the host to initiate a smart card session.

- All card contacts are inactive (approximately 200Ω to GND).
- The I/OIN pin in the high-impedance state (11kΩ pullup resistor to $V_{DD}$).
- Voltage generators are stopped.
- XTAL oscillator is running (if included in the device).
- Voltage supervisor is active.
- The internal oscillator is running at its low frequency.

## Activation Sequence

After power-on and the reset delay, the host microcontroller can monitor card presence with signals $\overline{OFF}$ and $\overline{CMDVCC}$, as shown in Table 2.

If the card is in the reader (if PRES_ is active), the host microcontroller can begin an activation sequence (start a card session) by pulling $\overline{CMDVCC}$ low. The following events form an activation sequence (Figure 3):

1) $\overline{CMDVCC}$ is pulled low.
2) The internal oscillator changes to high frequency ($t_0$).
3) The voltage generator is started (between $t_0$ and $t_1$).

## Table 2. Card Presence Indication

| SEL_AB | $\overline{OFF}$ | $\overline{CMDVCC}$ | STATUS |
|---|---|---|---|
| Low | High | High | Card A present. |
| Low | Low | High | Card A **not** present. |
| High | High | High | Card B present. |
| High | Low | High | Card B **not** present. |
| **SEL_AB** | **$\overline{OFF2}$** | **$\overline{CMDVCC}$** | **STATUS** |
| Low | High | High | Card B present. |
| Low | Low | High | Card B **not** present. |
| High | High | High | Card A present. |
| High | Low | High | Card A **not** present. |

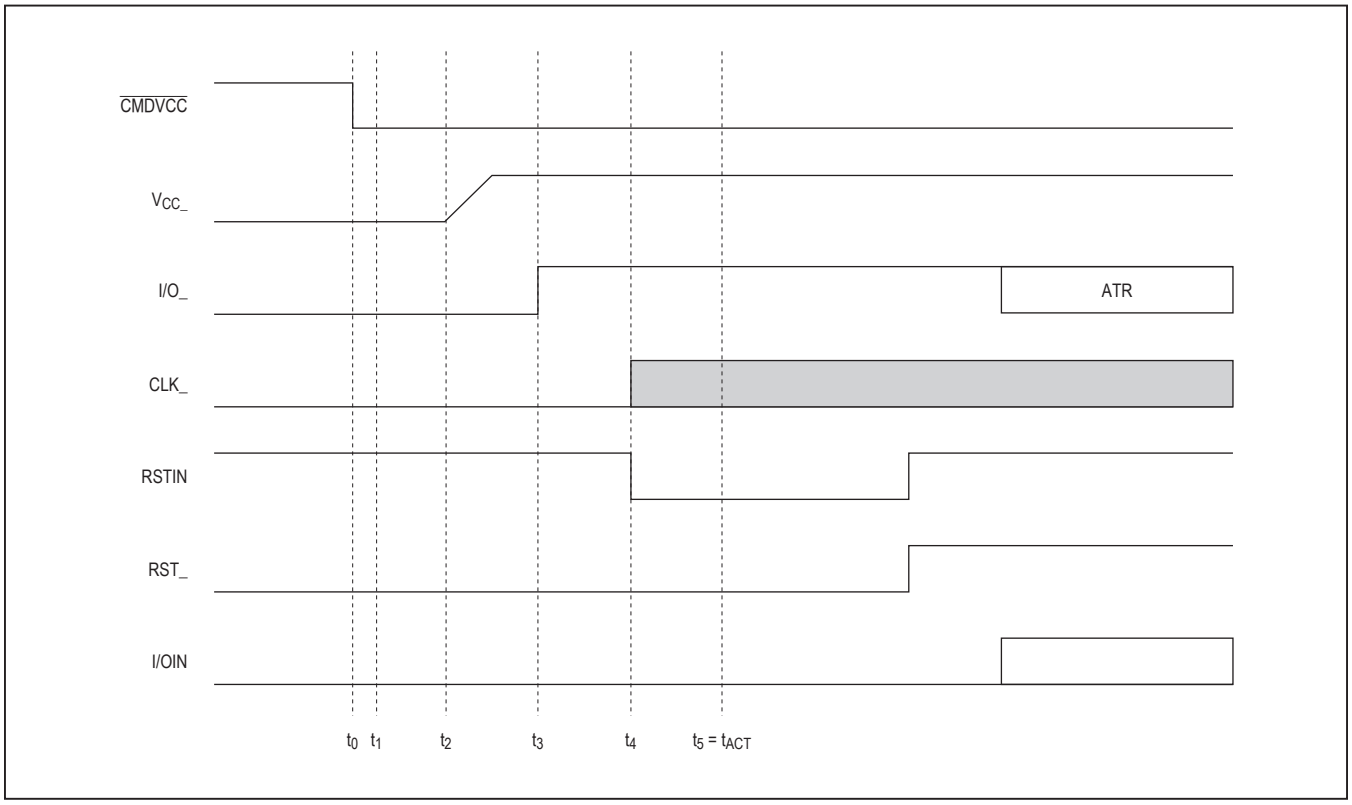



*Figure 3. Activation Sequence Using RSTIN and $\overline{CMDVCC}$*

4) $V_{CC\_}$ rises from 0 to 5V, 3V, or 1.8V with a controlled slope ($t_2 = t_1 + 1.5 \times T$). T is 64 times the internal oscillator period (approximately 25µs).
5) I/O_ pin is enabled ($t_3 = t_1 + 4T$) (they were previously pulled low).
6) The CLK_ signal is applied to the C3 contact ($t_4$).
7) RST_ is enabled ($t_5 = t_1 + 7T$).

To apply the clock to the card interface:

1) Set RSTIN high.
2) Set $\overline{CMDVCC}$ low.
3) Set RSTIN low between $t_3$ and $t_5$; CLK_ now starts.
4) RST_ stays low until $t_5$, then RST becomes the copy of RSTIN.
5) RSTIN has no further effect on CLK_ after $t_5$.

If the applied clock is not needed, set $\overline{CMDVCC}$ low with RSTIN low. In this case, CLK_ starts at $t_3$ (minimum 200ns after the transition on I/O; see Figure 4); after $t_5$, RSTIN can be set high to obtain an answer to request (ATR) from an inserted smart card. Do not perform activation with RSTIN held permanently high.

## Active Mode

When the activation sequence is completed, the card interface is in active mode. The host microcontroller and the smart card exchange data on the I/O lines.

## Deactivation Sequence

When a session is completed, the host microcontroller sets the $\overline{CMDVCC}$ line high to execute an automatic deactivation sequence and returns the card interface to the inactive mode (Figure 5).

1) RST_ goes low ($t_{10}$).
2) CLK_ is held low ($t_{12} = t_{10} + 0.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25µs).
3) I/O_ pin is pulled low ($t_{13} = t_{10} + T$).
4) $V_{CC}$ starts to fall ($t_{14} = t_{10} + 1.5 \times T$).
5) When $V_{CC\_}$ reaches its inactive state, the deactivation sequence is complete (at $t_{DE}$).
6) All card contacts become low impedance to GND; I/OIN remains at $V_{DD}$ (pulled up through an 11kΩ resistor).
7) The internal oscillator returns to its lower frequency.

## $V_{CC}$ Generator

Each $V_{CC\_}$ generator has a capacity to supply up to 80mA continuously at 5V, 65mA at 3V, and 30mA at 1.8V.

An internal overload detector triggers at approximately 120mA. Current samples to the detector are filtered. This allows spurious current pulses (with a duration of a few µs) up to 200mA to be drawn without causing deactivation. The average current must stay below the specified maximum current value. To maintain $V_{CC}$ voltage accuracy, a 100nF capacitor (with an ESR < 100mΩ) should be connected to CGND and placed near the $V_{CC\_}$ pin, and a 100nF or 220nF capacitor (220nF is the best choice) with the same ESR should be connected to CGND and placed near the smart card reader's C1 contact.

## Fault Detection

The following fault conditions are monitored:

- Short-circuit or high current on $V_{CC\_}$
- Removal of a card during a transaction
- $V_{DD}$ dropping
- Card voltage generator operating out of the specified values ($V_{DDA}$ too low or current consumption too high)
- Overheating

There are two different cases (Figure 6):

- **$\overline{CMDVCC}$ High Outside a Card Session.** Output $\overline{OFF\_}$ is low if a card is not in the card reader and high if a card is in the reader. The $V_{DD}$ supply is monitored—a decrease in input voltage generates an internal power-on reset pulse but does not affect the $\overline{OFF\_}$ signal. Short-circuit and temperature detection is disabled because the card is not powered up.
- **$\overline{CMDVCC}$ Low Within a Card Session.** Output $\overline{OFF\_}$ goes low when a fault condition is detected, and an emergency deactivation is performed automatically (Figure 7). When the system controller resets $\overline{CMDVCC}$ to high, it may sense the $\overline{OFF\_}$ level again after completing the deactivation sequence. This distinguishes between a card extraction and a hardware problem ($\overline{OFF\_}$ goes high again if a card is present). Depending on the connector's card-present switch (normally closed or normally open) and the mechanical characteristics of the switch, bouncing can occur on the PRES_ signals at card insertion or withdrawal.

The device has a debounce feature with an 8ms typical duration (Figure 6). When a card is inserted, output $\overline{OFF\_}$ goes high after the debounce time delay. When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES_ and output $\overline{OFF\_}$ goes low.

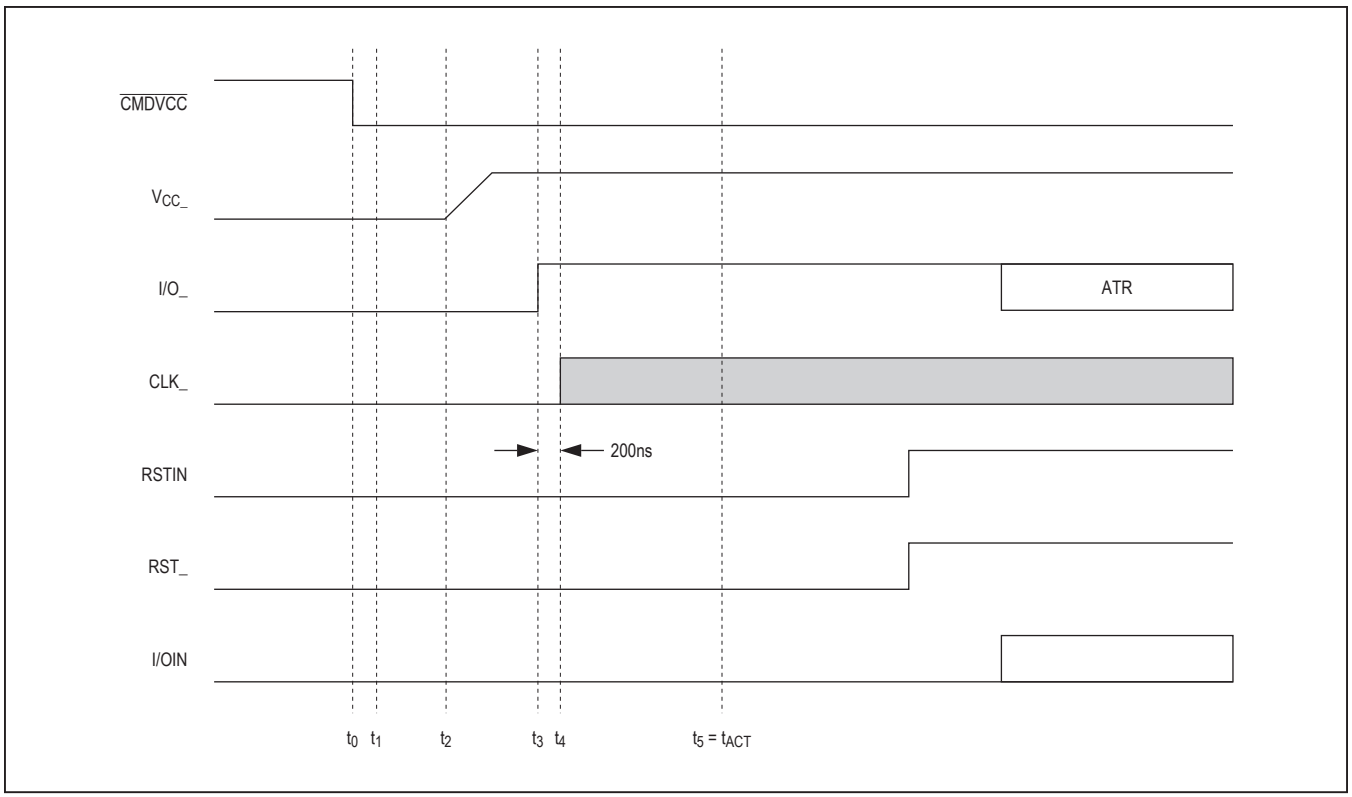



*Figure 4. Activation Sequence at $t_3$*

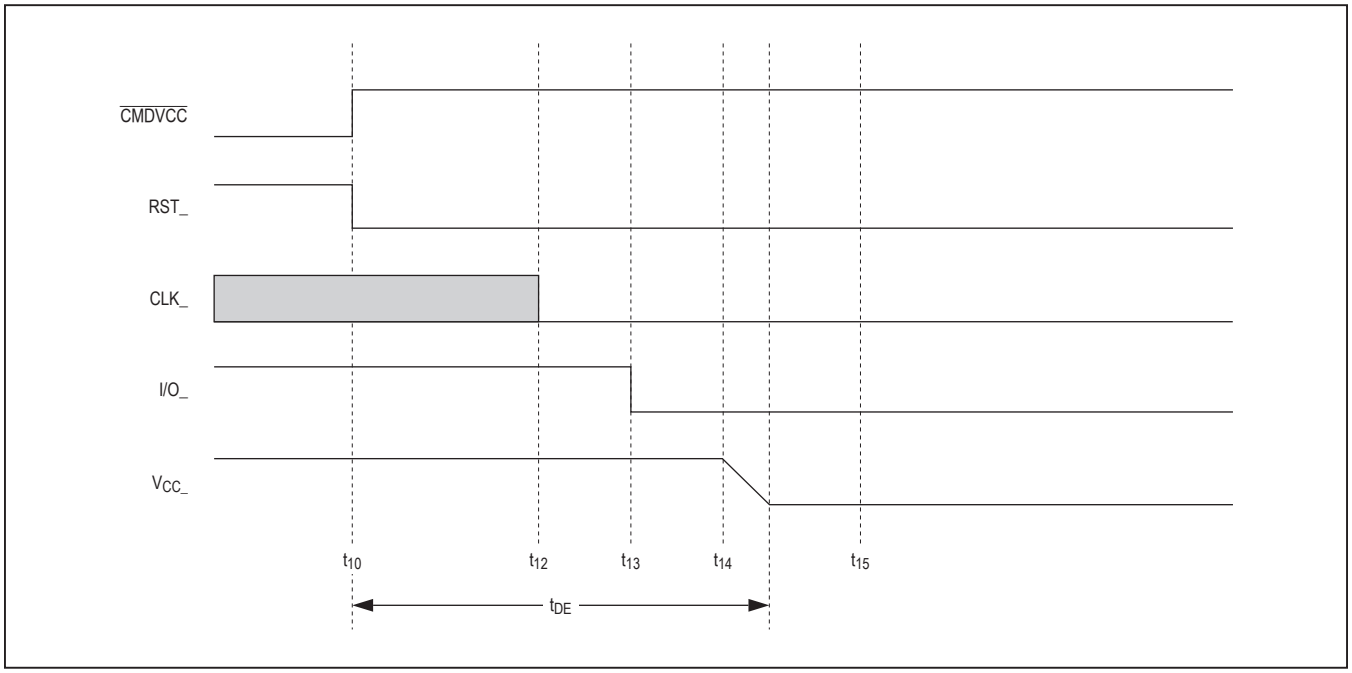



*Figure 5. Deactivation Sequence*

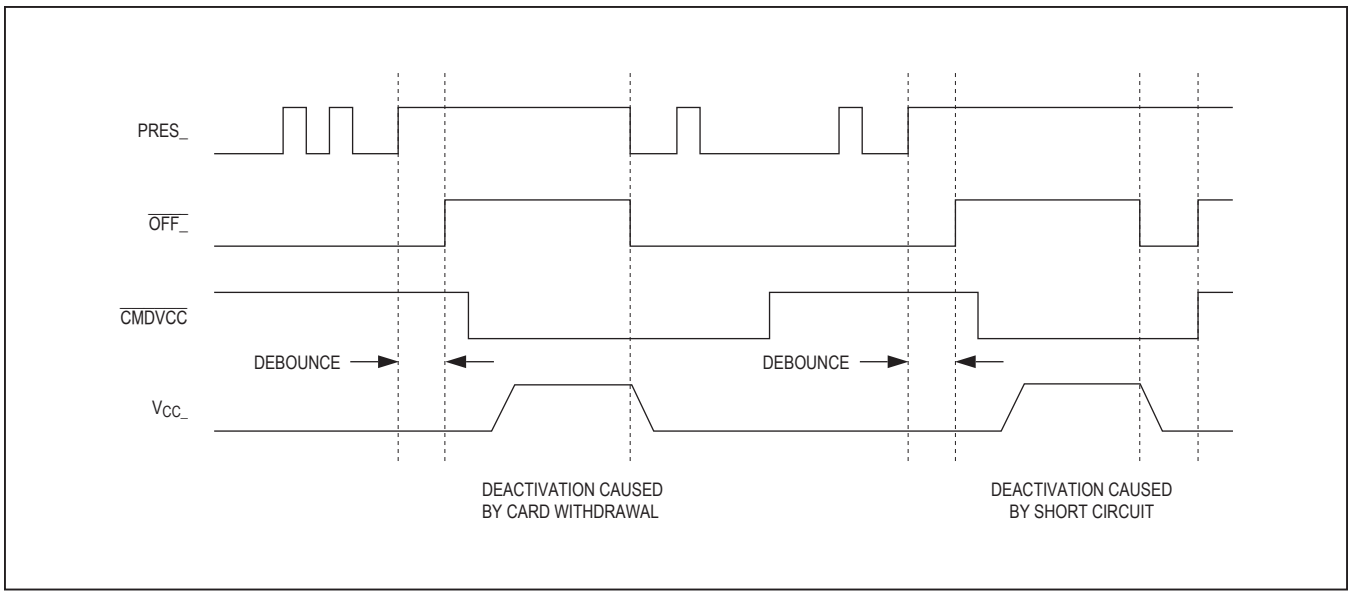



*Figure 6. Behavior of PRES_, OFF_, CMDVCC, and $V_{CC\_}$*

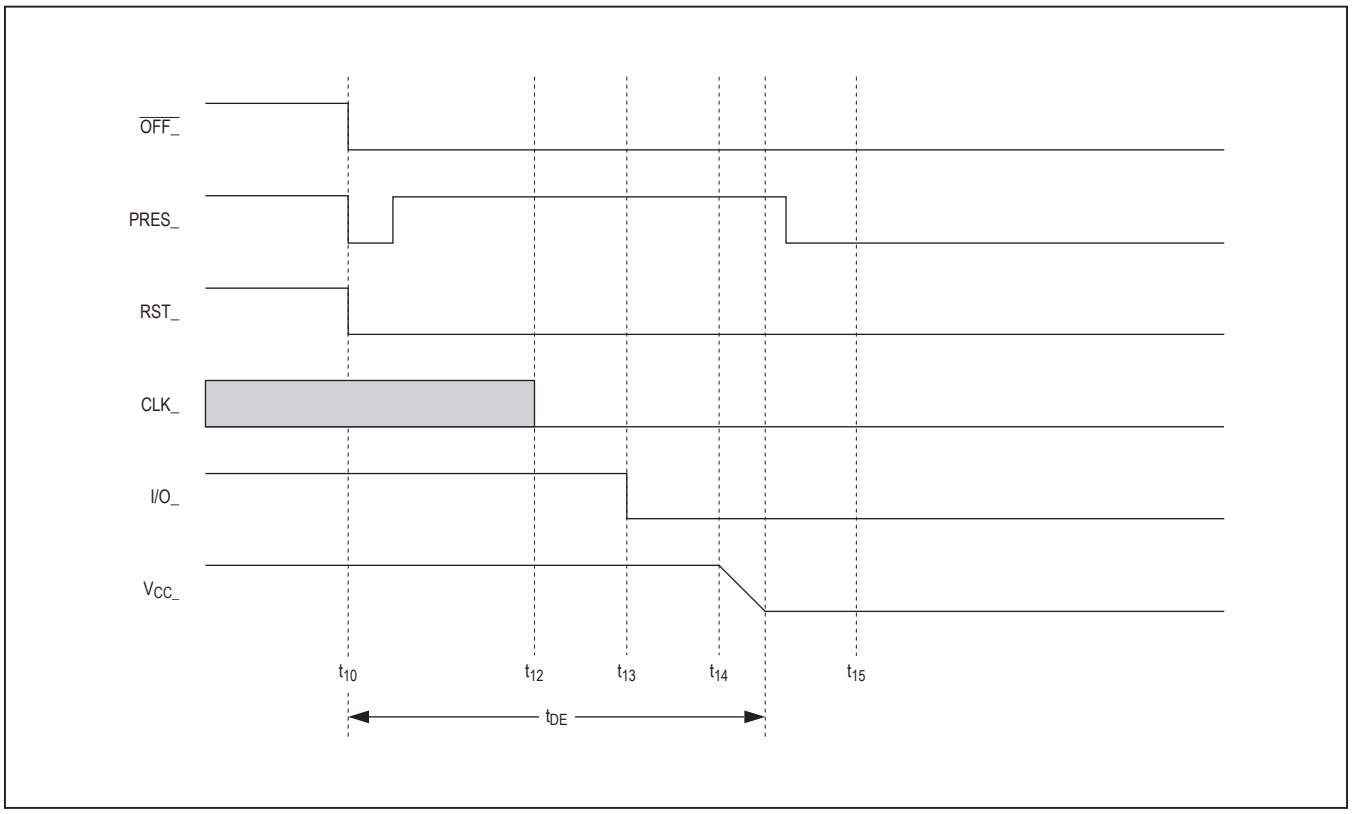



*Figure 7. Emergency Deactivation Sequence (Card Extraction)*

## Stop Mode (Low-Power Mode)

A low-power state, stop mode, can be entered by forcing the $\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V input pins to a logic-high state. Stop mode can only be entered when the smart card interface is inactive. In stop mode, all internal analog circuits are disabled. The $\overline{OFF\_}$ pin follows the status of the PRES_ pin. To exit stop mode, change the state of one or more of the three control pins to a logic-low. An internal 220µs (typ) power-up delay and the 8ms PRES_ debounce delay are in effect and $\overline{OFF\_}$ is asserted to allow the internal circuitry to stabilize. This prevents smart card access from occurring after leaving stop mode. Figure 8 shows the control sequence for entering and exiting stop mode. Note that an in-progress deactivation sequence always finishes before the device enters low-power stop mode.

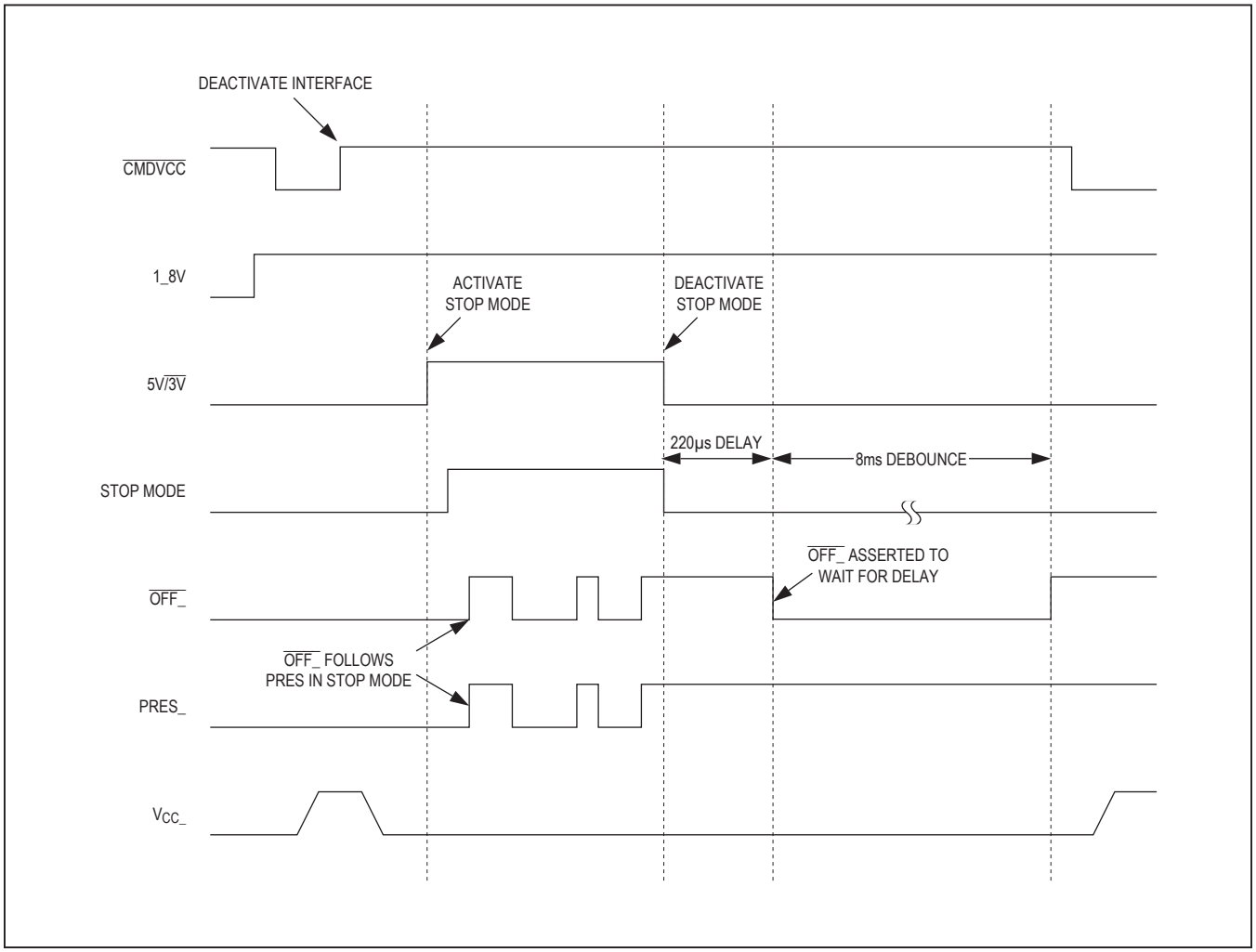



*Figure 8. Stop-Mode Sequence*

## Smart Card Power Select

The device supports three smart card $V_{CC}$ voltages: 1.8V, 3V, and 5V. The power select is controlled by the 1_8V and 5V/$\overline{3V}$ signals as shown in Table 3. The 1_8V signal has priority over 5V/$\overline{3V}$. When 1_8V is asserted high, 1.8V is applied to $V_{CC}$ when the smart card is active. When 1_8V is deasserted, 5V/$\overline{3V}$ dictates $V_{CC}$ power range. $V_{CC}$ is 5V if 5V/$\overline{3V}$ is asserted to a logic-high state, and $V_{CC}$ is 3V if 5V/$\overline{3V}$ is pulled to a logic-low state. Care must be exercised when switching from one $V_{CC}$ power selection to the other. If both 1_8V and 5V/$\overline{3V}$ are high with $\overline{CMDVCC}$ high at the same time, the device enters stop mode. To avoid accidental entry into stop mode, the state of 1_8V and 5V/$\overline{3V}$ must not be changed simultaneously. A minimum delay of 100ns should be observed between changing the states of 1_8V and 5V/$\overline{3V}$. See Figure 9 for the recommended sequence of changing the $V_{CC}$ range.

## Table 3. $V_{CC}$ Select and Operation Mode

| 1_8V | 5V/$\overline{3V}$ | $\overline{CMDVCC}$ | $V_{CC}$ SELECT (V) | CARD INTERFACE STATUS |
|---|---|---|---|---|
| 0 | 0 | 0 | 3 | Activated |
| 0 | 0 | 1 | 3 | Inactivated |
| 0 | 1 | 0 | 5 | Activated |
| 0 | 1 | 1 | 5 | Inactivated |
| 1 | 0 | 0 | 1.8 | Activated |
| 1 | 0 | 1 | 1.8 | Inactivated |
| 1 | 1 | 0 | 1.8 | Reserved (Activated) |
| 1 | 1 | 1 | 1.8 | Not Applicable—Stop Mode |

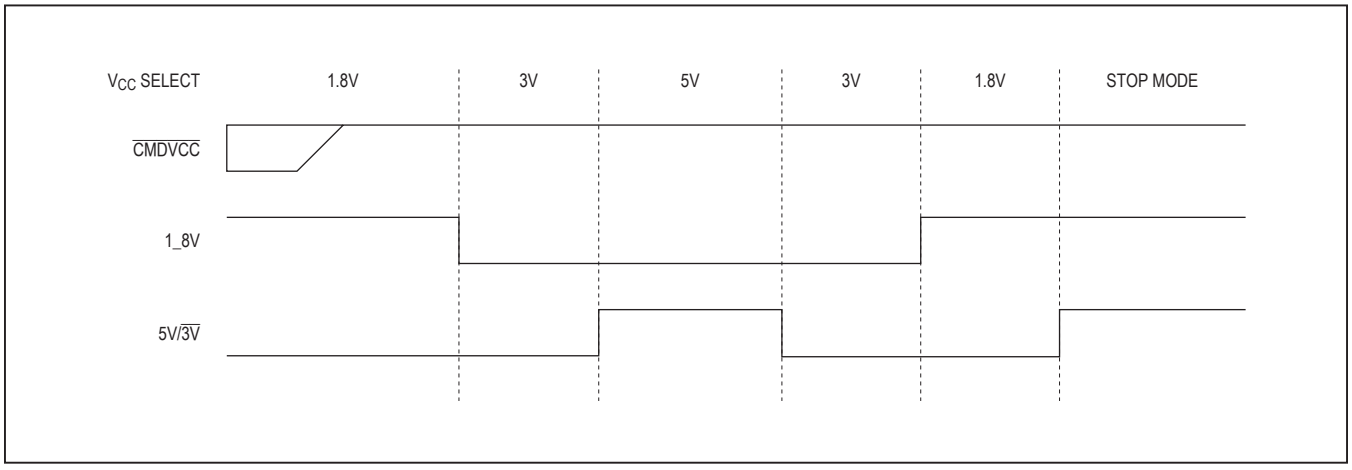



*Figure 9. Smart Card Power Select*

## Switching A/B Interfaces

One of the device's key features is the ability to manage two card slots at the same time. The multiplexing control signal SEL_AB is used to determine which interface is active for communication, though it is possible to leave both interfaces powered at the same time.

When switching between interfaces, the device preserves the state of control signals CLKDIV1, CLKDIV2, 1.8V, 5V/$\overline{3V}$, $\overline{CMDVCC}$, and RSTIN by latching the pin states. This allows the now inactive interface to stay powered while the other interface is activated for communication, and it also allows for fast switching between card interfaces without the need for a card deactivation and activation sequence.

When switching interfaces, the host must reset the control pins in the same configuration that was last used for that interface. Approximately 78µs after the SEL_AB transition, the device compares its internal state for the selected interface to the present state of the control pins. If the present state of the control pins does not match the previously latched state, the device does not perform the switchover correctly and enters an unknown state. This means that the host must always record the state of the control pins for the current interface before performing a switchover.

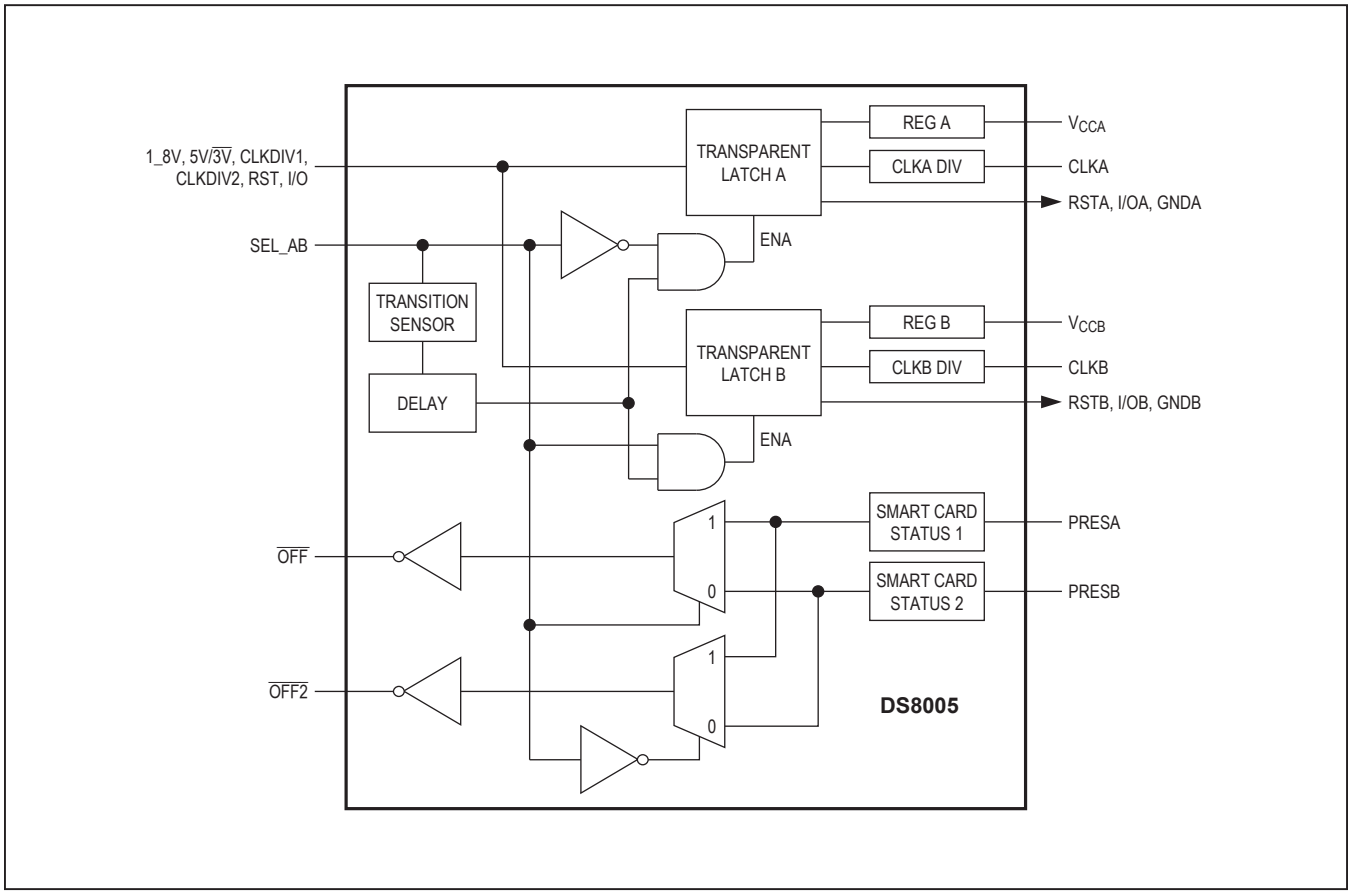



*Figure 10. Switching A/B Interfaces*

The following procedure summarizes the procedure when switching from card A to card B, and vice versa:

**Note:** The host must have previously recorded the state of the control pins for the card B interface.

1) The host must record the state of the control pins for the card A interface.
2) Ensure that the control pin configuration does not change state less than 220µs before changing the SEL_AB pin.
3) Switch SEL_AB to the desired valued.
4) Within 78µs, the host must restore the control pins the state previously recorded for the card B interface.
5) Wait at least 42µs before reconfiguring the control pins to change card B to a new state.

Note that the behavior of the $\overline{OFF}$ and $\overline{OFF2}$ pins is dependent on the SEL_AB pin. $\overline{OFF}$ always refers to the active interface, and $\overline{OFF2}$ always reports events on the inactive interface. This allows the device to monitor for card insertion and removal on both interfaces simultaneously. See Figure 10 for details on the behavior of the SEL_AB, $\overline{OFF}$, and $\overline{OFF2}$ pins with regard to card presence.

## Applications Information

Performance can be affected by the layout of the application. For example, an additional cross-capacitance of 1pF between card reader contacts C2 (RST_) and C3 (CLK_) or C2 (RST_) and C7 (I/O_) can cause contact C2 to be polluted with high-frequency noise from C3 (or C7). In this case, include a 100pF capacitor between contacts C2 and CGND.

Application recommendations include the following:

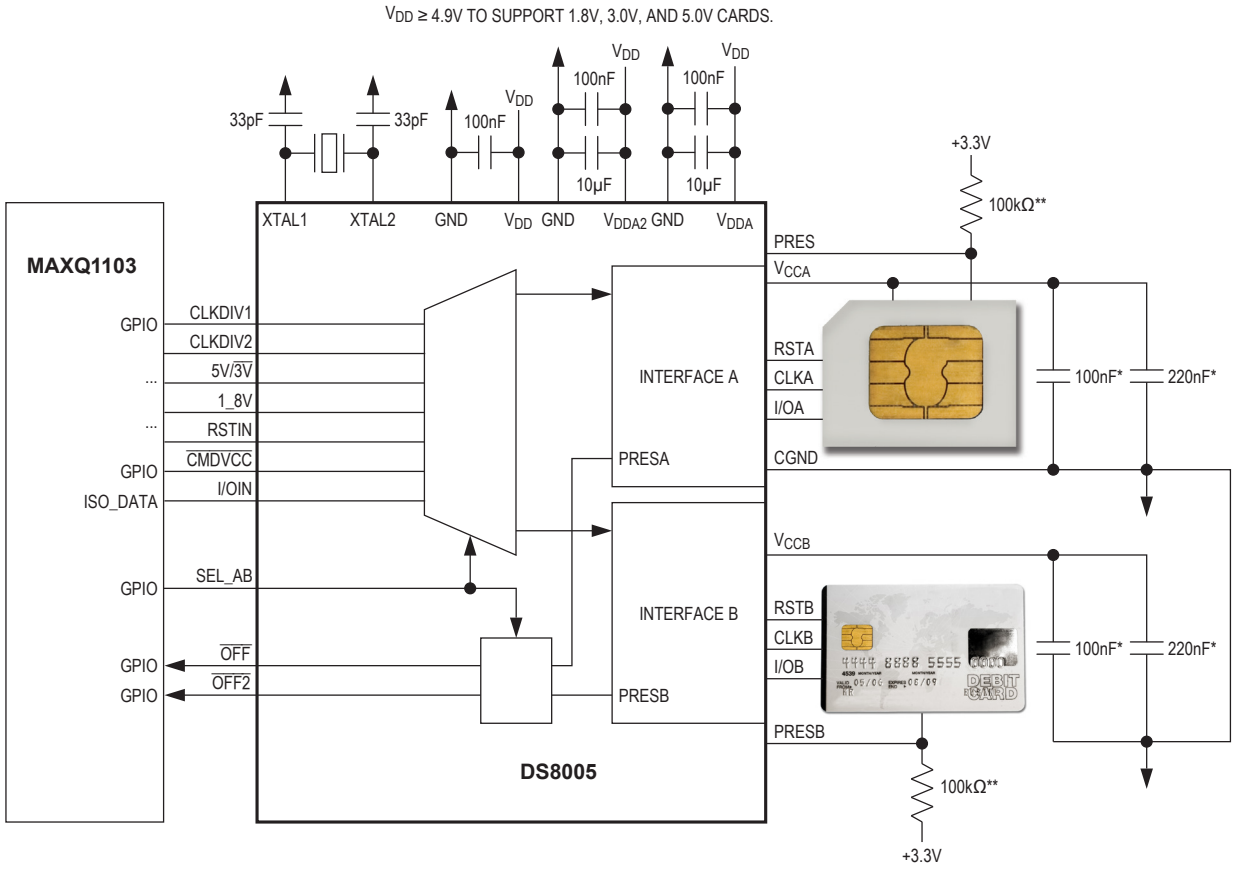
- Ensure there is ample ground area around the device and the connector; place the device very near to the connector; decouple the $V_{DD}$ and $V_{DDA}$ lines separately. These lines are best positioned under the connector.
- The device and the host microcontroller must use the same $V_{DD}$ supply. Pins CLKDIV1, CLKDIV2, $\overline{RSTIN}$, PRES_, I/OIN, 5V/$\overline{3V}$, 1_8V, $\overline{CMDVCC}$, and $\overline{OFF}$ are referenced to $V_{DD}$; if pin XTAL1 is to be driven by an external clock, also reference this pin to $V_{DD}$.
- Trace C3 (CLK) should be placed as far as possible from the other traces.
- The trace connecting CGND to C5 (GND) should be straight (the two capacitors on C1 ($V_{CC}$_) should be connected to this ground trace).
- Avoid ground loops between CGND and GND.
- Decouple $V_{DDA}$ and $V_{DD}$ separately. If two supplies are the same in the application, they should be connected in a star on the main trace

With all these layout precautions, noise should be kept to an acceptable level and jitter on C3 (CLK_) should be less than 100ps. Reference layouts are available on request.

## Technical Support

For technical support, go to **https://support.maximintegrated.com/micro**.

## Typical Application Circuit




*PLACE A 100nF CAPACITOR CLOSE TO THE DS8005 AND PLACE A 220nF CAPACITOR CLOSE TO CARD CONTACT.
**SCHEMATIC ASSUMES A NORMALLY CLOSED CONNECTION TO GROUND IN THE SOCKET. INSERTING A CARD BREAKS THE CONNECTION AND PULLS PRES HIGH.

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 28 SO | W28+1 | 21-0042 | 90-0109 |
| 28 TSSOP | U28+1 | 21-0066 | 90-0171 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 4/10 | Initial release | — |
| 1 | 7/15 | Added 28 TSSOP package, clarified function of $V_{DDA}$ and $V_{DDA2}$ pins, added $V_{DDA2}$ pin by passing and clarified default state of PRES pins in *Typical Application Circuit* | 1, 7, 8, 19 |
| 2 | 9/17 | Updated *Switching Interfaces A/B* section | 17, 18 |